CMOS 4-Bit Microcontroller

TMP47E186M
TMP47E187M

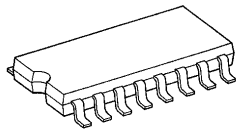
TMP47E186M/187M is a high-speed, advanced single-chip 4-bit microcomputer with built-in ROM, RAM, E^2PROM, SPI, I/O ports, a timer / counter.

Model	ROM	RAM	E^2PROM	Package	Oscillator	Built-in OTP
TMP47E186M	1024 × 8-bit	64 × 4-bit	16 × 8-bit	P-SOP16-300-1.27	CR oscillator	TMP47P186M
TMP47E187M					crystal/ceramic oscillator	TMP47P187M

Features

- 4-bit single-chip microcomputer
- Minimum instruction execution time: 1.3 μs (at 6 MHz)
- Minimum operating power supply voltage:
  TMP47E186M: 2.2 V (with 2.5 MHz CR oscillator)
  2.0 V (with 1.0 MHz CR oscillator)
  TMP47E187M: 2.7 V (with 4.2 MHz crystal/ceramic oscillator)
- Power dissipation in hold mode:
  Typ. 0.5 μA (TOPR = – 40 to 85°C)
- Basic machine instructions: 89
- Subroutine nesting level: 15 max
- Six independently latched interrupts
  (two external, four internal) offering multiple interrupt control
- I/O ports: 11 pins, defined as input or output by corresponding port data direction register
- 8-bit synchronous serial interface (SPI)
- Built-in 16 × 8-bit E^2PROM
  Can be rewritten in units of byte.
  Automatic rewrite time setting (built-in timer, write or delete in 4 ms)
  Ready/busy status monitor
- 12-bit timer / counter (TC2)
  Timer, event counter, pulse width measuring mode
- 12-bit programmable timer (TC1)

P-SOP16-300-1.27



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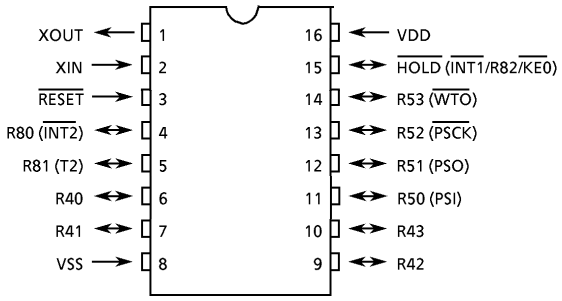
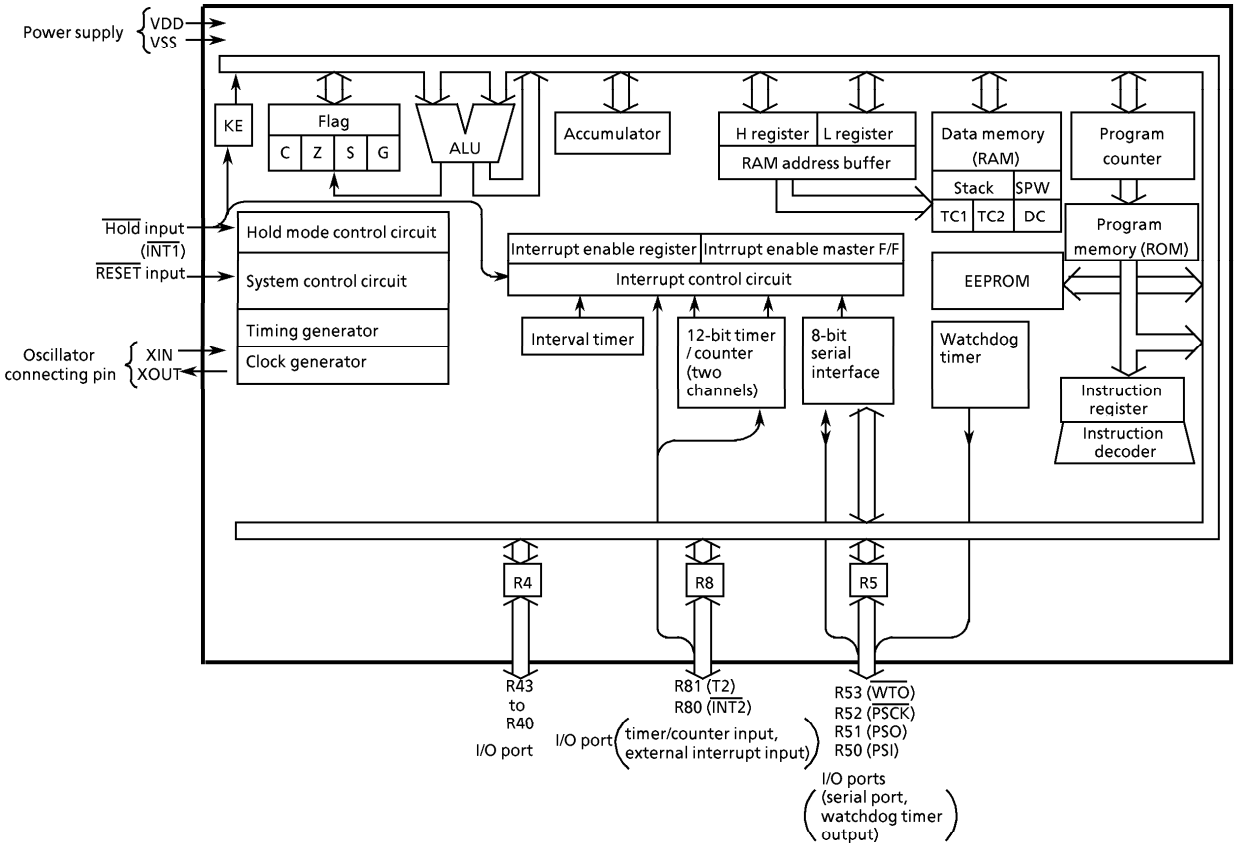
- Interval timer
- Watchdog timer
- Hold function: battery / capacitor backup
- Package: 16-pin SOP

Pin Assignment (Top View)

P-SOP16-300-1.27



Block Diagram



Pin Functions

Pin name	I/O	Function	
R43 to R40	I/O	4-bit latched I/O port. I/O set with DDR. Can be set, cleared, or tested in units of bits by bit manipulation instructions using L register indirect addressing.	
R53 ($\overline{WTO}$)	I/O (output)	4-bit latched I/O port. I/O set with DDR .	Watchdog timer output
R52 ($\overline{PSCK}$)	I/O (I/O)		Serial clock I/O
R51 ($\overline{PSO}$)	I/O (output)		Serial data output
R50 ($\overline{PSI}$)	I/O (input)		Serial data input
R81 (T2)	I/O (input)	2-bit latched I/O port I/O set with DDR	Timer / counter 2 input
R80 (INT2)			External interrupt 2 input
XIN	Input	Oscillator connecting pin. If an external clock is used, the input is XIN and XOUT is open circuit.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{INT1}$ / R82 / $\overline{KE0}$)	Input (I/O)	Hold request / release signal input	External interrupt 1 input, R82 I/O and hold signal sense input.
VDD	Power supply	+ 5 V (or other voltage)	
VSS		0 V (GND)	

Operation

The following is a description of the hardware functions and operation of TMP47E186/187. The configuration of the basic machine instructions for TMP47E186/187 is the same as that for the TLCS-47E series.

1. Configuration

- CPU core functions
  - 2.1 Program counter (PC)
  - 2.2 Program memory (ROM)
  - 2.3 H register, L register
  - 2.4 Data memory (RAM)
    - Stack
    - Stack pointer word (SPW)
    - Data counter (DC)
  - 2.5 Non-volatile data memory (E^2PROM)
  - 2.6 ALU, Accumulator
  - 2.7 Flag
  - 2.8 System control circuit
  - 2.9 Interrupt control circuit
  - 2.10 Reset circuit
- Peripheral hardware functions
  - 3.1 I/O ports
  - 3.2 Interval timer
  - 3.3 Timer/counters (TC1, TC2)
  - 3.4 Watchdog timer
  - 3.5 Serial interface (SPI)

2. CPU Core Functions

2.1 Program Counter (PC)

The program counter is a 10-bit register that holds the address of the next program instruction to be executed. At each instruction fetch, the register is incremented by the number of bytes fetched. Table 2-1 shows the operation of the program counter on execution of a jump or subroutine instruction, or on receipt of an interrupt. At reset, the PC is initialized to 0.

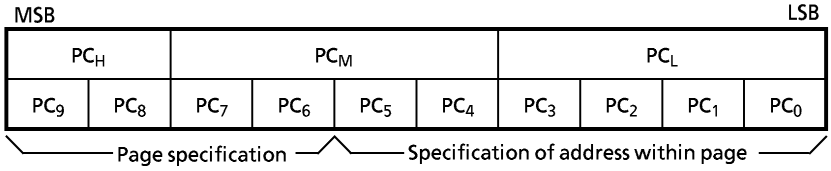


Figure 2-1. Program Counter configuration

The program counter directly addresses 1024 bytes of memory. Note the following points concerning short branch instructions.

- In-page branch instruction [BSS a]
  If the branch condition is satisfied on execution of the [BSS a] instruction, the branch value specified in the instruction is set in the lower six bits of the PC.
  If the [BSS a] instruction occurs at the final address in a page, the upper four bits of the PC point to the next instruction, which is within the next page. Therefore, the instruction will branch to an address within the next page.

2.2 Program Memory (ROM)

Program instructions and fixed data are stored in program memory. The program counter holds the address of the next program instruction to be executed.
The table look-up instructions are used to read fixed data.

- Table look-up instructions: [LDL, A,@DC], [LDH A,@DC +]
  The table look-up instructions read the upper or lower four bits of data stored at the ROM address specified by the data counter (DC) and load the result in the accumulator. (The [LDL A,@DC] instruction reads the lower four bits. The [LDH A,@DC +] instruction reads the upper four bits.) The DC consists of twelve bits and can specify any address in program memory. The upper two bits of the data counter are ignored.

Table 2-1. Operation of Program Counter

Instruction or operation		Condition		Program Counter (PC)									
				PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
Instruction execution	BS a	SF = 1 (branch condition satisfied)		Value specified in instruction									
		SF = 0 (branch condition not satisfied)		+ 2									
	BSS a	SF = 1	Lower six bits of address ≠ 1111111	No change						Value specified in instruction			
			Upper six bits of address = 1111111 (final address in page)	+ 1						Value specified in instruction			
		SF = 0		+ 1									
	CALL a			Value specified in instruction									
	CALLS a			0	0	Value generated from value specified in instruction					1	1	0
	RET			Return address restored from stack									
	RETI			Return address restored from stack									
	Other instructions			Incremented by number of bytes of instruction									
At interrupt				0	0	0	0	0	0	Interrupt vector			0
At reset				0	0	0	0	0	0	0	0	0	0

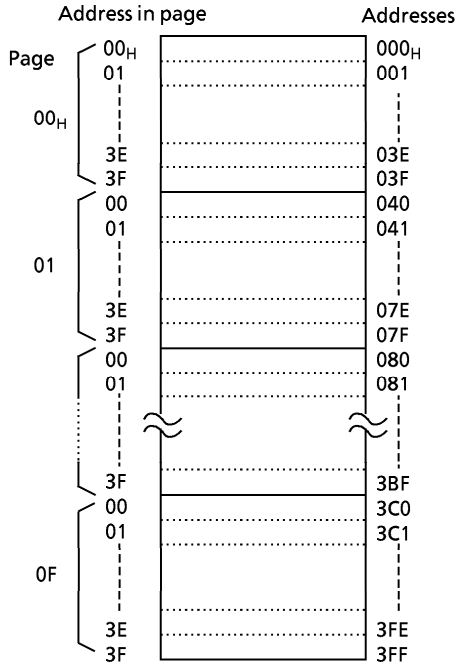


Figure 2-2. rogram Memory Configuration

2.2.1 Program Memory Map

TMP47E186/187 incorporates 1024 x 8 bits (addresses 000 to $3FF_H$) of program memory (mask ROM). Figure 2-3 is the program memory map. Program memory addresses 000 to $3FF_H$ can also be used for special applications.

2.2.2 Program Memory Capacity

TMP47E186/187 does not have physical memory at addresses 400 to $7FF_H$. However, if the program accesses addresses within this range, the processor treats the upper two bits of the addresses as 0 and reads the contents of the corresponding program memory at addresses 000 to $3FF_H$.

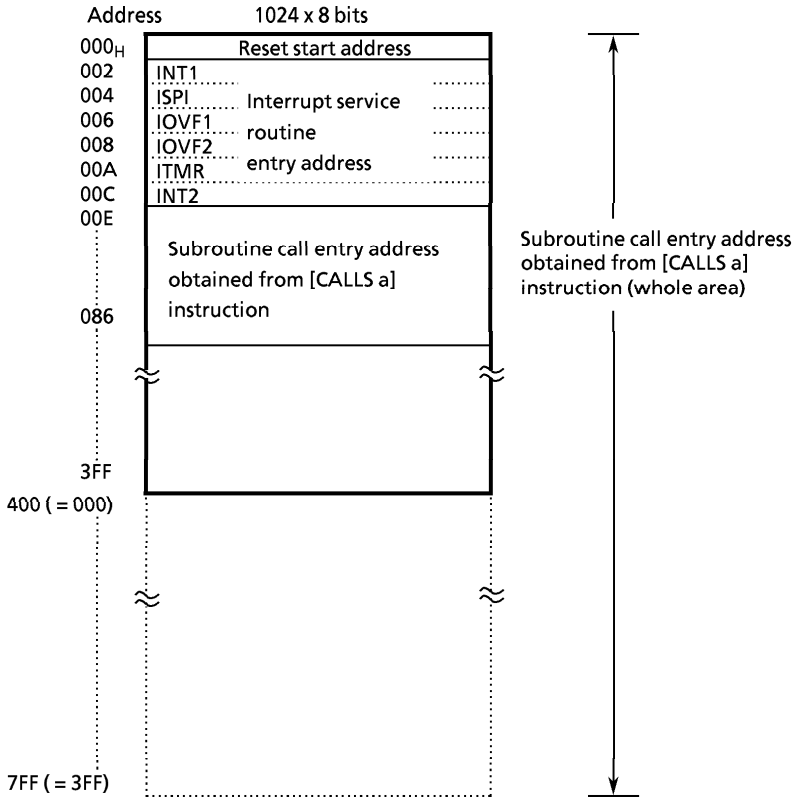


Figure 2-3. Program Memory Map

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pin	Specifications	Unit
Power supply voltage	V_{DD}		– 0.3 to 6.5	V
Input voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output current (per pin)	I_{OUT}		3	mA
Output current (total for all pins)	ΣI_{OUT}		12	mA
Power dissipation	PD		88	mW
Soldering temperature (time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		– 55 to 125	°C
Operating temperature	T_{OPR}		– 40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Power supply voltage	V_{DD}	At normal operation	Crystar or ceramic (Note 2)	fc = 6.0 MHz	4.5	5.5	V
				fc = 4.2 MHz	2.7		
			RC (Note 3)	fc = 2.5 MHz	2.2		
				fc = 1 MHz	2.0		
		In hold mode	–	–	2.0		
High-level input voltage	V_{IH1}	Excluding hysteresis input	VDD ≧ 4.5 V		V_{DD} × 0.7	VDD	V
	V_{IH2}	Hysteresis input			V_{DD} × 0.75		
	V_{IH3}		VDD < 4.5 V		V_{DD} × 0.9		
Low-level input voltage	V_{IL1}	Excluding hysteresis input	VDD ≧ 4.5 V		0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis input				V_{DD} × 0.25	
	V_{IL3}		VDD < 4.5 V			V_{DD} × 0.1	
Clock frequency	fc	XIN, XOUT	VDD = 4.5 to 5.5 V		0.4	0.6	MHz
			VDD = 2.7 to 5.5 V			4.2	
			VDD = 2.2 to 5.5 V (CR)			2.5	
			VDD = 2.0 to 5.5 V (CR)			1.0	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: TMP47E187M

Note 3: TMP47E186M

DC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pin	Condition	Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input		–	0.7	–	V
Input current	I_{IN1}	$\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	μA
Input resistance	R_{IN}	$\overline{RESET}$		100	220	450	kΩ
High-level output current	V_{OH}	Push-pull output portH	VDD = 4.5 V, IOH = – 1.6 mA	2.4	–	–	V
			VDD = 2.2 V, IOH = – 20 μA	2.0	–	–	
Low-level output voltage	V_{OL}	Excluding XOUT	VDD = 4.5 V, IOL = 1.6 mA	–	–	0.4	V
			VDD = 2.2 V, IOL = 20 μA	–	–	0.1	
Power supply current at normal operation	I_{DD}	Except for E²PROM Erase / write	V_{DD} = 5.5 V, fc = 4 MHz	–	2	4	mA
			V_{DD} = 3.0 V, fc = 4 MHz	–	1	2	
			V_{DD} = 3.0 V, fc = 400 kHz	–	0.5	1	
		During E²PROM Erase / write	V_{DD} = 5.5 V, fc = 4 MHz	–	5	7	
Power supply current in hold mode	I_{DDH}		V_{DD} = 5.5 V	–	0.5	10	μA
			V_{DD} = 3.0 V	–	0.3	1	

Note 1: Typ. values are for when Topr = 25°C, V_{DD} = 5 V.

Note 2: Input current: IIN1 excludes current due to built-in pull-up resistors.

Note 3: VIN = 5.3 V / 0.2 V (V_{DD} = 5 V) or VIN = 2.8 V / 0.2 V (V_{DD} = 3.0 V)

E²PROM Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition		Unit
Programming time	t_{PW}		4.1 (Typ.)	ms
Erase time	t_{EW}		4.1 (Typ.)	
Number of rewrites		Topr = T_H, V_{DD} = 5 V	10^4 (Min.)	cycle
Data retention characteristics		After rewriting 10^4 times, Ta = 55°C	10 (Min.)	year

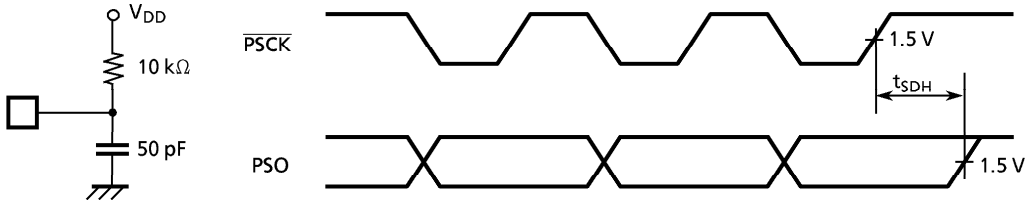
AC Characteristics (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition		Min	Typ.	Max	Unit
Instruction cycle time	tcy		V_{DD} = 4.5 to 5.5 V	1.3	–	20	μs
			V_{DD} = 2.7 to 5.5 V	1.9			
			V_{DD} = 2.2 to 5.5 V	3.2 *1			
			V_{DD} = 2.0 to 5.5 V	8.0 *1			
High-level clock pulse width	t_{WCH}	External clock (XIN input)	$V_{DD} \geqq 2.7$ V	80	–	–	ns
			$V_{DD} < 2.7$ V	160			
Low-level clock pulse width	t_{WCL}		$V_{DD} \geqq 2.7$ V	80			
			$V_{DD} < 2.7$ V	160			
Shift data storage time	t_{SDH}			0.5 tcy – 0.3	–	–	μs

*1: TMP47E186M only

Note: Shift data retention time: $\overline{PSCK}$ and PSO pin external circuits

Serial ports (Transmission ended)



Recommended Oscillation Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

(1) 6 MHz (TMP47E187M) (VDD = 4.5 to 5.5 V)

Ceramic oscillator

CSA6.00MGU (Murata Mfg. Co., Ltd.)	CXIN = CXOUT = 30 pF
KBR-6.0MS (Kyocera)	〃
EFOEC6004A4 (Matsushita Electronic Components)	〃

(2) 4 MHz (TMP47E187M) (VDD = 2.7 to 5.5 V)

Ceramic oscillator

CSA4.00MG (Murata Mfg.Co., Ltd.)	CXIN = CXOUT = 30 pF
KBR-4.0MS (Kyocera)	〃
EFOEC4004A4 (Matsushita Electronic Components)	〃

Crystal oscillator

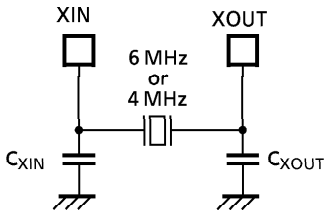
204B 4.0000 (TOYOCOM)	CXIN = CXOUT = 20 pF

(3) 400 kHz (TMP47E187M) (VDD = 2.7 to 5.5 V)

Ceramic oscillator

CSB400P (Murata Mfg. Co., Ltd.)	CXIN = CXOUT = 220 pF, RXOUT = 6.8 kΩ
KBR-400B (Kyocera)	CXIN = CXOUT = 100 pF, RXOUT = 10 kΩ
EFOA400K04B (Matsushita Electronic Components)	CXIN = CXOUT = 470 pF, RXOUT = 0 Ω

TMP47E187M



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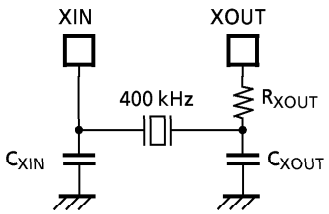
TMP47E187M



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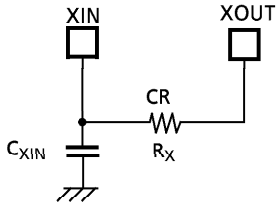
TMP47E186M



CR Oscillation Circuit