# XC18V00 Series of In-System Programmable Configuration PROMs

DS026 (v3.2) February 27, 2002

**Product Specification**

## Features

- In-system programmable 3.3V PROMs for configuration of Xilinx FPGAs
    - Endurance of 20,000 program/erase cycles
    - Program/erase over full commercial/industrial voltage and temperature range
- IEEE Std 1149.1 boundary-scan (JTAG) support
- Simple interface to the FPGA
- Cascadable for storing longer or multiple bitstreams
- Low-power advanced CMOS FLASH process
- Dual configuration modes
    - Serial Slow/Fast configuration (up to 33 MHz)
    - Parallel (up to 264 Mb/s at 33 MHz)
- 5V tolerant I/O pins accept 5V, 3.3V and 2.5V signals
- 3.3V or 2.5V output capability
- Available in PC20, SO20, PC44 and VQ44 packages
- Design support using the Xilinx Alliance and Foundation series software packages.
- JTAG command initiation of standard FPGA configuration

## Description

Xilinx introduces the XC18V00 series of in-system programmable configuration PROMs (Figure 1). Initial devices in this 3.3V family are a 4-megabit, a 2-megabit, a 1-megabit, a 512-Kbit, and a 256-Kbit PROM that provide an easy-to-use, cost-effective method for re-programming and storing large Xilinx FPGA or CPLD configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising CCLK, data is available on the PROM DATA (D0) pin that is connected to the FPGA $D_{IN}$ pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. When the FPGA is in Slave Serial mode, the PROM and the FPGA are clocked by an external clock.

When the FPGA is in Slave-Parallel or SelectMAP Mode, an external oscillator generates the configuration clock that drives the PROM and the FPGA. After the rising CCLK edge, data are available on the PROMs DATA (D0-D7) pins. The data is clocked into the FPGA on the following rising edge of the CCLK. Neither Slave-Parallel nor SelectMAP utilize a Length Count, so a free-running oscillator can be used.

Multiple devices can be concatenated by using the $\overline{\text{CEO}}$ output to drive the $\overline{\text{CE}}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family or with the XC17V00 one-time programmable Serial PROM family.

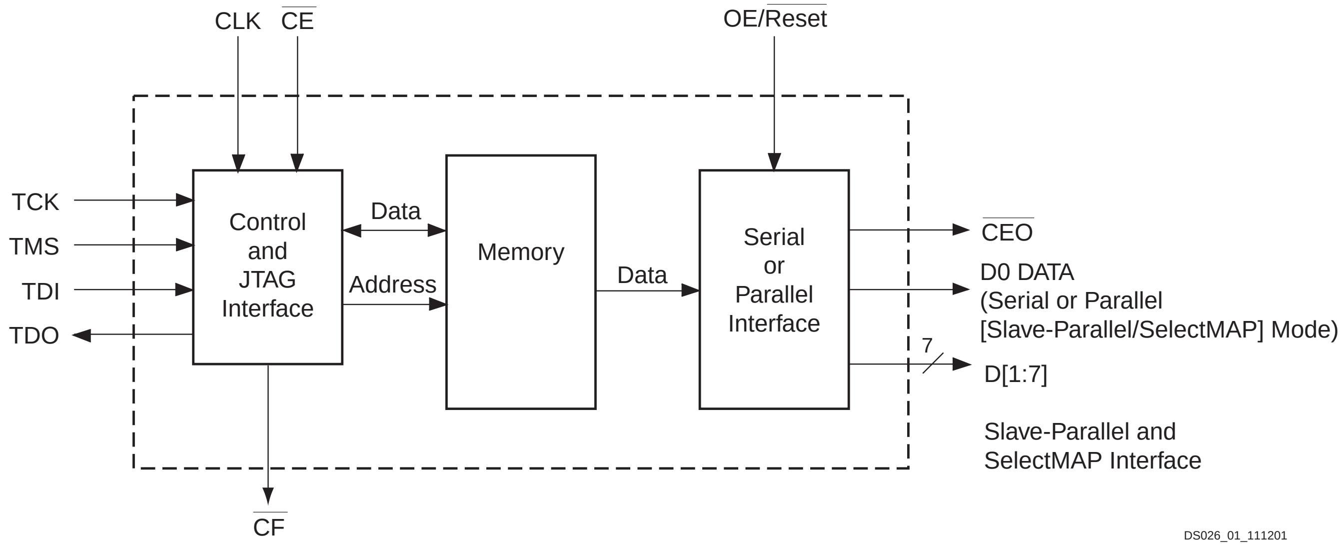


*Figure 1:* **XC18V00 Series Block Diagram**

## Pinout and Pin Description

*Table 1:* **Pin Names and Descriptions (pins not listed are "no connect")**

| Pin Name | Boundary Scan Order | Function | Pin Description | 44-pin VQFP | 44-pin PLCC | 20-pin SOIC and PLCC |
|---|---|---|---|---|---|---|
| D0 | 4 | DATA OUT | D0 is the DATA output pin to provide data for configuring an FPGA in serial mode. | 40 | 2 | 1 |
| | 3 | OUTPUT ENABLE | | | | |
| D1 | 6 | DATA OUT | D0-D7 are the output pins to provide parallel data for configuring a Xilinx FPGA in Slave-Parallel/SelectMap mode. | 29 | 35 | 16 |
| | 5 | OUTPUT ENABLE | | | | |
| D2 | 2 | DATA OUT | | 42 | 4 | 2 |
| | 1 | OUTPUT ENABLE | | | | |
| D3 | 8 | DATA OUT | | 27 | 33 | 15 |
| | 7 | OUTPUT ENABLE | | | | |
| D4 | 24 | DATA OUT | | 9 | 15 | 7(1) |
| | 23 | OUTPUT ENABLE | | | | |
| D5 | 10 | DATA OUT | | 25 | 31 | 14 |
| | 9 | OUTPUT ENABLE | | | | |
| D6 | 17 | DATA OUT | | 14 | 20 | 9 |
| | 16 | OUTPUT ENABLE | | | | |
| D7 | 14 | DATA OUT | | 19 | 25 | 12 |
| | 13 | OUTPUT ENABLE | | | | |
| CLK | 0 | DATA IN | Each rising edge on the CLK input increments the internal address counter if both $\overline{\text{CE}}$ is Low and OE/$\overline{\text{RESET}}$ is High. | 43 | 5 | 3 |
| OE/$\overline{\text{RESET}}$ | 20 | DATA IN | When Low, this input holds the address counter reset and the DATA output is in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM is reset. Polarity is NOT programmable. | 13 | 19 | 8 |
| | 19 | DATA OUT | | | | |
| | 18 | OUTPUT ENABLE | | | | |
| $\overline{\text{CE}}$ | 15 | DATA IN | When $\overline{\text{CE}}$ is High, this pin puts the device into standby mode and resets the address counter. The DATA output pin is in a high-impedance state, and the device is in low power standby mode. | 15 | 21 | 10 |

*Table 1:* **Pin Names and Descriptions (pins not listed are “no connect”) *(Continued)***

| Pin Name | Boundary Scan Order | Function | Pin Description | 44-pin VQFP | 44-pin PLCC | 20-pin SOIC and PLCC |
|---|---|---|---|---|---|---|
| $\overline{\text{CF}}$ | 22 | DATA OUT | Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command. | 10 | 16 | 7[1] |
| | 21 | OUTPUT ENABLE | | | | |
| $\overline{\text{CEO}}$ | 11 | DATA OUT | Chip Enable Output ($\overline{\text{CEO}}$) is connected to the $\overline{\text{CE}}$ input of the next PROM in the chain. This output is Low when $\overline{\text{CE}}$ is Low and OE/$\overline{\text{RESET}}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. When OE/$\overline{\text{RESET}}$ goes Low, $\overline{\text{CEO}}$ stays High until the PROM is brought out of reset by bringing OE/$\overline{\text{RESET}}$ High. | 21 | 27 | 13 |
| | 12 | OUTPUT ENABLE | | | | |
| GND | | | GND is the ground connection. | 6, 18, 28 & 41 | 3, 12, 24 & 34 | 11 |
| TMS | | MODE SELECT | The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50K ohm resistive pull-up on it to provide a logic “1” to the device if the pin is not driven. | 5 | 11 | 5 |
| TCK | | CLOCK | This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics. | 7 | 13 | 6 |
| TDI | | DATA IN | This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50K ohm resistive pull-up on it to provide a logic “1” to the system if the pin is not driven. | 3 | 9 | 4 |
| TDO | | DATA OUT | This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50K ohm resistive pull-up on it to provide a logic “1” to the system if the pin is not driven. | 31 | 37 | 17 |
| $V_{CC}$ | | | Positive 3.3V supply voltage for internal logic and input buffers. | 17, 35 & 38 | 23, 41 & 44 | 18 & 20 |
| $V_{CCO}$ | | | Positive 3.3V or 2.5V supply voltage connected to the output voltage drivers. | 8, 16, 26 & 36 | 14, 22, 32 & 42 | 19 |

**Notes:**

1. Pin 7 is $\overline{\text{CF}}$ in Serial Mode, D4 in Slave-Parallel Mode for 20-pin packages.

## Xilinx FPGAs and Compatible PROMs

Table 2 provides a list of Xilinx FPGAs and compatible PROMs.

*Table 2:* **Xilinx FPGAs and Compatible PROMs**

| Device | Configuration Bits | XC18V00 Solution |
|---|---|---|
| XC2VP2 | 1,305,440 | XC18V02 |
| XC2VP4 | 3,006,560 | XC18V04 |
| XC2VP7 | 4,485,472 | XC18V04 + XC18V512 |
| XC2VP20 | 8,214,624 | 2 0f XC18V04 |
| XC2VP50 | 19,021,408 | 5 of XC18V04 |
| XC2V40 | 360,160 | XC18V512 |
| XC2V80 | 635,360 | XC18V01 |
| XC2V250 | 1,697,248 | XC18V02 |
| XC2V500 | 2,761,952 | XC18V04 |
| XC2V1000 | 4,082,656 | XC18V04 |
| XC2V1500 | 5,659,360 | XC18V04 + XC18V02 |
| XC2V2000 | 7,492,064 | 2 of XC18V04 |
| XC2V3000 | 10,494,432 | 3 of XC18V04 |
| XC2V4000 | 15,660,000 | 4 of XC18V04 |
| XC2V6000 | 21,849,568 | 5 of XC18V04 + XC18V02 |
| XC2V8000 | 29,063,136 | 7 of XC18V04 |
| XCV50 | 559,200 | XC18V01 |
| XCV100 | 781,216 | XC18V01 |
| XCV150 | 1,040,096 | XC18V01 |
| XCV200 | 1,335,840 | XC18V02 |
| XCV300 | 1,751,808 | XC18V02 |
| XCV400 | 2,546,048 | XC18V04 |
| XCV600 | 3,607,968 | XC18V04 |
| XCV800 | 4,715,616 | XC18V04 + XC18V512 |
| XCV1000 | 6,127,744 | XC18V04 + XC18V02 |
| XCV50E | 630,048 | XC18V01 |
| XCV100E | 863,840 | XC18V01 |
| XCV200E | 1,442,106 | XC18V02 |
| XCV300E | 1,875,648 | XC18V02 |
| XCV400E | 2,693,440 | XC18V04 |
| XCV405E | 3,430,400 | XC18V04 |
| XCV600E | 3,961,632 | XC18V04 |
| XCV812E | 6,519,648 | 2 of XC18V04 |
| XCV1000E | 6,587,520 | 2 of XC18V04 |
| XCV1600E | 8,308,992 | 2 of XC18V04 |
| XCV2000E | 10,159,648 | 3 of XC18V04 |
| XCV2600E | 12,922,336 | 4 of XC18V04 |
| XCV3200E | 16,283,712 | 4 of XC18V04 |
| XC2S15 | 197,696 | XC18V256 |
| XC2S30 | 336,768 | XC18V512 |
| XC2S50 | 559,200 | XC18V01 |
| XC2S100 | 781,216 | XC18V01 |
| XC2S150 | 1,040,096 | XC18V01 |
| XC2S200 | 1,335,840 | XC18V02 |
| XC2S50E | 630,048 | XC18V01 |
| XC2S100E | 863,840 | XC18V01 |
| XC2S150E | 1,134,528 | XC18V02 |
| XC2S200E | 1,442,016 | XC18V02 |
| XC2S300E | 1,875,648 | XC18V02 |

## Capacity

| Devices | Configuration Bits |
|---|---|
| XC18V04 | 4,194,304 |
| XC18V02 | 2,097,152 |
| XC18V01 | 1,048,576 |
| XC18V512 | 524,288 |
| XC18V256 | 262,144 |

## In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be daisy-chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 2. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The Xilinx development system provides the programming data sequence using either Xilinx JTAG Programmer software and a download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The JTAG Programmer software also outputs serial vector format (SVF) files for use with any tools that accept SVF format and with automatic test equipment.

All outputs are held in a high-impedance state or held at clamp levels during in-system programming.

### OE/$\overline{\text{RESET}}$

The ISP programming algorithm requires issuance of a reset that causes OE to go Low.

## External Programming

Xilinx reprogrammable PROMs can also be programmed by the Xilinx HW-130 device programmer. This provides the added flexibility of using pre-programmed devices in board design and boundary-scan manufacturing tools, with an in-system programmable option for future enhancements and design changes.

## Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 20,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

## Design Security

The Xilinx in-system programmable PROM devices incorporate advanced data security features to fully protect the programming data against unauthorized reading. Table 3 shows the security setting available.

The read security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. When set, it allows device erase. Erasing the entire device is the only way to reset the read security bit.

*Table 3:* **Data Security Options**

| Default = Reset | Set |
|---|---|
| Read Allowed<br>Program/Erase Allowed | Read Inhibited via JTAG<br>Erase Allowed |

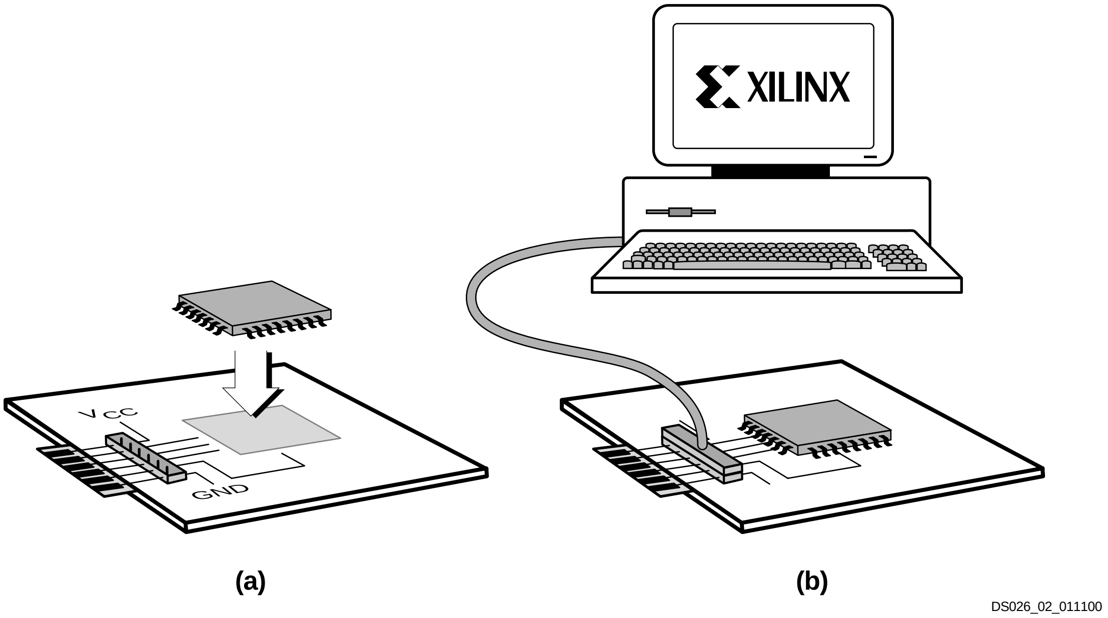


*Figure 2:* **In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable**

## IEEE 1149.1 Boundary-Scan (JTAG)

The XC18V00 family is fully compliant with the IEEE Std. 1149.1 Boundary-Scan, also known as JTAG. A Test Access Port (TAP) and registers are provided to support all required boundary scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the XC18V00 device.

Table 4 lists the required and optional boundary-scan instructions supported in the XC18V00. Refer to the IEEE Std. 1149.1 specification for a complete description of boundary-scan architecture and the required and optional instructions.

*Table 4:* **Boundary Scan Instructions**

| Boundary-Scan Command | Binary Code [7:0] | Description |
|---|---|---|
| **Required Instructions** | | |
| BYPASS | 11111111 | Enables BYPASS |
| SAMPLE/ PRELOAD | 00000001 | Enables boundary-scan SAMPLE/PRELOAD operation |
| EXTEST | 00000000 | Enables boundary-scan EXTEST operation |
| **Optional Instructions** | | |
| CLAMP | 11111010 | Enables boundary-scan CLAMP operation |
| HIGHZ | 11111100 | all outputs in high-impedance state simultaneously |
| IDCODE | 11111110 | Enables shifting out 32-bit IDCODE |
| USERCODE | 11111101 | Enables shifting out 32-bit USERCODE |
| **XC18V00 Specific Instructions** | | |
| CONFIG | 11101110 | Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low |

## Instruction Register

The Instruction Register (IR) for the XC18V00 is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI. The detailed composition of the instruction capture pattern is illustrated in Figure 3.

The ISP Status field, IR(4), contains logic “1” if the device is currently in ISP mode; otherwise, it contains logic “0”. The Security field, IR(3), contains logic “1” if the device has been programmed with the security option turned on; otherwise, it contains logic “0”.

| | IR[7:5] | IR[4] | IR[3] | IR[2] | IR[1:0] | |
|---|---|---|---|---|---|---|
| TDI-> | 0 0 0 | ISP Status | Security | 0 | 0 1 | ->TDO |

**Notes:**

1. IR(1:0) = 01 is specified by IEEE Std. 1149.1

*Figure 3:* **Instruction Register Values Loaded into IR as Part of an Instruction Scan Sequence**

## Boundary Scan Register

The boundary-scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the XC18V00 has two register stages that contribute to the boundary-scan register, while each input pin only has one register stage.

For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the High-Z enable state of the pin.

For each input pin, the register stage controls and observes the input state of the pin.

### Identification Registers

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG.

The IDCODE register has the following binary format:

```
vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1
```

where

v = the die version number
f = the family code (50h for XC18V00 family)
a = the ISP PROM product ID (26h for the XC18V04)
c = the company code (49h for Xilinx)

Note: The LSB of the IDCODE register is always read as logic “1” as defined by IEEE Std. 1149.1

Table 5 lists the IDCODE register values for the XC18V00 devices.

*Table 5:* **IDCODES Assigned to XC18V00 Devices**

| ISP-PROM | IDCODE |
|---|---|
| XC18V01 | 05024093h |
| XC18V02 | 05025093h |
| XC18V04 | 05026093h |
| XC18V256 | 05022093h |
| XC18V512 | 05023093h |

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device’s programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the XC18V00 device. If the device is blank or was not loaded during programming, the USERCODE register contains FFFFFFFFh.

## XC18V00 TAP Characteristics

The XC18V00 family performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the XC18V00 TAP are described as follows.

## TAP Timing

Figure 4 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations.

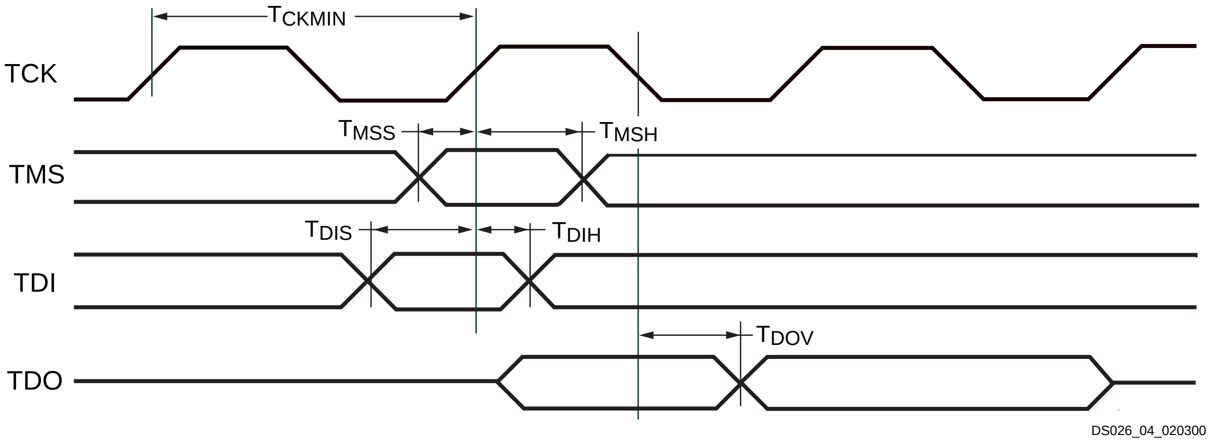


*Figure 4:* **Test Access Port Timing**

## TAP AC Parameters

Table 6 shows the timing parameters for the TAP waveforms shown in Figure 4

*Table 6:* **Test Access Port Timing Parameters**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CKMIN1}$ | TCK minimum clock period | 100 | - | ns |
| $T_{CKMIN2}$ | TCK minimum clock period, Bypass Mode | 50 | - | ns |
| $T_{MSS}$ | TMS setup time | 10 | - | ns |
| $T_{MSH}$ | TMS hold time | 25 | - | ns |
| $T_{DIS}$ | TDI setup time | 10 | - | ns |
| $T_{DIH}$ | TDI hold time | 25 | - | ns |
| $T_{DOV}$ | TDO valid delay | - | 25 | ns |

## Connecting Configuration PROMs

Connecting the FPGA device with the configuration PROM (see Figure 6).

- The DATA output(s) of the PROM(s) drives the $D_{IN}$ input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s) (in Master Serial mode only).
- The $\overline{\text{CEO}}$ output of a PROM drives the $\overline{\text{CE}}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{\text{RESET}}$ input of all PROMs is best driven by the $\overline{\text{INIT}}$ output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a $V_{CC}$ glitch.
- The PROM $\overline{\text{CE}}$ input can be driven from the DONE pin. The $\overline{\text{CE}}$ input of the first (or only) PROM can be driven by the DONE output of the first FPGA device, provided that DONE is not permanently grounded. $\overline{\text{CE}}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.
- Slave-Parallel/SelectMap mode is similar to slave serial mode. The DATA is clocked out of the PROM one byte per CCLK instead of one bit per CCLK cycle. See FPGA data sheets for special configuration requirements.

### Initiating FPGA Configuration

The XC18V00 devices incorporate a pin named $\overline{CF}$ that is controllable through the JTAG CONFIG instruction. Executing the CONFIG instruction through JTAG pulses the $\overline{CF}$ low for 300-500 ns, which resets the FPGA and initiates configuration.

The $\overline{CF}$ pin must be connected to the $\overline{PROGRAM}$ pin on the FPGA(s) to use this feature.

The JTAG Programmer software can also issue a JTAG CONFIG command to initiate FPGA configuration through the “Load FPGA” setting.

### Selecting Configuration Modes

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the “Parallel mode” setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

## Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. Xilinx PROMs are designed to accommodate the Master Serial mode.

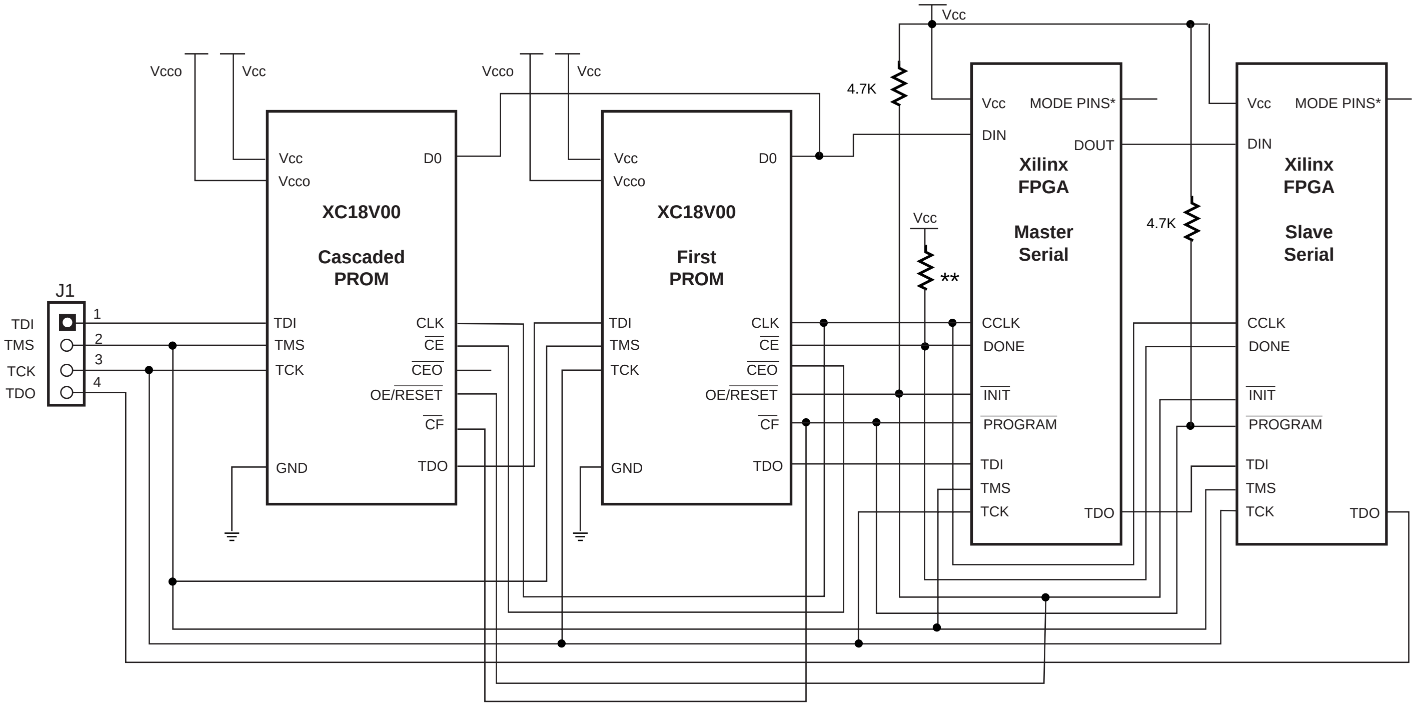
Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated by the FPGA during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK. If the user-programmable, dual-function $D_{IN}$ pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip pull-up resistor.

### Cascading Configuration PROMs

For multiple FPGAs configured as a serial daisy-chain, or a single FPGA requiring larger configuration memories in a serial or SelectMAP configuration mode, cascaded PROMs provide additional memory (Figure 5). Multiple XC18V00 devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the downstream device. The clock inputs and the data outputs of all XC18V00 devices in the chain are interconnected. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and drives its DATA line to a high-impedance state. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 6.

After configuration is complete, address counters of all cascaded PROMs are reset if the PROM OE/$\overline{RESET}$ pin goes Low.



* For Mode pin connections, refer to appropriate FPGA data sheet.
** Virtex, Virtex-E, Virtex-II, and Virtex-II Pro are 300 ohms, all others are 4.7K.

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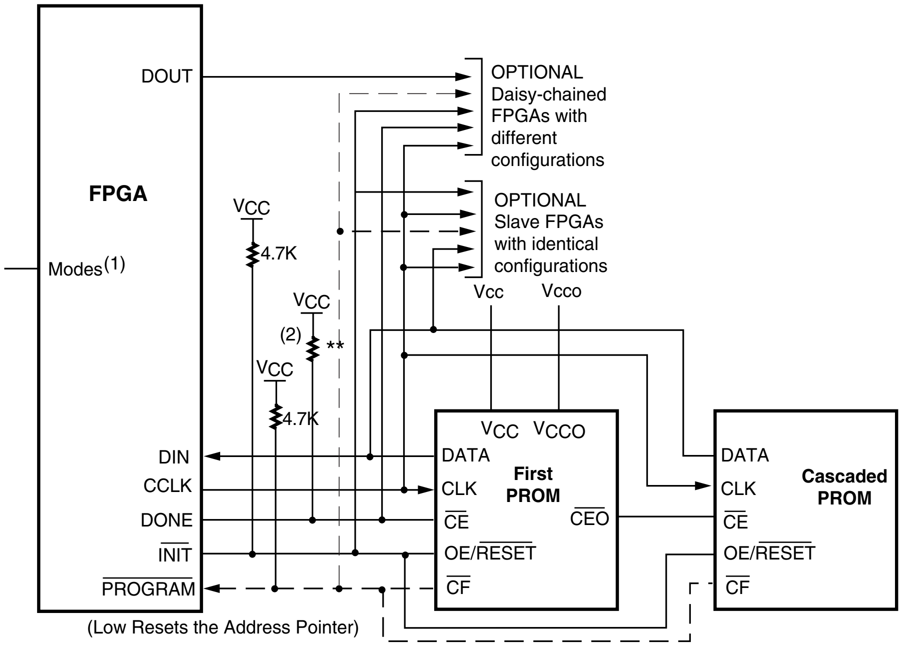
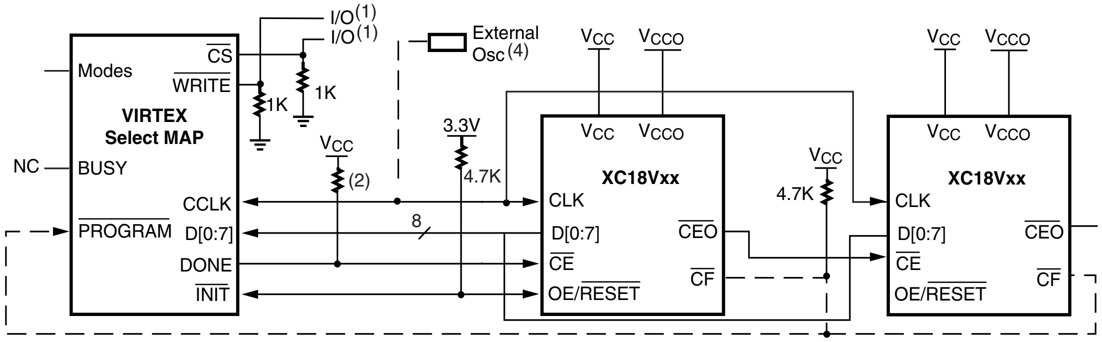
*Figure 5:* **JTAG Chain for Configuring Devices in Master Serial Mode**



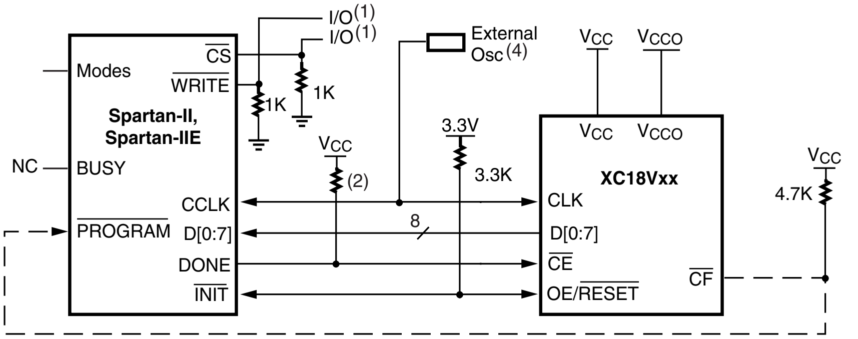
(1) For Mode pin connections, refer to the appropriate FPGA data sheet.
(2) Virtex, Virtex-E, and Virtex-II are 300 ohms.

**Master Serial Mode**



(1) CS and WRITE must be pulled down to be used as I/O. One option is shown.
(2) Virtex, Virtex-E, Virtex-II, and Virtex-II Pro are 300 ohms, all others are 4.7K.
(3) For Mode pin connections, refer to the appropriate FPGA data sheet.
(4) External oscillator required for Virtex/Virtex-E SelectMAP or Virtex-II/Virtex-II Pro Slave-SelectMAP modes.

**Virtex/Virtex-E/Virtex-II/Virtex-II Pro SelectMAP Mode**



(1) CS and WRITE must be pulled down to be used as I/O. One option is shown.
(2) If Drive Done configuration option is not active for any of the FPGAs, pull up DONE with a 3.3-kΩ resistor.
(3) For Mode pin connections, refer to the appropriate FPGA data sheet.
(4) External oscillator required for Spartan-II/Spartan-IIE Slave-Parallel modes.

**Spartan-II/Spartan-IIE Slave-Parallel Mode**

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*Figure 6:* **(a) Master Serial Mode (b) Virtex™/Virtex-E/Virtex-II/Virtex-II Pro™ SelectMAP Mode (c) Spartan-II/Spartan-IIE Slave-Parallel Mode** (dotted lines indicate optional connection)

## 5V Tolerant I/Os

The I/Os on each re-programmable PROM are fully 5V tolerant even through the core power supply is 3.3V. This allows 5V CMOS signals to connect directly to the PROM inputs without damage. In addition, the 3.3V $V_{CC}$ power supply can be applied before or after 5V signals are applied to the I/Os. In mixed 5V/3.3V/2.5V systems, the user pins, the core power supply ($V_{CC}$), and the output power supply ($V_{CCO}$) can have power applied in any order. This makes the PROM devices immune to power supply sequencing issues.

## Reset Activation

On power up, OE/$\overline{\text{RESET}}$ is held low until the XC18V00 is active (1 ms) and able to supply data after receiving a CCLK pulse from the FPGA. OE/$\overline{\text{RESET}}$ is connected to an external resistor to pull OE/$\overline{\text{RESET}}$ HIGH releasing the FPGA $\overline{\text{INIT}}$ and allowing configuration to begin. OE/$\overline{\text{RESET}}$ is held low until the XC18V00 voltage reaches the operating voltage range. If the power drops below 2.0V, the PROM resets. OE/$\overline{\text{RESET}}$ polarity is NOT programmable.

## Standby Mode

The PROM enters a low-power standby mode whenever $\overline{\text{CE}}$ is asserted High. The output remains in a high-impedance state regardless of the state of the OE input. JTAG pins TMS, TDI and TDO can be in a high-impedance state or High.

## Customer Control Pins

The XC18V00 PROMs have various control bits accessible by the customer. These can be set after the array has been programmed using “Skip User Array” in Xilinx JTAG Programmer Software.

*Table 7:* **Truth Table for PROM Control Inputs**

| Control Inputs | | Internal Address | Outputs | | |
|---|---|---|---|---|---|
| **OE/RESET** | **CE** | | **DATA** | **CEO** | **$I_{CC}$** |
| High | Low | If address $\leq$ TC(1): increment<br>If address > TC(1): don’t change | Active<br>High-Z | High<br>Low | Active<br>Reduced |
| Low | Low | Held reset | High-Z | High | Active |
| High | High | Held reset | High-Z | High | Standby |
| Low | High | Held reset | High-Z | High | Standby |

**Notes:**

1. TC = Terminal Count = highest address value. TC + 1 = address 0.

## Absolute Maximum Ratings(1,2)

| Symbol | Description | Value | Units |
|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to GND | –0.5 to +4.0 | V |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 to +5.5 | V |
| $V_{TS}$ | Voltage applied to High-Z output | –0.5 to +5.5 | V |
| $T_{STG}$ | Storage temperature (ambient) | –65 to +150 | °C |
| $T_{SOL}$ | Maximum soldering temperature (10s @ 1/16 in.) | +260 | °C |
| $T_J$ | Junction temperature | +150 | °C |

**Notes:**

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins can undershoot to –2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal voltage supply ($T_A$ = 0°C to +70°C) | Commercial | 3.0 | 3.6 | V |
| | Internal voltage supply ($T_A$ = –40°C to +85°C) | Industrial | 3.0 | 3.6 | V |
| $V_{CCO}$ | Supply voltage for output drivers for 3.3V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers for 2.5V operation | | 2.3 | 2.7 | V |
| $V_{IL}$ | Low-level input voltage | | 0 | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCO}$ | V |
| $T_{VCC}$ | $V_{CC}$ rise time from 0V to nominal voltage(1) | | 1 | 50 | ms |

**Notes:**

1. At power up, the device requires the $V_{CC}$ power supply to monotonically rise from 0V to nominal voltage within the specified $V_{CC}$ rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly.

## Quality and Reliability Characteristics

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DR}$ | Data retention | 20 | - | Years |
| $N_{PE}$ | Program/erase cycles (Endurance) | 20,000 | - | Cycles |
| $V_{ESD}$ | Electrostatic discharge (ESD) | 2,000 | - | Volts |

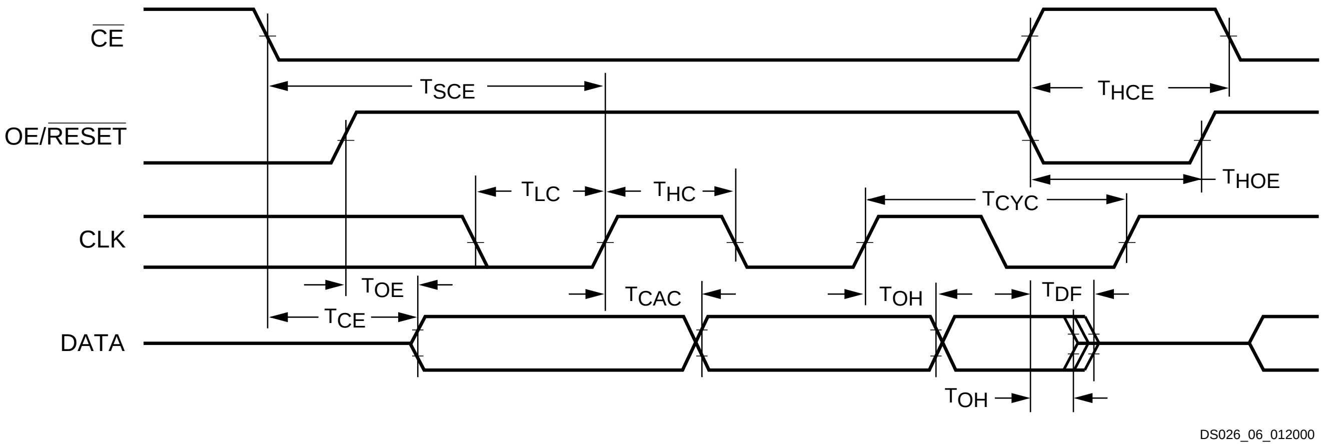
## DC Characteristics Over Operating Conditions

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage for 3.3V outputs | $I_{OH}$ = –4 mA | 2.4 | - | V |
| | High-level output voltage for 2.5V outputs | $I_{OH}$ = –500 µA | 90% $V_{CCO}$ | - | V |
| $V_{OL}$ | Low-level output voltage for 3.3V outputs | $I_{OL}$ = 8 mA | - | 0.4 | V |
| | Low-level output voltage for 2.5V outputs | $I_{OL}$ = 500 µA | - | 0.4 | V |
| $I_{CC}$ | Supply current, active mode | 25 MHz | - | 25 | mA |
| $I_{CCS}$ | Supply current, standby mode | | - | 10 | mA |
| $I_{ILJ}$ | JTAG pins TMS, TDI, and TDO | $V_{CC =}$ MAX<br>$V_{IN}$ = GND | –100 | - | µA |
| $I_{IL}$ | Input leakage current | $V_{CC}$ = Max<br>$V_{IN}$ = GND or $V_{CC}$ | –10 | 10 | µA |
| $I_{IH}$ | Input and output High-Z leakage current | $V_{CC}$ = Max<br>$V_{IN}$ = GND or $V_{CC}$ | –10 | 10 | µA |
| $C_{IN}$ and $C_{OUT}$ | Input and output capacitance | $V_{IN}$ = GND<br>f = 1.0 MHz | - | 10 | pF |

**Notes:**

1. 18V01/18V512/18V256 only, cascadable.
2. 18V01/18V512/18V256 only, non-cascadable, no brown-out protection.

## AC Characteristics Over Operating Conditions for XC18V04 and XC18V02

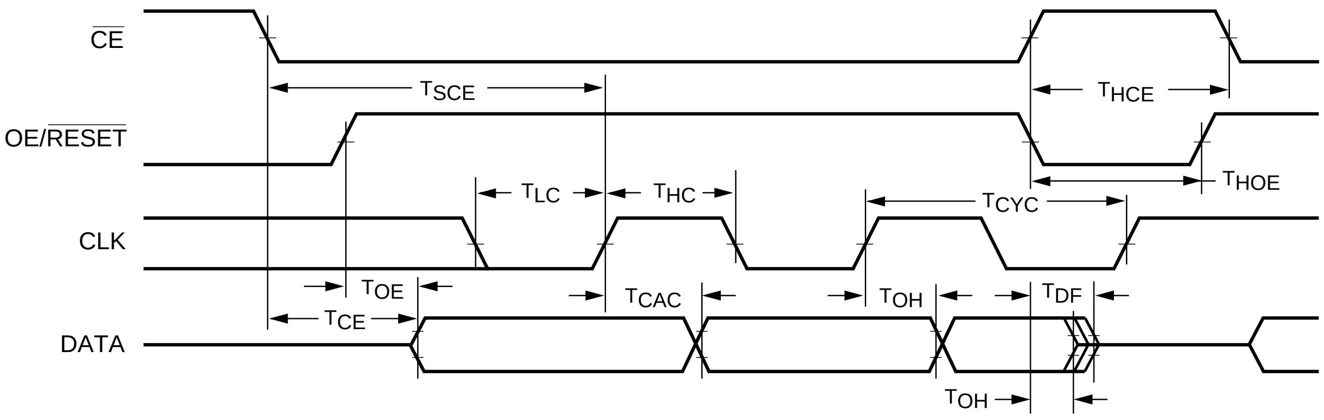


| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{OE}$ | OE/$\overline{\text{RESET}}$ to data delay | - | 10 | ns |
| $T_{CE}$ | $\overline{\text{CE}}$ to data delay | - | 20 | ns |
| $T_{CAC}$ | CLK to data delay | - | 20 | ns |
| $T_{OH}$ | Data hold from $\overline{\text{CE}}$, OE/$\overline{\text{RESET}}$, or CLK | 0 | - | ns |
| $T_{DF}$ | $\overline{\text{CE}}$ or OE/$\overline{\text{RESET}}$ to data float delay(2) | - | 25 | ns |
| $T_{CYC}$ | Clock periods | 50 | - | ns |
| $T_{LC}$ | CLK Low time(3) | 10 | - | ns |
| $T_{HC}$ | CLK High time(3) | 10 | - | ns |
| $T_{SCE}$ | $\overline{\text{CE}}$ setup time to CLK (to guarantee proper counting)(3) | 25 | - | ns |
| $T_{HCE}$ | $\overline{\text{CE}}$ High time (to guarantee proper counting) | 2 | - | µs |
| $T_{HOE}$ | OE/$\overline{\text{RESET}}$ hold time (guarantees counters are reset) | 25 | - | ns |

**Notes:**

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with $V_{IL} = 0.0V$ and $V_{IH} = 3.0V$.
5. If $T_{HCE}$ High < 2 µs, $T_{CE}$ = 2 µs.

## AC Characteristics Over Operating Conditions for XC18V01, XC18V512, and XC18V256



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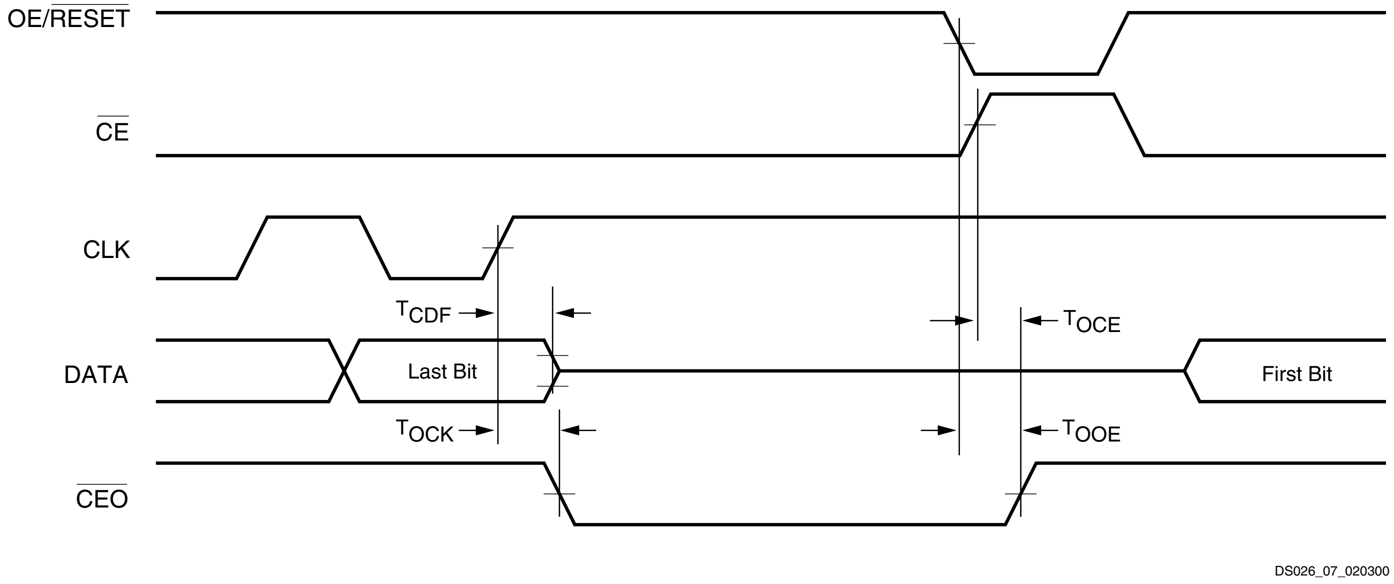
| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{OE}$ | OE/$\overline{RESET}$ to data delay | - | 10 | ns |
| $T_{CE}$ | $\overline{CE}$ to data delay | - | 15 | ns |
| $T_{CAC}$ | CLK to data delay | - | 15 | ns |
| $T_{OH}$ | Data hold from $\overline{CE}$, OE/$\overline{RESET}$, or CLK | 0 | - | ns |
| $T_{DF}$ | $\overline{CE}$ or OE/$\overline{RESET}$ to data float delay$^{(2)}$ | - | 25 | ns |
| $T_{CYC}$ | Clock periods | 30 | - | ns |
| $T_{LC}$ | CLK Low time$^{(3)}$ | 10 | - | ns |
| $T_{HC}$ | CLK High time$^{(3)}$ | 10 | - | ns |
| $T_{SCE}$ | $\overline{CE}$ setup time to CLK (to guarantee proper counting)$^{(3)}$ | 20 | - | ns |
| $T_{HCE}$ | $\overline{CE}$ hold time to CLK (to guarantee proper counting) | 2 | - | µs |
| $T_{HOE}$ | OE/$\overline{RESET}$ hold time (guarantees counters are reset) | 20 | - | ns |

**Notes:**

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with $V_{IL}$ = 0.0V and $V_{IH}$ = 3.0V.
5. If $T_{HCE}$ High < 2 µs, $T_{CE}$ = 2 µs.

# AC Characteristics Over Operating Conditions When Cascading for XC18V04 and XC18V02

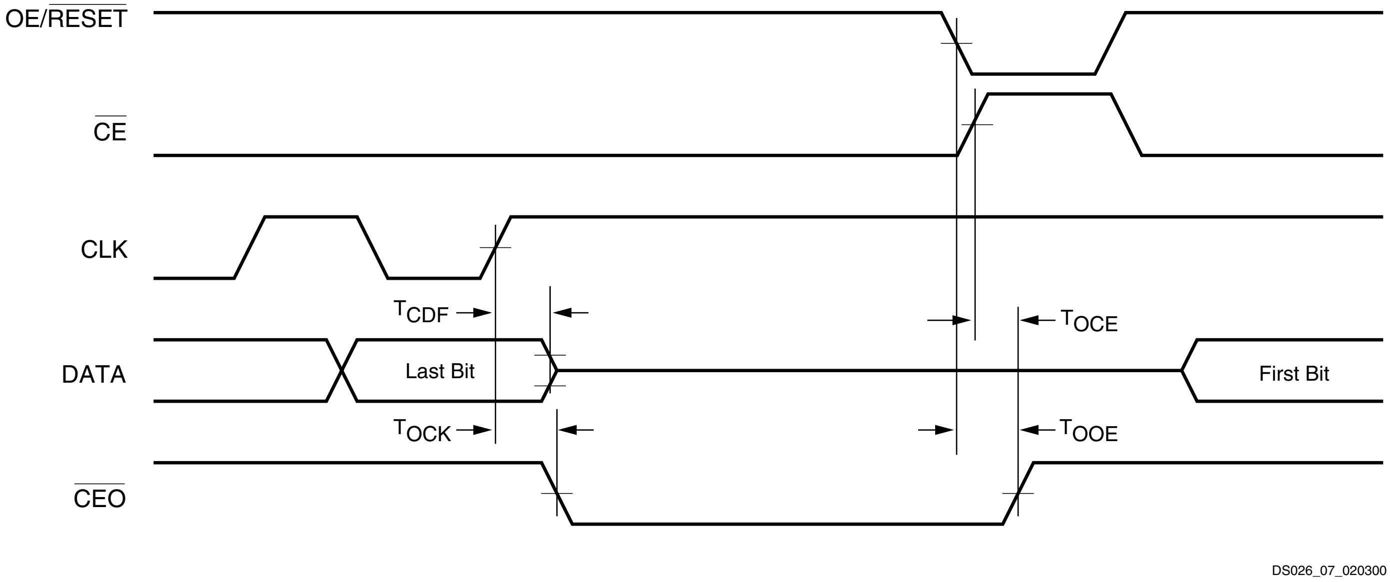


| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{CDF}$ | CLK to data float delay(2,3) | - | 25 | ns |
| $T_{OCK}$ | CLK to $\overline{CEO}$ delay(3) | - | 20 | ns |
| $T_{OCE}$ | CE to $\overline{CEO}$ delay(3) | - | 20 | ns |
| $T_{OOE}$ | OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) | - | 20 | ns |

**Notes:**

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with $V_{IL}$ = 0.0V and $V_{IH}$ = 3.0V.

## AC Characteristics Over Operating Conditions When Cascading for XC18V01, XC18V512, and XC18V256



| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{CDF}$ | CLK to data float delay$^{(2,3)}$ | - | 25 | ns |
| $T_{OCK}$ | CLK to $\overline{\text{CEO}}$ delay$^{(3)}$ | - | 20 | ns |
| $T_{OCE}$ | CE to $\overline{\text{CEO}}$ delay$^{(3)}$ | - | 20 | ns |
| $T_{OOE}$ | OE/$\overline{\text{RESET}}$ to $\overline{\text{CEO}}$ delay$^{(3)}$ | - | 20 | ns |

**Notes:**

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with $V_{IL}$ = 0.0V and $V_{IH}$ = 3.0V.

## Ordering Information

**XC18V04 VQ44 C**

**Device Number**

XC18V04
XC18V02
XC18V01
XC18V512
XC18V256

**Package Type**

VQ44 = 44-pin Plastic Quad Flat Package
PC44 = 44-pin Plastic Chip Carrier(1)
SO20 = 20-pin Small-Outline Package(2)
PC20 = 20-pin Plastic Leaded Chip Carrier(2)

**Operating Range/Processing**

C = Commercial ($T_A$ = 0° to +70°C)
I = Industrial ($T_A$ = –40° to +85°C)

**Notes:**

1. XC18V04 and XC18V02 only.
2. XC18V01, XC18V512, and XC18V256 only.

## Valid Ordering Combinations

| | | | | |
|---|---|---|---|---|
| XC18V04VQ44C | XC18V02VQ44C | XC18V01VQ44C | XC18V512VQ44C | XC18V256VQ44C |
| XC18V04PC44C | XC18V02PC44C | XC18V01PC20C | XC18V512PC20C | XC18V256PC20C |
| | | XC18V01SO20C | XC18V512SO20C | XC18V256SO20C |
| XC18V04VQ44I | XC18V02VQ44I | XC18V01VQ44I | XC18V512VQ44I | XC18V256VQ44I |
| XC18V04PC44I | XC18V02PC44I | XC18V01PC20I | XC18V512PC20I | XC18V256PC20I |
| | | XC18V01SO20I | XC18V512SO20I | XC18V256SO20I |

## Marking Information

### 44-pin Package

**XC18V04 VQ44 C**

**Device Number**

XC18V04
XC18V02
XC18V01
XC18V512
XC18V256

**Package Type**

VQ44 = 44-pin Plastic Quad Flat Package
PC44 = 44-pin Plastic Leaded Chip Carrier(1)

**Operating Range/Processing**

C = Commercial ($T_A$ = 0° to +70°C)
I = Industrial ($T_A$ = –40° to +85°C)

**Notes:**

1. XC18V02 and XC18V04 Only.

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### 20-pin Package(1)

Due to the small size of the commercial serial PROM packages, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows:

**18V01 S C**

**Device Number**

18V01
18V512
18V256

**Package Type**

S20 = 20-pin Small-Outline Package
J20 = 20-pin Plastic Leaded Chip Carrier

**Operating Range/Processing**

C = Commercial ($T_A$ = 0° to +70°C)
I = Industrial ($T_A$ = –40° to +85°C)

**Notes:**

1. XC18V01, XC18V512, and XC18V256 only.

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 2/9/99 | 1.0 | First publication of this early access specification |
| 8/23/99 | 1.1 | Edited text, changed marking, added $\overline{CF}$ and parallel load |
| 9/1/99 | 1.2 | Corrected JTAG order, Security and Endurance data. |
| 9/16/99 | 1.3 | Corrected SelectMAP diagram, control inputs, reset polarity. Added JTAG and $\overline{CF}$ description, 256 Kbit and 128 Kbit devices. |
| 01/20/00 | 2.0 | Added Q44 Package, changed XC18xx to XC18Vxx |
| 02/18/00 | 2.1 | Updated JTAG configuration, AC and DC characteristics |
| 04/04/00 | 2.2 | Removed stand alone resistor on INIT pin in Figure 5. Added Virtex-E and EM parts to FPGA table. |
| 06/29/00 | 2.3 | Removed XC18V128 and updated format. Added AC characteristics for XC18V01, XC18V512, and XC18V256 densities. |
| 11/13/00 | 2.4 | Features: changed 264 MHz to 264 Mb/s at 33 MHz; AC Spec.: $T_{SCE}$ units to ns, $T_{HCE}$ CE High time units to µs. Removed Standby Mode statement: “The lower power standby modes available on some XC18V00 devices are set by the user in the programming software”. Changed 10,000 cycles endurance to 20,000 cycles. |
| 01/15/01 | 2.5 | Updated Figures 5 and 6, added 4.7 resistors. Identification registers: changes ISP PROM product ID from 06h to 26h. |
| 04/04/01 | 2.6 | Updated Figure 6, Virtex SelectMAP mode; added XC2V products to Compatible PROM table; changed Endurance from 10,000 cycles, 10 years to 20,000, 20 years; |
| 04/30/01 | 2.7 | Updated Figure 6: removed Virtex-E in Note 2, fixed SelectMAP mode connections. Under **AC Characteristics Over Operating Conditions for XC18V04 and XC18V02**, changed $T_{SCE}$ from 25 ms to 25 ns. |
| 06/11/01 | 2.8 | **AC Characteristics Over Operating Conditions for XC18V01, XC18V512, and XC18V256** Changed Min values for $T_{SCE}$ from 20 ms to 20 ns and for $T_{HCE}$ from 2 ms to 2 µs. |
| 09/28/01 | 2.9 | Changed the boundary scan order for the CEO pin in Table 1, updated the configuration bits values in the table under **Xilinx FPGAs and Compatible PROMs**, and added information to the **Recommended Operating Conditions** table. |
| 11/12/01 | 3.0 | Updated for Spartan-IIE FPGA family. |
| 12/06/01 | 3.1 | Changed Figure 6(c). |
| 02/27/02 | 3.2 | Updated Table 2 and Table 6 for the Virtex-II Pro family of devices. |