CS5361

Battery Charger Buck Controller

The CS5361 is a high voltage step down controller that provides a simple way to build a battery charger suited for various types of batteries. With an operating range of up to 30 V, it can be used to charge a multiple number of cells from a DC voltage, as is supplied by high AC–DC adapter voltages. Proprietary I^2 architecture ensures full control over both Average and Peak charging currents. Independent voltage loop allows for precision regulation of the battery voltage. Average current outer control loop provides tight regulation and easy loop compensation while pulse by pulse inner control provides for fast response.

The CS5361 is designed to provide a high performance, full–featured battery charger that is simple to use. A 4.2 V reference with 0.8% tolerance can be used to implement 1.0% accurate output voltages. It also features an additional pulse–by–pulse current limit input to allow for fast output current control.

The CS5361 operates over a 7.0 V to 30 V range and is available in a 16 lead surface mount narrow body.

Features

- Switching Regulator Controller
  - Synchronous Buck Regulator Topology for High Efficiency
  - Top Side P–Channel Allows High Input Voltage and Requires No Charge Pump
  - Pulse–by–Pulse Inner Control Loop for Fast Response
  - Programmable Peak Current Limit
  - True Current Soft Start
  - Clamped Gate–to–Source Voltage
- Oscillator
  - Constant Frequency Design
  - 100 kHz to 500 kHz Adjustable Frequency
- System Power Management
  - Programmable UVLO
  - 2.0 μA Sleep Mode Current (Typical)
  - Bias Mode Uses Top Switch to Connect Battery to Load
  - 4.2 V ± 0.8% Reference Output
  - Thermal Shutdown

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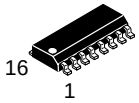
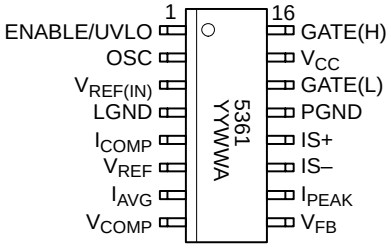


SO–16
D SUFFIX
CASE 751B

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS5361GD16	SO–16	48 Units/Rail
CS5361GDR16	SO–16	2500 Tape & Reel

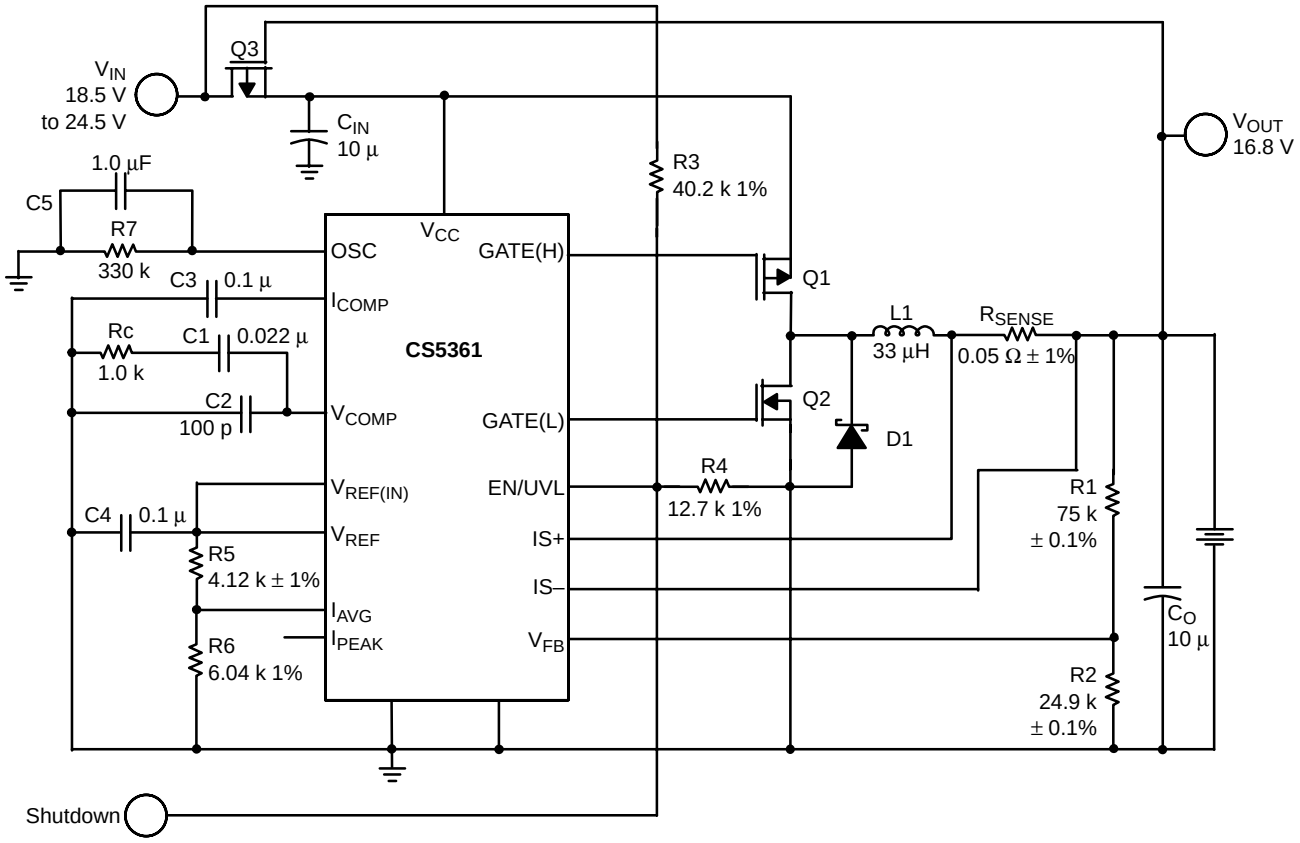


Figure 1. Application Diagram, 16.8 V/2.0 A Four Cell Lithium–Ion Battery Charger with High Side Current Sensing

MAXIMUM RATINGS*

Rating		Value	Unit
Operating Junction Temperature		150	°C
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak	°C
Storage Temperature Range		–65 to +150	°C
Package Thermal Resistance: Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$		 28 115	 °C/W °C/W
ESD Susceptibility (Human Body Model)		2.0	kV

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{CC}	30 V	–0.3 V	N/A	2.0 A Peak 50 mA DC
Positive Current Sense Input	IS+	30 V	–0.3 V	1.0 mA	1.0 mA
Negative Current Sense Input	IS–	30 V	–0.3 V	1.0 mA	1.0 mA
Shutdown and UVLO Input	Enable/UVLO	6.0 V	–0.3 V	1.0 mA	10 mA
Average Current Loop Set Point	I_{AVG}	6.0 V	–0.3 V	1.0 mA	1.0 mA
Peak Current Loop Set Point	I_{PEAK}	6.0 V	–0.3 V	1.0 mA	1.0 mA
Voltage Feedback Input	V_{FB}	6.0 V	–0.3 V	1.0 mA	1.0 mA
Reference Voltage Input	$V_{REF(IN)}$	6.0 V	–0.3 V	1.0 mA	1.0 mA
Voltage Loop Compensation Pin	V_{COMP}	6.0 V	–0.3 V	1.0 mA	1.0 mA
High–Side FET Driver	GATE(H)	30 V	–0.3 V –2.0 V for 50 ns	2.0 A Peak 200 mA DC	2.0 A Peak 200 mA DC
Low–Side FET Driver	GATE(L)	15 V	–0.3 V –2.0 V for 50 ns	2.0 A Peak 200 mA DC	2.0 A Peak 200 mA DC
Current Loop Compensation Pin	I_{COMP}	6.0 V	–0.3 V	1.0 mA	1.0 mA
Power Ground	PGND	0 V	0 V	2.0 A Peak 200 mA DC	N/A
Logic Ground	LGND	0 V	0 V	200 mA DC	N/A
Reference Voltage Output	V_{REF}	6.0 V	–0.3 V	50 mA	50 mA
Oscillator Pin	OSC	6.0 V	–0.3 V	10 mA	10 mA

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $0°C < T_J < 115°C$; $7.0\ V < V_{CC} < 30\ V$; $C_{GATE(H)} = C_{GATE(L)} = 1.0\ nF$, $C_{REF} = 0.1\ \mu F$, $CV_{CC} = 0.1\ \mu F$, $C_{ICOMP} = 0.1\ \mu F$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Voltage Error Amplifier					
V_{FB} Bias Current	$V_{FB} = 0\ V$	–	0.1	0.27	μA
V_{COMP} Source Current	$V_{COMP} = 0.5\ V$ to $3.3\ V$; $V_{FB} = 0.9\ V$	68	100	170	μA
V_{COMP} Sink Current	$V_{COMP} = 0.5\ V$ to $3.3\ V$; $V_{FB} = 1.1\ V$	60	100	160	μA
Open Loop DC Gain	Note 2	60	80	100	dB
Transconductance (Gm)	–	0.6	1.2	2.1	mA/V
Output Impedance	Note 2	1.4	8.3	47.6	MΩ
PSRR @ 1.0 kHz	Note 2	60	85	–	dB
CMRR @ 1.0 kHz	Note 2	80	110	–	dB
Input Voltage Offset	1.0 V to 5.0 V	–5.0	–	6.5	mV
V_{COMP} Max Voltage	$V_{REF(IN)} = 3.3\ V$, $V_{FB} = 3.2\ V$	3.9	5.0	6.5	V
V_{COMP} Min Voltage	$V_{REF(IN)} = 3.3\ V$, $V_{FB} = 3.4\ V$	–	0.1	0.2	V
GATE(H) and GATE(L)					
High Voltage (AC)	Note 2	$V_{CC} – 0.5$	V_{CC}	–	V
Low Voltage (AC)	Note 2	–	0	0.5	V
Rise Time	For $V_{CC} > 10\ V$: Note 2 $1.0\ V < GATE(L) < 3.0\ V$, $V_{CC} – 8.0\ V < GATE(H) < V_{CC} – 1.0\ V$; For $7.0\ V < V_{CC} < 10\ V$: $1.0\ V < GATE(L) < V_{CC} – 1.0\ V$, $1.0\ V < GATE(H) < V_{CC}\ 1.0\ V$	–	40	80	ns
Fall Time	For $V_{CC} > 10\ V$: Note 2 $3.0\ V > GATE(L) > 1.0\ V$, $V_{CC} – 1.0\ V > GATE(H) < V_{CC} – 8.0\ V$; For $7.0\ V < V_{CC} < 10\ V$: $V_{CC} – 1.0\ V > GATE(L) < 1.0\ V$, $V_{CC} – 1.0\ V > GATE(H) > 1.0\ V$	–	40	80	ns
GATE(H) to GATE(L) Delay	$V_{CC} – GATE(H) < 2.0\ V$, $GATE(L) > 2.0\ V$ Note 2	40	80	110	ns
GATE(L) to GATE(H) Delay	$GATE(L) < 2.0\ V$, $V_{CC} – GATE(H) > 2.0\ V$ Note 2	15	60	80	ns
GATE(L) Clamp to GND	–	4.0	5.0	6.0	V
GATE(H) Clamp to V_{CC}	–	–15	–12	–10	V
GATE(H) Sleep Clamp	$I_{GATE(H)} = 100\ \mu A$	–	$V_{CC} – 0.7$	$V_{CC} – 1.0$	V
GATE(L) Resistance to GND	–	20	50	100	kΩ
GATE(H) Bias Clamp	$I_{GATE(H)} = 10\ \mu A$ to GND in Bias mode	13	16	20	V
GATE(H) Bias Current	$GATE(H) = V_{CC} – 5.0\ V$	3.0	10	20	μA

2. Guaranteed by design, not 100% production tested.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 115°C$; $7.0\ V < V_{CC} < 30\ V$; $C_{GATE(H)} = C_{GATE(L)} = 1.0\ nF$, $C_{REF} = 0.1\ \mu F$, $CV_{CC} = 0.1\ \mu F$, $C_{ICOMP} = 0.1\ \mu F$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Oscillator					
Switching Frequency	960 kΩ from OSC to GND	80	100	120	kHz
Switching Frequency	330 kΩ from OSC to GND	240	300	360	kHz
Switching Frequency	185 kΩ from OSC to GND	420	500	635	kHz
Bias Threshold Positive	–	2.5	2.75	3.0	V
Bias Threshold Negative	–	2.25	2.5	2.75	V
Bias Threshold Hysteresis	–	150	250	350	mV
Bias Input Current	OSC = 5.0 V	–	–	1.0	μA
Average Current Error Amplifier					
I_{AVG} Bias Current	I_{AVG} = 0 V	–	0.2	1.0	μA
I_{COMP} Source Current	I_{COMP} = 0.5 V to 3.3 V	18	25	32	μA
I_{COMP} Sink Current	I_{COMP} = 0.5 V to 3.3 V	18	25	32	μA
Set Point	I_{AVG} = 0.25V, 7.0 V < V_{CC} < 24 V I_{AVG} = 2.5 V, 7.0 V < V_{CC} < 24 V	2.0 90	10 100	16.5 110	mV mV
Open Loop DC Gain	Note 3	60	80	100	dB
Transconductance (Gm)	Note 3	0.2	0.3	0.7	mA/V
Output Impedance	Note 3	5.0	33	143	MΩ
PSRR @ 1.0 kHz	Note 3	60	80	–	dB
I_{COMP} Max Voltage	$V_{I(AVG)}$ = 3.3 V, IS+ = IS– = 0V	3.9	5.0	6.5	V
I_{COMP} Min Voltage	$V_{I(AVG)}$ = 0 V, IS+ = 0.2 V, IS– = 0 V	–	0.1	0.2	V
Current Sense Amplifier					
IS+, IS– Bias Current	IS– = IS+ = 0 V to V_{CC} (20 V max)	–5.0	1.0	5.0	μA
Input Offset	IS– = 0 to V_{CC}	–8.0	–	7.0	mV
DC Gain	IS– = 1.0 V to V_{CC}	23	25	27	V/V
Gain Bandwidth (–3.0 dB)	Note 3	3.5	5.5	–	MHz
Propagation Delay	Note 3	–	70	105	ns
PSRR @ 1.0 kHz	Note 3	60	85	–	dB
CMRR @ 1.0 kHz	Note 3	80	100	–	dB
Input Common Mode Range	–	0	–	V_{CC}	V
Input Differential Mode Range	Note 3	0	–	125	mV
Peak Current Comparator					
Set Point	I_{PEAK} = 3.0 V, Duty Cycle = 50%	90	100	110	mV
I_{PEAK} Bias Current	I_{PEAK} = 0 V	–	0.3	1.0	μA

3. Guaranteed by design, not 100% production tested.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 115°C$; $7.0\ V < V_{CC} < 30\ V$; $C_{GATE(H)} = C_{GATE(L)} = 1.0\ nF$, $C_{REF} = 0.1\ \mu F$, $CV_{CC} = 0.1\ \mu F$, $C_{ICOMP} = 0.1\ \mu F$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
PWM Comparator					
Transient Response	Note 4	–	50	–	ns
I_{COMP} Input Resistance	–	200	500	800	Ω
Slope Compensation	Note 4	0.8	1.0	1.2	V
Oscillator Duty Cycle	Note 4	85	90	95	%
Minimum Pulse Width	Note 4	–	150	200	ns
Enable/UVLO Management					
Enable Input Threshold	–	2.25	2.5	2.75	V
Input Resistance	Note 4	10	50	80	kΩ
Input Bias Current	$V_{ENABLE/UVLO} = 2.75\ V$	–	0.1	1.0	μA
Reference Output					
V_{REF} Output Voltage	$0\ mA < I_{V(REF)} < 1.0\ mA$	4.166	4.2	4.234	V
V_{REF} Short Circuit Current	$V_{REF} = 0V$	3.0	6.0	10	mA
Thermal Protection					
Over Temperature Trip Point	Note 4	125	150	175	°C
Thermal Shutdown Hysteresis	Note 4	–	25	–	°C
General Electrical Specifications					
V_{CC} Operating Current (Non–Switching)	$V_{COMP} = I_{COMP} = 0\ V$	–	17	30	mA
V_{CC} Sleep Current	ENABLE/UVLO = 0V; $7.0\ V < V_{CC} < 20\ V$; $T_A = 25°C$	–	2.0	5.0	μA
V_{CC} Bias Mode Current	ENABLE/UVLO = 0 V	–	50	75	μA

4. Guaranteed by design, not 100% production tested.

PACKAGE PIN DESCRIPTION

Package Pin # SO–16	Pin Symbol	Function
1	ENABLE/UVLO	Shutdown input. Connect to V_{IN} through a resistor divider to program minimum operating voltage. Pull below 2.5 V to shut down the IC.
2	OSC	Oscillator pin. Place resistor to GND to set the switching frequency. Enters bias mode when pulled above 2.75 V and the ENABLE/UVLO Input is low (PFET turned ON).
3	$V_{REF(IN)}$	Reference input of the voltage error amplifier. Connect to the built–in or external reference.
4	LGND	Logic Ground. IC Substrate Connection.
5	I_{COMP}	Current feedback compensation network.
6	V_{REF}	4.2 V Reference output voltage. Capable of sourcing 3.0 mA.
7	I_{AVG}	Average current control loop input. Voltage at this pin sets average output current.
8	V_{COMP}	Voltage feedback compensation network.
9	V_{FB}	Voltage feedback pin. Connect a resistor divider between output and this pin to set output voltage.
10	I_{PEAK}	Peak current control loop input. This input is used to set peak value of the inductor ripple current. This pin can override average current loop setting. It can be used for fast current control.
11	IS–	Negative input of the current sense amplifier.
12	IS+	Positive input of the current sense amplifier.
13	PGND	Power Ground.
14	GATE(L)	Low–Side FET Driver. This pin is capable of delivering peak currents of 1.0 A.
15	V_{CC}	Input power supply pin or V_{CC} bias.
16	GATE(H)	High–Side FET Driver. This pin is capable of delivering peak currents of 1.0 A.

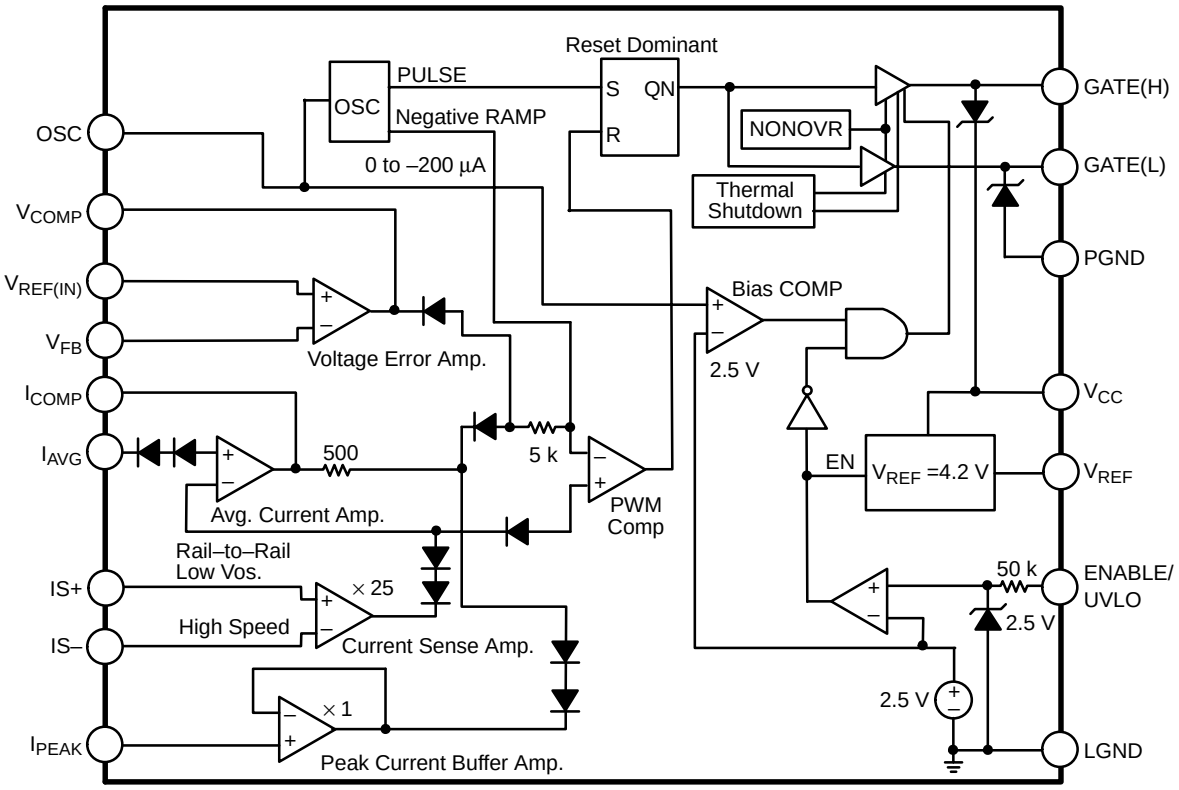


Figure 2. Block Diagram

APPLICATIONS INFORMATION

THEORY OF OPERATION

Overview

The CS5361 battery charger controller has been designed with the flexibility to charge several types of batteries, such as Lithium Ion, Nickel Cadmium, Nickel Metal Hydride and Lead Acid. The differences in chemistry between different battery types result in differing charge requirements.

Lithium Ion batteries are charged with a constant voltage, current limit supply. When the battery voltage is low, the charger operates in constant current mode. When the battery voltage reaches 4.2 V, the current begins to taper off and the charger enters into constant voltage mode until the current essentially reaches zero. Nickel Cadmium and Nickel Metal Hydride batteries can be charged with a constant current profile. Lead Acid batteries are charged with a constant voltage, current limiting supply or with a constant–current supply.

For a battery charger with the capability to charge all those battery types, at least two operation modes are required: constant current mode and constant voltage mode. Synchronous operation enables designs with greater than 94% efficiency to be realized.

Control Method

1. Current Control

I^2 control scheme is employed to regulate the charging current. The sense resistor senses the inductor current. A low offset, high speed Current Sense amplifier with rail–to–rail inputs amplifies the voltage across the sense resistor. The output of the amplifier (I_{SENSE}), which is proportional to the inductor current, is used as feedback for two control loops. The DC level is used by the outer loop and is fed to the Average Current Error Amplifier. The Error Amplifier compares I_{SENSE} to an externally set reference voltage I_{AVG} and generates a PWM control voltage I_{COMP}. Charger designers can use the I_{COMP} pin to design the compensation for the Average Current Amplifier. The current ripple is used as the ramp signal of the PWM comparator. I^2 control has inherent compensation for duty cycle in response to line voltage or load changes. Changes in line and load conditions affect the inductor current. Because the ramp signal of the PWM comparator is generated from the inductor current, the duty cycle can be adjusted on a pulse by pulse basis. Since the fast PWM control loop handles transient response, a high gain, low bandwidth error amplifier can be used to improve DC accuracy, stability and noise immunity.

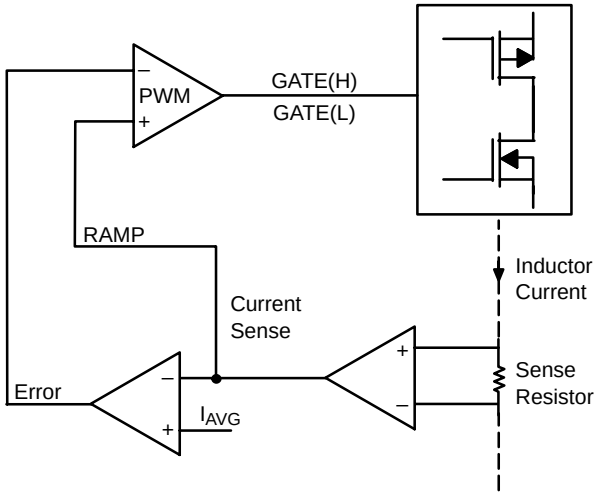


Figure 3. I^2 Control Scheme

2. Voltage Control

Current mode voltage control method is used to regulate the voltage. The V_{FB} pin monitors the battery voltage. A resistor divider is used to scale the voltage down to the reference level set at the $V_{REF(IN)}$ pin. CS5361 provides a 4.2 V ± 0.8%reference voltage which can obviate the need for a resistor network if charging a single 4.2 V cell. V_{FB} and $V_{REF(IN)}$ are the two inputs of the Voltage Error Amplifier. The output V_{COMP} is compared with the ramp signal, which is generated from the inductor current, to adjust the duty cycle. Similar to I_{COMP}, V_{COMP} provides user with compensation capability.

Start–Up

CS5361 provides a controlled startup of regulator output current and voltage through the Error Amplifiers and external compensation networks. The capacitor at the I_{COMP} output provides true current soft start. As the capacitor charges up, the Average Current Error Amplifier signal increases. The output current of the regulator ramps up in a controlled manner. The compensation network at V_{COMP} has the similar function, which will prevent instantaneous switching of the output voltage.

Oscillator

The battery charger controller is designed for constant frequency operation. The user can adjust the switching frequency from 100 kHz to 500 kHz by connecting a resistor from the OSC pin to GND. This function simplifies the

selection of external components and allows the user freedom to choose switching frequency.

Gate Drivers GATE(H) and GATE(L)

In synchronous buck operation, GATE(H) and GATE(L) drive the high–side P–channel MOSFET and the low–side N–channel MOSFET respectively. The advantage of this circuit is that no charge pump is required. The low–side FET (the synchronous rectifier) behaves like a diode but has a smaller voltage drop and improves the efficiency. A 60 ns nonoverlap dead time is added between the time when the high–side FET is turned off and when the synchronous rectifier is turned on, and vice versa. This function effectively prevents crowbar currents during switching transitions.

Gate Voltage Clamps

Internal clamps prevent driving the external power MOSFET gate voltages to levels higher than required for complete enhancement. This improves converter efficiency by reducing gate rise time, fall time, and the losses associated with the charge and discharge of gate capacitance.

Bias Mode

When the battery is fully charged, the charger can be shut down externally by pulling the ENABLE/UVLO pin low. When the part is off and the OSC pin is pulled above 2.75 V, the charger will enter into Bias Mode. In Bias mode, the high–side PFET turns on and connect the battery to the load so that the battery starts discharging to the load.

100% Duty Cycle

The maximum duty cycle of the CS5361 is 100%. This feature is useful when the input voltage is marginally higher than the output voltage. If the battery voltage is very close to the input line voltage, the controller will simply go to 100% duty cycle.

Slope Compensation

In both current and voltage controls, the sensed inductor current signal is used as the ramp of the PWM comparator to afford fast response to line and load variations. An artificial ramp signal with negative slope generated by the oscillator is added to the two negative inputs (V_{COMP} and I_{COMP}) of the PWM comparator to be compared with the ramp generated by the inductor current. The output of the PWM comparator is used to control the duty cycle. This method helps stabilize the system over the whole operation duty cycle range as well as minimize response time to output current changes.

Error Amplifier Compensation

The outputs of the Average Current Error Amplifier and the Voltage Error Amplifier are available to users. Users have the freedom to design the compensation network to improve the dynamic characteristics such as transient response time, over/undershoot, and loop stability.

Enable/Under–Voltage Lockout

The input voltage of the charger must remain above a certain level in order to work. Control is required to ensure that the charger will not start to operate without sufficient voltage. Under–Voltage Lockout provides this protection with a comparator, which compares the input to 2.5 V. The output of the comparator enables the charger's reference voltage, which in turn controls startup of the charger. The comparator's output also controls the high–side MOSFET so that the batteries will power the load when the charger is shut off. This pin also provides the function of manual shutdown by bringing the pin below 2.5 V. Chip current in the shutdown mode is only 2.0 μA.

Peak Current Control

The Peak Current Buffer Amplifier compares the current control signal (the output of the Average Current Error Amplifier) with a preset reference voltage, which can be set externally at pin I_{PEAK}. When output of the Error Amplifier exceeds the limit, the output of the Peak Current Buffer Amplifier goes low and clamps current control signal. Therefore, the peak current control can override the average current control. In laptop computer systems, fast reducing the charge current is required to prevent overloading the input supply when the computer switches into active mode from sleep mode. On the other hand, a trickle charging mode is required in many battery chargers either to prevent over–discharged or fully charged cells from being damaged by constant–current charging. The current for trickle charging is usually much lower than that of constant–current charging. The Peak Current Control can be utilized to implement trickle charging mode without changing the setting of the average charging current.

Input Current Limiting

An input current limiting function can be implemented externally using a dual op–amp, a sense resistor and several resistors and capacitors. The first op–amp is configured into a differential amplifier. The second op–amp compares the amplified input current signal with a reference voltage. The output is used to clamp the I_{COMP} pin voltage when input current exceeds the limit. See Figure 9 for detailed implementation.

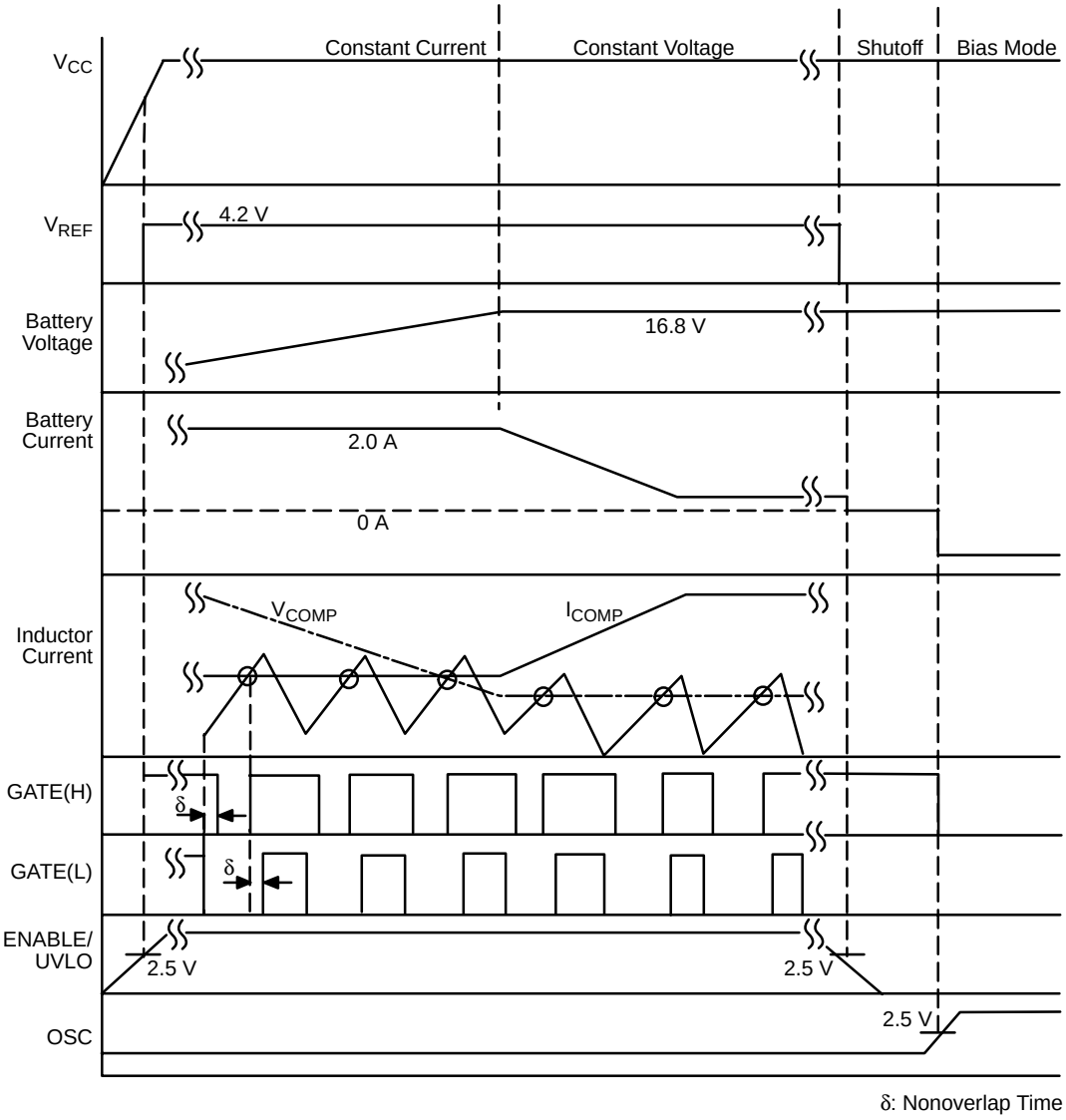


Figure 4. Key Operation Waveforms

DESIGN GUIDELINES

1. Selection of the Output Inductor

The value of the output inductor can be calculated based on the inductor ripple current requirement:

$$L = (1.0 - D) \times \frac{T_S V_{OUT}}{\Delta I_L} \quad (1)$$

where V_{OUT} is the output voltage; T_S is the period of one switching cycle; ΔI_L is the peak–to–peak inductor ripple current given by design specification; and D is the duty cycle. Because both duty cycle and the output voltage change during charging operation, the designer should determine the maximum product of (1.0 – D) and V_{OUT} to calculate the inductance. The peak inductor current is given by:

$$I_{L,PEAK} = I_O + \frac{\Delta I_L}{2.0} \quad (2)$$

The peak current should not saturate the core of the inductor.

2. Selection of Output Capacitor

Both the output voltage ripple and the inductor current ripple determine the value of the output capacitance. The required minimum is given by:

$$C = 0.125 \times \frac{\Delta I_L T_S}{\Delta V_{OUT}} \quad (3)$$

The capacitor ESR (Equivalent Series Resistance) of the capacitor also needs to be small enough to meet the ripple requirement.

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_L} \quad (4)$$

If the ESR obtained from the above equation is smaller than the ESR specified in the capacitor manufacturer's data

sheet; several capacitors should be paralleled. The number of capacitors is determined by:

$$\text{Number of Capacitors} = \frac{\text{ESR}_{\text{PER CAP}}}{\text{ESR}_{\text{MAX}}} \quad (5)$$

3. Design of Resistor Divider for Voltage Sensing

Because the internal reference voltage is 4.2 V, which is equal to the voltage of one Lithium Ion battery cell, we have:

$$\frac{R2}{R1 + R2} = \frac{1.0}{\text{Cell Count}}$$

The maximum input bias current of the Voltage Error Amplifier is 1.0 μA, the resistor divider current should be much higher than that to ensure that there is sufficient bias current. For 4–cell charger, the output voltage is 16.8 V. If we choose R1 + R2 = 100 kΩ, then

$$\frac{16.8\ \text{V}}{100\ \text{k}\Omega} = 168\ \mu\text{A} >> 1.0\ \mu\text{A}$$

Therefore,

$$R2 = \frac{100\ \text{k}\Omega}{\text{Cell Count}}, R1 = 100\ \text{k}\Omega - R2 \quad (6)$$

R1 and R2 must be ± 0.1% precise resistors to meet the ± 1.0% overall charge voltage accuracy.

4. Design of Resistor Divider for Enable/Under–Voltage Lockout

The resistor divider should be so designed that the controller can be enabled at the required minimum input voltage.

$$\frac{R4}{R3 + R4} = \frac{2.5\ \text{V}}{V_{\text{IN,MIN}}}$$

The maximum bias current for this pin is also 1.0 μA. The sum of R3 and R4 can also be chosen as 100 kΩ, so

$$R4 = \frac{100\ \text{k}\Omega \times 2.5\ \text{V}}{V_{\text{IN,MIN}}}, R3 = 100\ \text{k}\Omega - R4 \quad (7)$$

5. Selection of Current Sense Resistor and Resistor Divider for Current Setting

The tolerance of the current sense resistor affects the accuracy of current regulation, so a sense resistor with ± 1.0% tolerance should be used. Since the Current Sense Amplifier is a high–speed, low voltage rail–to–rail amplifier, the value of the current sensing resistor should satisfy the following condition:

$$I_{\text{PEAK}} \times R_{\text{SENSE}} \leq 125\ \text{mV}$$

where 125 mV is the differential mode input range of the Current Sense Amplifier.

Therefore,

$$R_{\text{SENSE}} \leq \frac{125\ \text{mV}}{I_{\text{PEAK}}} \quad (8)$$

After the value of current sense resistor is determined, the resistor divider for current setting can be designed.

$$\frac{R6}{R5 + R6} = I_{\text{OUT}} \times R_{\text{SENSE}} \times \frac{25}{4.2\ \text{V}}$$

where I_{OUT} is the target value of the output current.

The maximum bias current of the Current Error Amplifier is 1.0 mA. The voltage across the resistor divider is 4.2 V. If we choose R5 + R6 = 10 kΩ, we have

$$\frac{42}{10\ \text{k}\Omega} = 420\ \mu\text{A} >> 1.0\ \mu\text{A}$$

Therefore,

$$R6 = 10\ \text{k}\Omega \times 25 \times I_{\text{OUT}} \times \frac{R_{\text{SENSE}}}{4.2\ \text{V}}, \quad R5 = 10\ \text{k}\Omega - R6 \quad (9)$$

6. Design of Average Current Compensation Network

As mentioned before, there are two feedback loops in the I^2 control scheme. The slow outer loop provides tight regulation and easy loop compensation. The fast inner loop handles the transient response on a pulse–by–pulse basis. The design of the compensation network is based on the control–to–output transfer function with closed inner current feedback loop. In this case, "control" is the output of the Average Current Error Amplifier (I_{COMP}) and "output" is the inductor current.

The approximate control–to–output transfer function for the Buck converter is given by:

$$\frac{I_L}{I_{\text{COMP}}} \approx \frac{1.0 + sC \times (\text{ESR} + R)}{R_I(1.0 + sCR)[1.0 + s/(\omega_n Q) + s^2/\omega_n{}^2]} \quad (10)$$

where R_I is the current sense gain, ωn is half of the switching frequency and

$$Q = \frac{1.0}{\pi[(1.0 + Se/Sn) \times (1.0 - D) - 0.5]} \quad (11)$$

where Se is the slope of the external ramp signal and Sn is the inductor current up slope.

The transfer function is a third–order system with a double pole at half of the switching frequency and a low frequency pole. Because ESR of the output capacitor is usually very small compared to load resistor R, the zero and the low frequency pole can cancel out each other. The system degrades to second–order.

The compensation design for such a system becomes very easy. A single integrator pole gives the system high DC gain and makes it crossover with –1.0 slope. The Bode plot of the

closed loop control–to–output transfer function without and with compensation is shown in Figure 5.

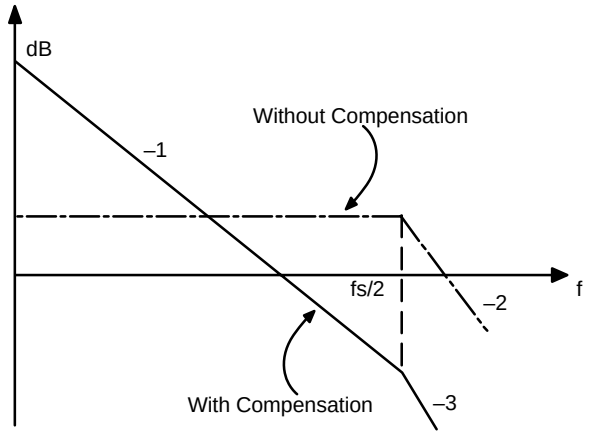


Figure 5. Bode Plot of Control–to–Output Transfer Function

If a transconductance amplifier is used as the error amplifier, the integrator pole can be implemented by connecting a capacitor from the amplifier output to the ground. The compensation gain is given by:

$$F_C(s) = \frac{G}{(sC_{COMP})} \quad (12)$$

where G is the transconductance of the amplifier.

The total loop gain is

$$T(s) = \frac{G}{R_I \times sC_{COMP}[1.0 + s/(\omega_n Q) + s^2/\omega_n^2]} \quad (13)$$

The value of the compensation capacitor C_{COMP} can be calculated if the crossover frequency is known. Generally, the crossover frequency should be chosen well below the switching frequency.

We can choose

$$f_{CO} = 1/6 \times f_S$$

So

$$C_{COMP} = \frac{G}{R_I \times 2.0\pi f_{CO}} \quad (14)$$

7. Design of Voltage Compensation Network

For voltage, “control” is referred to the output of the Voltage Error Amplifier (V_{COMP}) and “output” is the output voltage. The control–to–output transfer function with closed current loop is given by:

$$\frac{V_{OUT}}{V_{COMP}} \approx \frac{R(1.0 + sC \times ESR)}{R_I(1.0 + sCR)[1.0 + s/(\omega_n Q) + s^2/\omega_n^2]} \quad (15)$$

Compare the above expression with equation (9), the transfer function of current mode voltage control has same poles as I^2 control. The difference is the zero. For I^2 control, the zero is determined by both ESR of the output capacitor and the load resistor and can be cancel out the low frequency pole. But for current mode voltage control, the zero is a high frequency ESR zero. The low frequency pole cannot be cancelled. So the system is third–order. The Bode plot of the control–to–output transfer function with closed current loop is illustrated in Figure 6

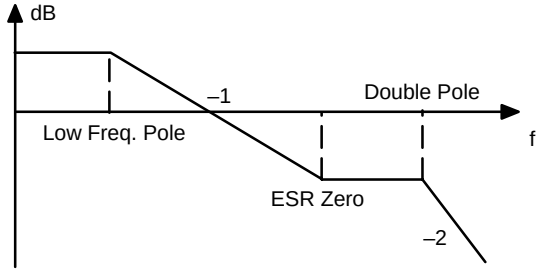


Figure 6. Bode Plot

For a transconductance error amplifier, a possible compensation network is shown in Figure 7. The compensation network has two poles and one zero.

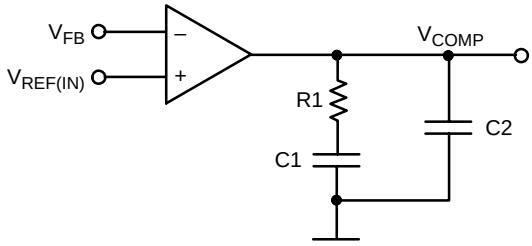


Figure 7. Compensation Network

The compensation gain is given by:

$$F(s) = \frac{G \times (1.0 + sR1C1)}{(C1 + C2) \times s[1.0 + sR1C1C2/(C1 + C2)]} \quad (16)$$

The integrator pole will give the system high DC gain. Use the zero to compensate the excessive phase delay caused by the low frequency pole of the control–to–output transfer function. The other pole of the compensation network should be placed around the ESR zero to make sure the amplitude decrease fast after the 0 dB crossover.

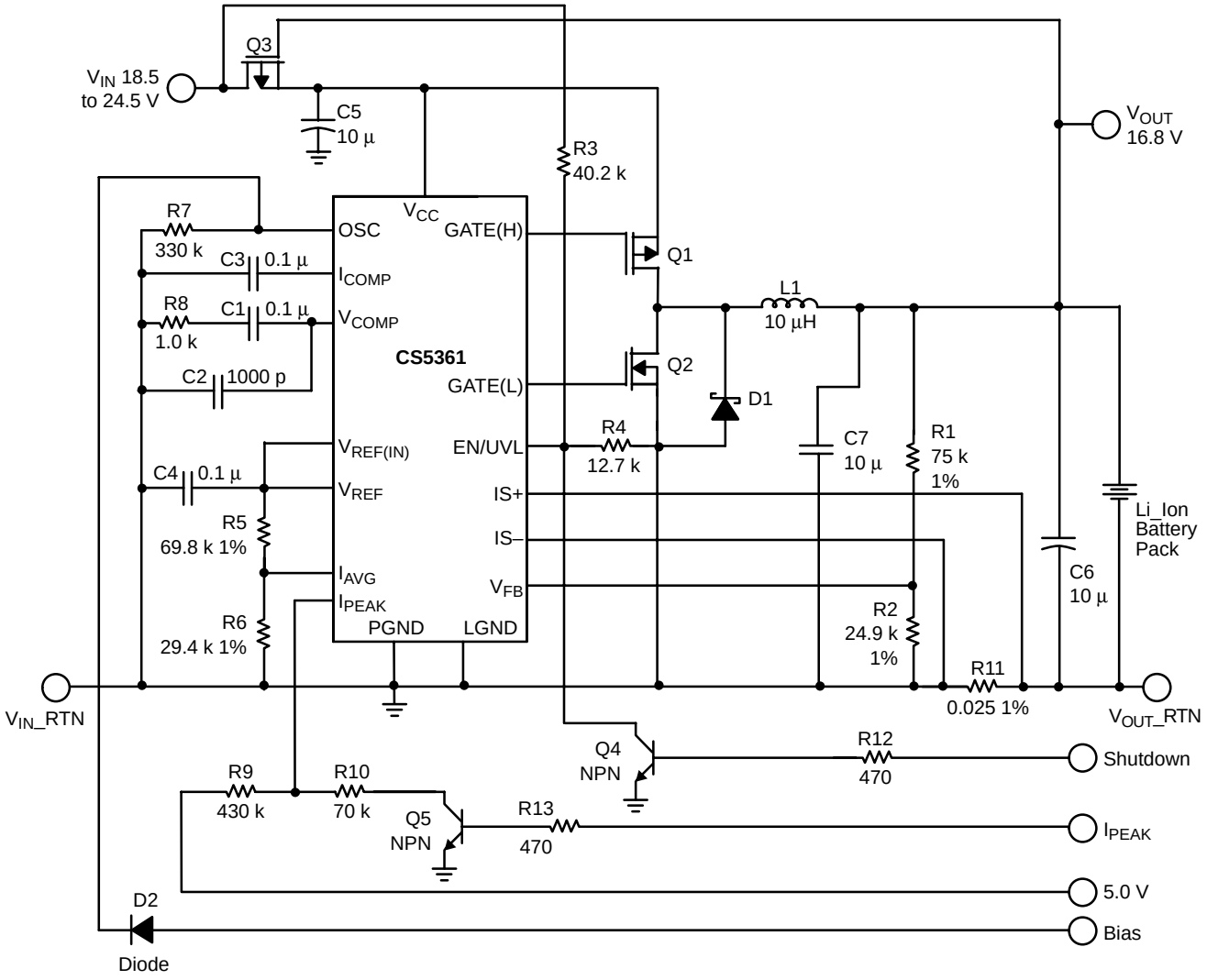


Figure 8. Additional Application Diagram, 16.8 V/2.0 A Four Cell Lithium–Ion Battery Charger with Low Side Current Sensing

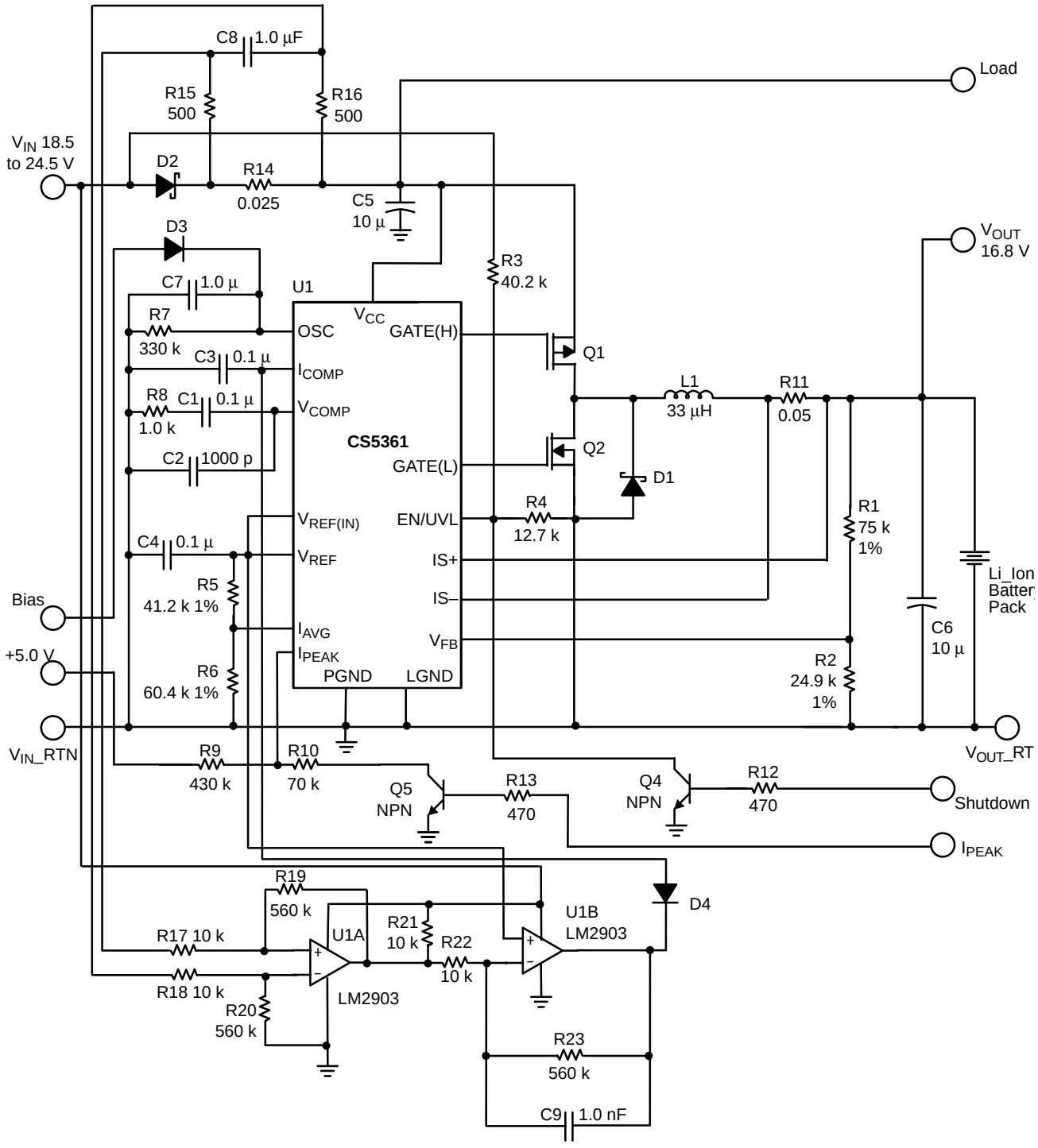
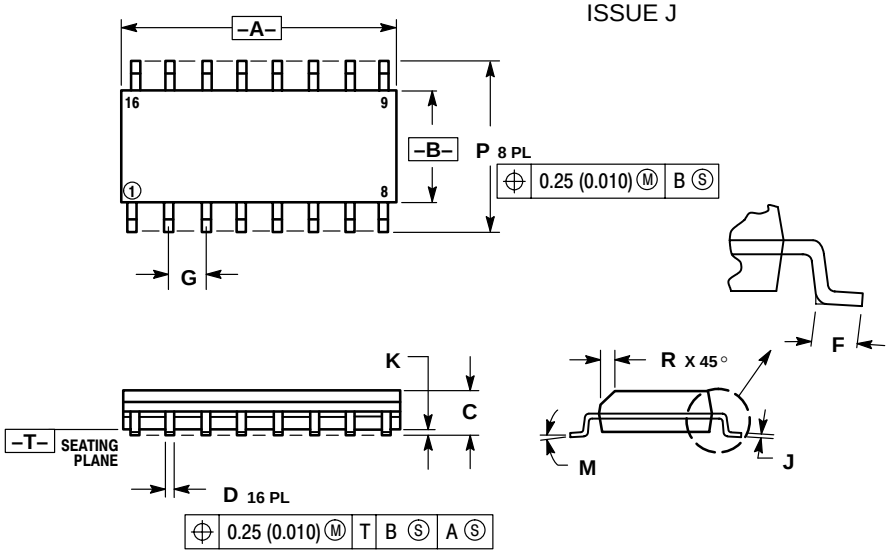


Figure 9. Additional Application Diagram, 16.8 V/2.0 A Four Cell Lithium–Ion Battery Charger with High Side Current Sensing and Input Current Limiting

PACKAGE DIMENSIONS

SO–16
D SUFFIX
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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