CMOS 4-BIT MICROCONTROLLER

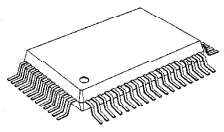
TMP47C423ADF

The 47C423A is a high speed and high performance 4-bit single chip microcomputer with LCD driver, High Speed Event Counter and Pulse output circuit based on the TLCS-47 series.

PART No.	ROM	RAM	PACKAGE
TMP47C423ADF	4096 × 8-bit	256 × 4-bit	QFP64-P-1420-1.00A

FEATURES

QFP64-P-1420A-1.00A

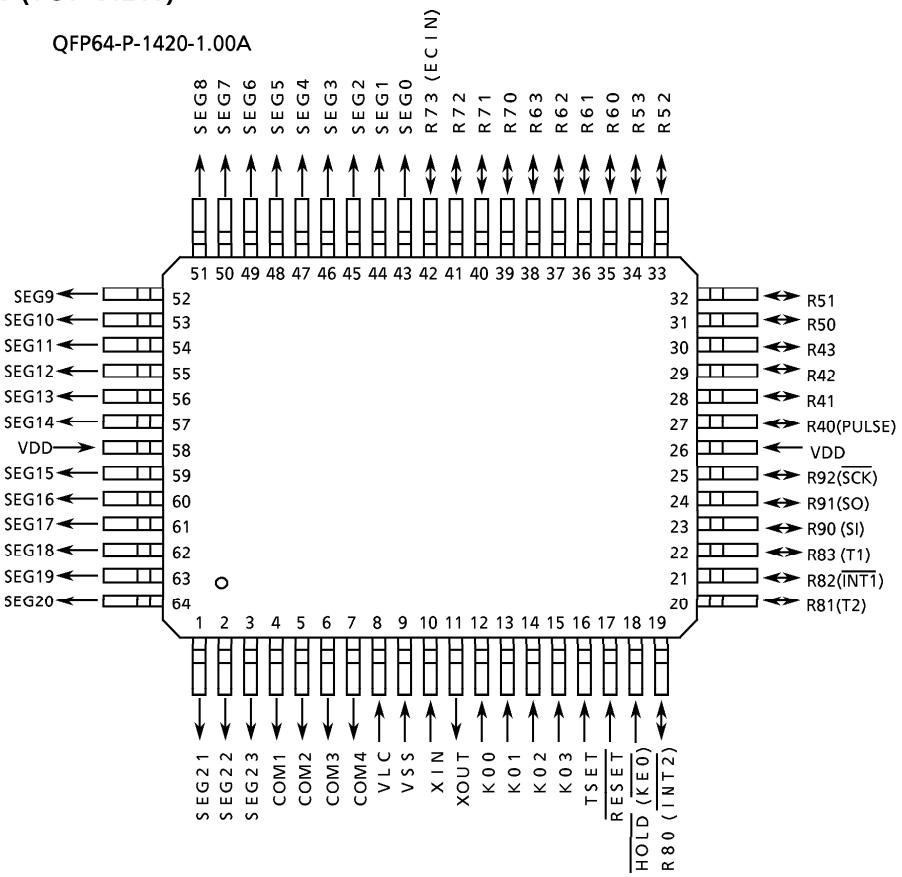


TMP47C423ADF

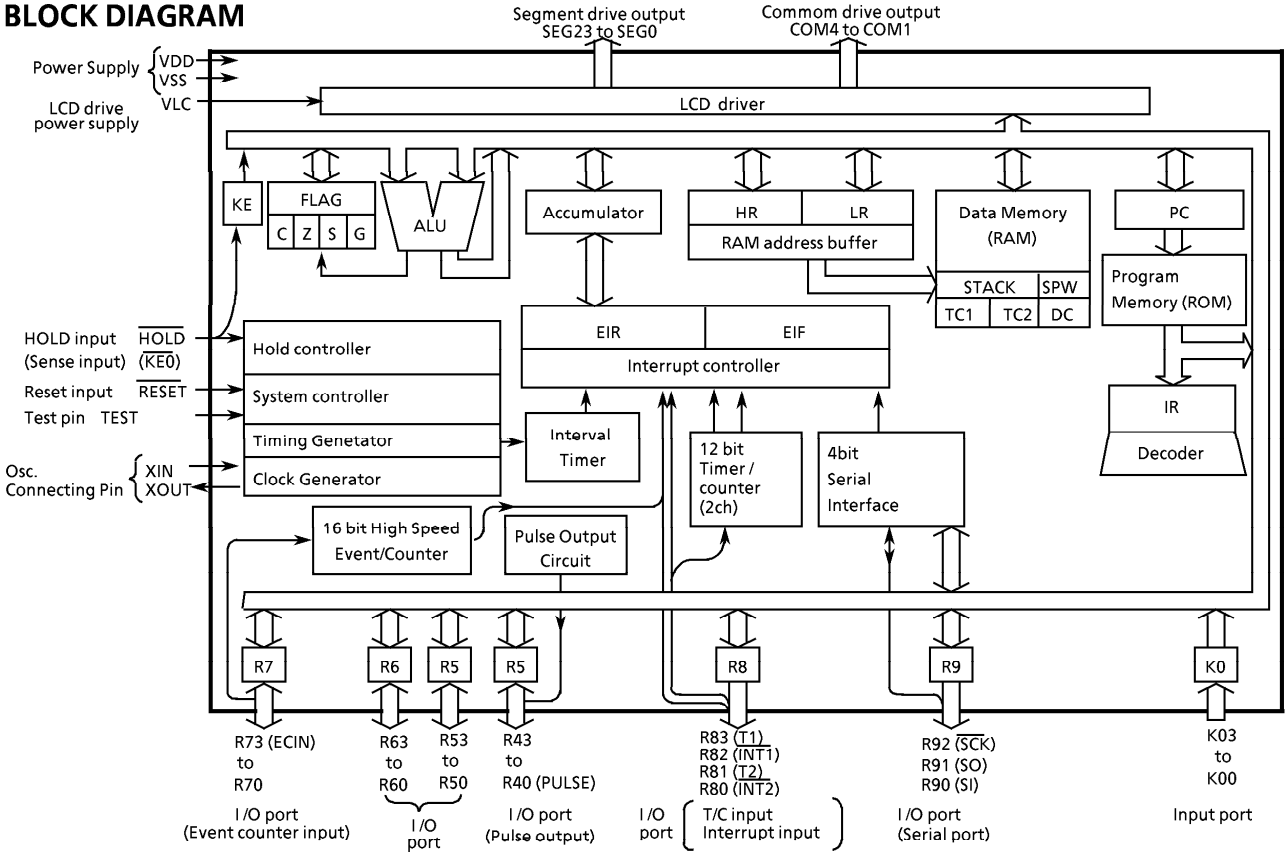
- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9 μs (at 4.2 MHz)
- ◆89 basic instructions
  - Table look-up instrucitons
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External: 2, Internal: 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (28 pins)
  - Input 2 ports 5 pins
  - I/O 6 ports 23 pins
- ◆Interval Timer
- ◆Two 12-bit Timer / Counters
  Timer, event counter, and pulse width measurement mode
- ◆16 bit High Speed Event Counter
- ◆Serial Interface with 4-bit buffer
  External/Internal colck, and leading / training edge shift mode
- ◆LCD driver
  - LCD direct drive is available (Max.12-digit dIsplay at 1/4 duty LCD)
  - 1/4, 1/3, 1/2 duties or static drive programmably selectable.
- ◆Pulse Output
  Output frequency select
- ◆High current output ports
  - Sink current (typ. 20 mA × 2 bit)
  - Source current (typ. – 20 mA × 2 bit)
- ◆Hold function
  Battery / Capacitor back-up
- ◆Real Time Emulator : BM47219A

PIN ASSIGNMENT (TOP VIEW)

QFP64-P-1420-1.00A



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input / Output	FUNCTIONS	
K03 to K00	Input	4-bit input port	
R43 to R41	I/O	4-bit I/O port with latch. When using as pluse output, the latch must be set to "1".	
R40 (PULSE)	I/O (Output)		Pulse output
R53 to R50	I/O	4-bit I/O port with latch. When using as input port, the latch must be set to "1".	
R63 to R60			
R73 (ECIN)	I/O (Input)	4-bit I/O port with latch. When using High speed event/counter, the latch must be set to "1".	High Speed Event Contor Input
R72 to R70	I/O		
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer / Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer / Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I /O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
SEG23 to SEG0	Output	LCD Segment drive output	
COM4-COM1		LCD Common drive output	
XIN	Input	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request / release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5 V	
VSS		0 V (GND)	
VLC		LCD drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C423A the configuration and functions of hardwars are described. As the description has been provided with priority on those parts deffering from the 47C400B, thchnical data sheets for the 47C400B shall also be referred to.

1. SYSTEM CONFIGURATION

◆ INTERNAL CPU FUNCTION

They are the same as those of the 47C 400B

◆ PERIPHERAL HARDWARE FUNCTION

① I/O Ports
② Interval Timer
③ Timer / Counter
④ High Speed Event counter
⑤ Pulse output
⑥ LCD Driver
⑦ Serial Interface

The description has been provided with priority on functions (① and ③ to ⑥) added to and changed from the 47C400B.

2. PERIPHERAL HARDWARE FUNCTION

2.1 I/O Ports

The 47C423A has 8 I/O ports (28 pins) each as fllows:

① K0 ; 4-bit input
② R4 ; 4-bit input/output (R40 pin is shared with pulse output)
③ R5, R6 ; 4-bit input/output
④ R7 ; 4-bit input/output (R73 pin is shared with pulse output)
⑤ R8 ; 4-bit input/output (Shared with external interrupt input and timer/counter input)
⑥ R9 ; 3-bit input/output (Shared with serial port)
⑦ KE ; 1-bit Sense input (Shared with hold request/release signal input)

As the description has been provided with priority on ports (②, ④ and ⑥) changed from 47C400B. Futher, 47C423A has not P1, P2 port, Therefore, the instruction [OUTB @ HL] and 5bit to 8bit data conversion table cannot be used.

Table 2-1, lists the port address asignment and the I/O instruction that can access the port.

Table 2-1. Port Address Assigments and Available I/O Insruction

Port Address (**)	Port		Input / output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p,b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	——	——	–	–	–	–	–	–	–
02	——	——	–	–	–	–	–	–	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port (HEC input)	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port (Note 2)	R9 output port	○	○	○	–	○	○	–
0A	——	HEC1 Ta Setting register	–	○	○	–	–	–	–
0B	——	HEC2 Tb Setting resister	–	○	○	–	–	–	–
0C	HEC Low data input	——	○	–	–	–	–	–	–
0D	HEC High data input	——	○	–	–	–	–	–	–
0E	SIO, hold status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial tansmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	——	–	–	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	HEC Control	–	○	–	–	–	–	–
18	Undefined	Pulse output control	–	○	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	LCD driver control 1	–	○	–	–	–	–	–
1B	Undefined	LCD driver control 2	–	○	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial Interface control	–	○	–	–	–	–	–

Note 1. "——" means the reserved state. Unavailable for the user programs.

Note 2. Bits 3 of IP09 is used for a status register of the High Speed Event/Counter (HEC).

(1) Port R4 (R43 to R40), Port R7 (R73 to R70)
The 4-bit I/O ports with a latch. When used as an input port, the latch showld be set to "1". The latch is initialized to "1" during reset. R40 pin is shared by pulse output pin. To use this pin for the furctional pin, the latch must be set to "1". R73 pin is shared by High speed event input pin. To use this pin for the furctional pin, the latch must be set to "1". To use it for an oridinary I/O pin, the acceptance of pulse output must be disabled.

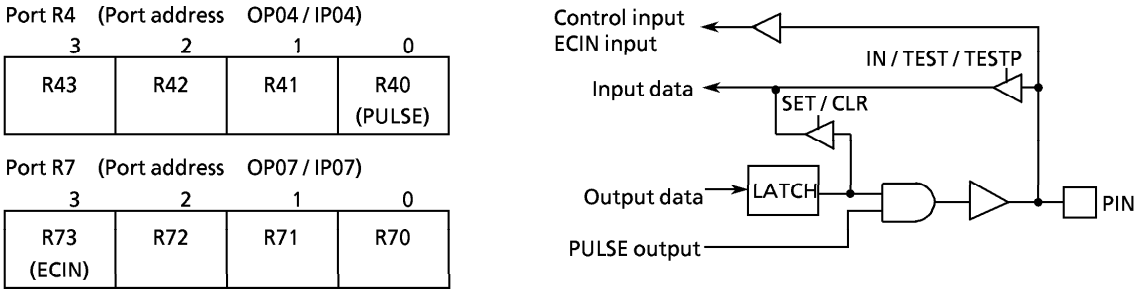


Figure 2-1. Port R4, R7

(2) Port R9 (R92 to R90)
The 3-bit I/O port with a latch. That pin R93 does not exist.
R93 input port is used for a status register of the High Speed Event / Counter.
In detail a chapter of High Speed Event/Counter shall also be referred to.
All else is the same as for the 47C400B.

2.2 Timer Counter (TC1, TC2)

The timer / counter of 47C423A is similer to that of the 47C400B except for the following point.
The maximum frequency applied to the external input pin under the event counter mode is dependent upon the operating state of the LCD drive circuit.

Table 2-2. The maximum frequency applied to external input pin under the event counter mode.

Operating State of the LCD driver	Maximum frequency applied [Hz]			
	1-channel operation		2-channel operation	
	TC1	TC2	TC1	TC2
At time of blanking operation	fc/32		fc/32	fc/40
When LCD display is enabled	fc/64		fc/72	

Note fc ; Basic clock frequency

2.3 High Speed Event/Counter (HEC)

The 47C423A has a 16-bit high-speed event counter (HEC) which can be used for ECIN pin input frequency measurement. HEC counts the falling edge of input pulses while the window gate pulse is at "H" level and interrupt requests (ECNT) are generated when the window gate pulse falls.
The window gate pulse cycle is set by command.
The ECIN pin is also used as the R73 pin. When used as the ECIN pin, the R73 output latch is set to"1".

2.3.1 Configuration of HEC circuit

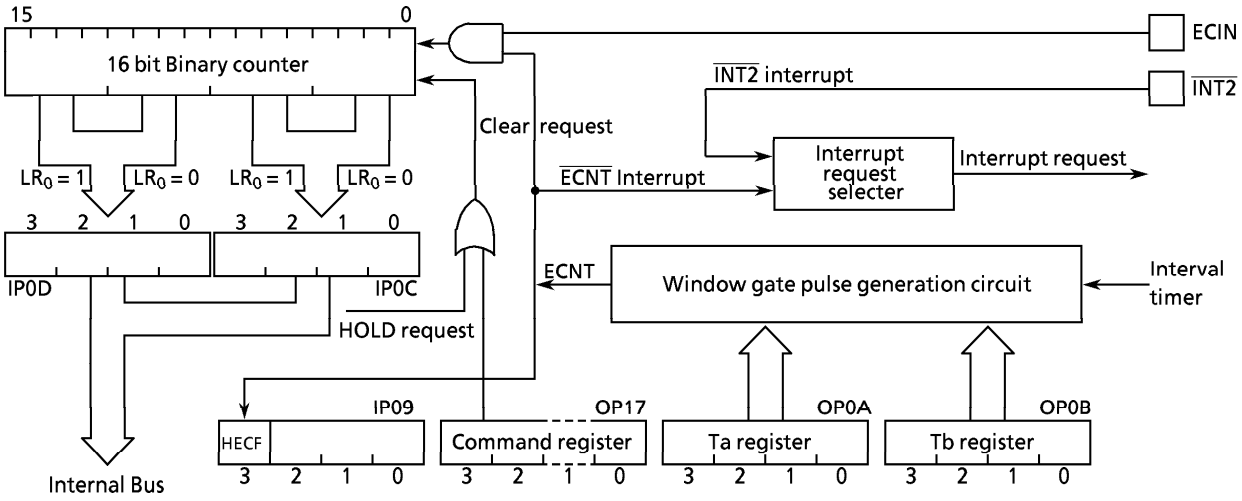


Figure 2-2. Configuration of High Speed Event / Counter

2.3.2 Control of HEC

HEC is controlled by the command register (OP17). External interrupt 2 is used as the interrupt source. The INT2 interrupt request is selected during reset, so ECNT interrupt is requested by command. Interrupt priority is the same as for external interrupt 2.

HEC control command reguster

(port address OP17)

3	2	1	0	
EHEC	CHEC		SINT	(Initial value 00*0)

EHEC	High Speed Event/Counter Function

0 : Disable
1 : Enable (Enable window gate pulse generation)

CHEC	Clear of High Speed Event/counter

0 : Clear requset (After Clear, CHEC is set to "1" autmatticary)

SINT	Select of Interrupt request

0 : $\overline{\text{INT2}}$ Interrupt request
1 : $\overline{\text{ECNT}}$ Interrupt request (folling edge of window gate pulse)

*Note. * ; don't care*

Figure 2-3. HEC Control Command Resister

HEC Operation status register (port address IP09)

(port address IP09)

3	2	1	0
HECF	(R92)	(R91)	(R90)

HECF	Operation Status

0 : Stopped (at Tb) or desable
1 : Count in process (at Ta)

Figure 2-4. HEC Operation status register

2.3.3 HEC Operation

HEC counts input frequency only during the intervals that the window gate pulse is at "H" level when EHEC (command register bit3) is"1". The window gate pulse can be set to 256 different cyclse using port addresses OP0A and OP0B.

(1) Window gate pulse setting

The window gate pulse (ECNT) consists of a count time (Ta) and non-count time (Tb), each of which can be set independently using OP0A and OP0B. Thus, one cycle is Ta + Tb. The Ta and Tb setting times are as follows.

$$(16 - n) \times 2^{13} / fc \ [s] \qquad (n = 0 \text{ to } 15)$$

Table 2-3 shows the setting times when fc = 4.194304 MHz ECNT can be generated at the next rise edge of interval timer output (fc/2^{13} [Hz] by setting EHEC = 1.

Example : Generating ECNT with a cycle of approximately 29ms and a duty ratio of 3:2.

```
OUT     #07H, %OP0A  ;  Set Ta to 17.58 ms
OUT     #0AH, %OP0B  ;  Set Tb to 11.72 ms
LD      A, #0FH
OUT     A, % OP17    ;  Enables ECNT generation
```

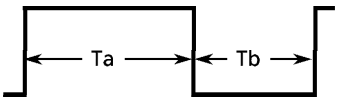


Table 2-3. Setting of Ta, Tb

Setting value	Setting time	Setting value	Setting time
0	31.25 ms	8	15.63 ms
1	29.30 ms	9	13.67 ms
2	27.34 ms	A	11.72 ms
3	25.39 ms	B	9.77 ms
4	23.44 ms	C	7.81 ms
5	21.48 ms	D	5.86 ms
6	19.53 ms	E	3.91 ms
7	17.58 ms	F	1.95 ms

(2) Count operation

Counting is enabled by setting EHEC to "1". Counting is stopped by clearing EHEC to "0" but the binary count values are held.

An INT2 interrupt is issued at the fall edge of the window gate pulse when SINT(command register bit 0) is set to"1". Normally, binary counter date are read, the counter cleared and the next count operation started by the interrupt service routine.

The binary counter is cleared with CHEC (command register bit2). EHEC and the binary counter are cleared during hold operation.

The window gate pulse (ECNT) status can be monitored using the status register. "1" is read out at "H" level (during counting). Figure 2-5 shows the HEC operation timing.

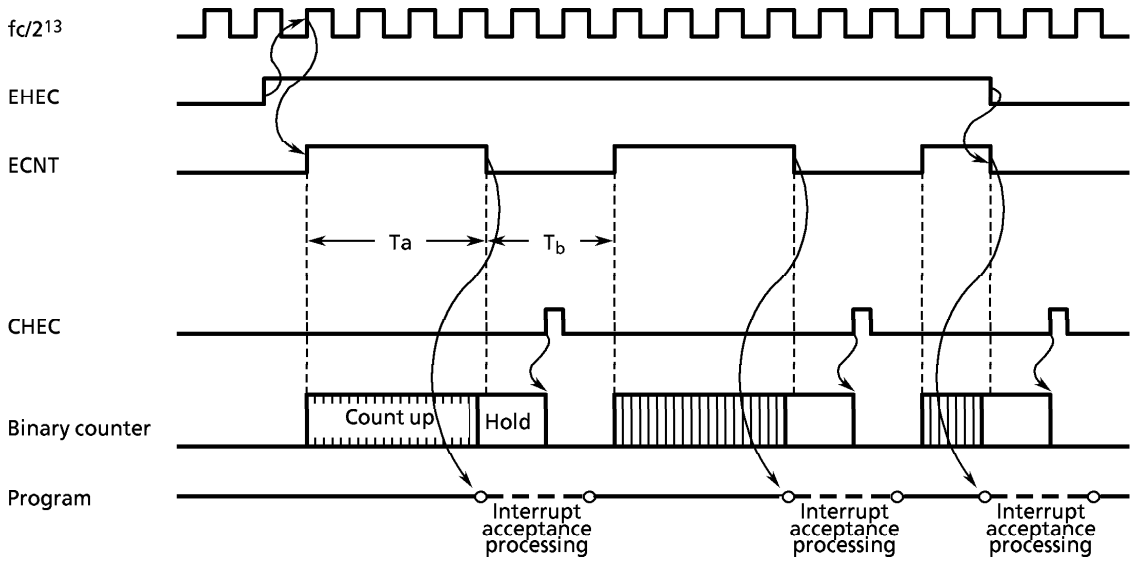


Figure 2-5. HEC Operation Timing

(3) Reading of count data

Binary counter data are read out by port addresses IP0C and IP0D. At that time, a total of 16 bits of data is read out by reading 4 bits at a time in accordance with the LR0 (L register bit 0) value. Table 2-4 shows the relationship between port address LR0 and count data.

Table 2-4. The relation ship between port address LR0 or count data

Port address	LR_0	Reading bit of HEC
IP0C	0	HEC3 to HEC0
	1	HEC7 to HEC4
IP0D	0	HEC11 to HEC8
	1	HEC15 to HEC12

2.4 Pulse output circuit

The 47C423A has a built-in one-channel pulse output to use in driving, for example, a buzzer. Eight different pulse output frequencies can be selected by command. Pulses are output from the PULSE pin. The PULSE pin is also used as the R40 pin. When used as the PULSE pin, the R40 output latch is set to "1".

2.4.1 Configuration of pulse output circuit

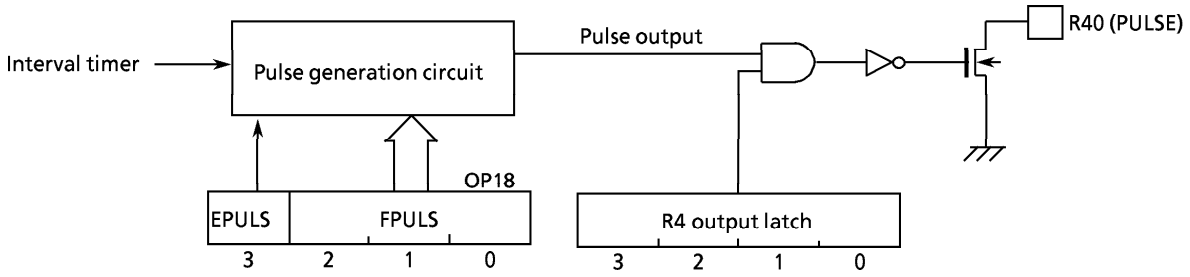


Figure 2-6. Pulse output circuit

2.4.2 Control of pulse output circuit

The pulse output circuit is controlled by the command register (OP18). Pulses are output by setting EPULS to "1". Pulse output is disabled (by clearing OP18 to"0") during hold operation.

Pulse output control command resister

(Port address OP18)

3	2	1	0	
EPULS	FPULS			(Initial value 0000)

EPULS	Pulse output control

0 : Disable
1 : Enable

FPULS	Pulse output frequency select

Example: At fc = 4.19 MH_Z

000:	$fc/(2^9 \times 8)$ [Hz]	1.024 [kHz]
001:	$fc/(2^9 \times 7)$	1.170
010:	$fc/(2^9 \times 6)$	1.365
011:	$fc/(2^9 \times 5)$	1.638
100:	$fc/(2^9 \times 4)$	2.048
101:	$fc/(2^9 \times 3)$	2.731
110:	$fc/(2^9 \times 2)$	4.096
111:	$fc/(2^9 \times 1)$	8.192

Note. fc : Basic clock frequency [H_z]

Figure 2-7. Pulse output command resister

2.5 LCD Driver

The 47C423A has the built-in circuit that directly drives the liquid crystal display (LCD) and its control circuit. The 47C423A has the following connecting pins with LCD.

① Segment output port 24pins (SEG23-SEG0)
② Common output port 4pins (COM4-COM1)

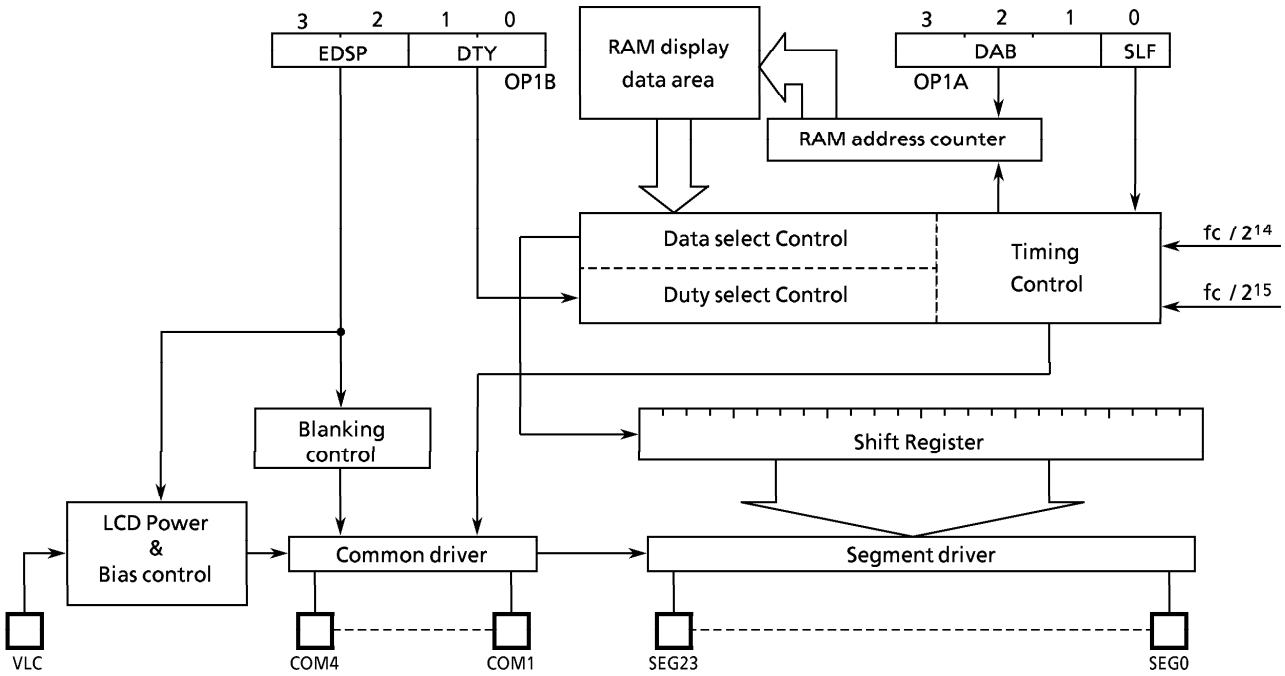
In addition, VLC pins is provided as the drive power pin.

The devices that can be directly driven is selectable from LCD of follwing drive methods.

① 1/4 DUTY (1/3 Bias) LCD MAX. 96 segments (8 segments × 12 disits)
② 1/3 DUTY (1/3 Bias) LCD MAX. 72 segments (8 segments × 9 disits)
③ 1/2 DUTY (1/2 Bias) LCD MAX. 48 segments (8 segments × 6 disits)
④ Static LCD MAX. 24 segments (8 segments × 3 disits)

2.5.1 Configuration of LCD driver

Figure 2-9. shows the configuration of the LCD driver.



Figue 2-8. Configuration of LCD driver

2.5.2 Control of LCD driver

The LCD driver is controlled by the command register 1, 2 (OP1A, OP1B)
Futher, when the command resister 1 is accessed, the most significant bit of the command register 2 must be set to "0" (Blanking or Designation of driving methods).

LCD driver control command register 1
(port address OP1A) (Initial value 1000)

3	2	1	0
DAB			SLF

DAB	Designation of display data bank
000 :	Reserved
001:	20 to 37_H
010 :	40 to 57_H
011 :	60 to 77_H
100 :	80 to 97_H
101 :	A0 to $B7_H$
110 :	C0 to $D7_H$
111 :	E0 to $F7_H$

SLF	Selection of LCD drive frequency

Example : At fc = 4.19

0 : $fc / 2^{15}$ [Hz] ..... 128 [Hz]
1 : $fc / 2^{14}$ 256

LCD driver control command register2
(port address OP1B) (Initial value 0000)

3	2	1	0
EDSP		DTY	

EDSP	LCD display control
00 :	Designation of driving methods
01 :	Blanking
10 :	Reserved
11 :	LCD display enable

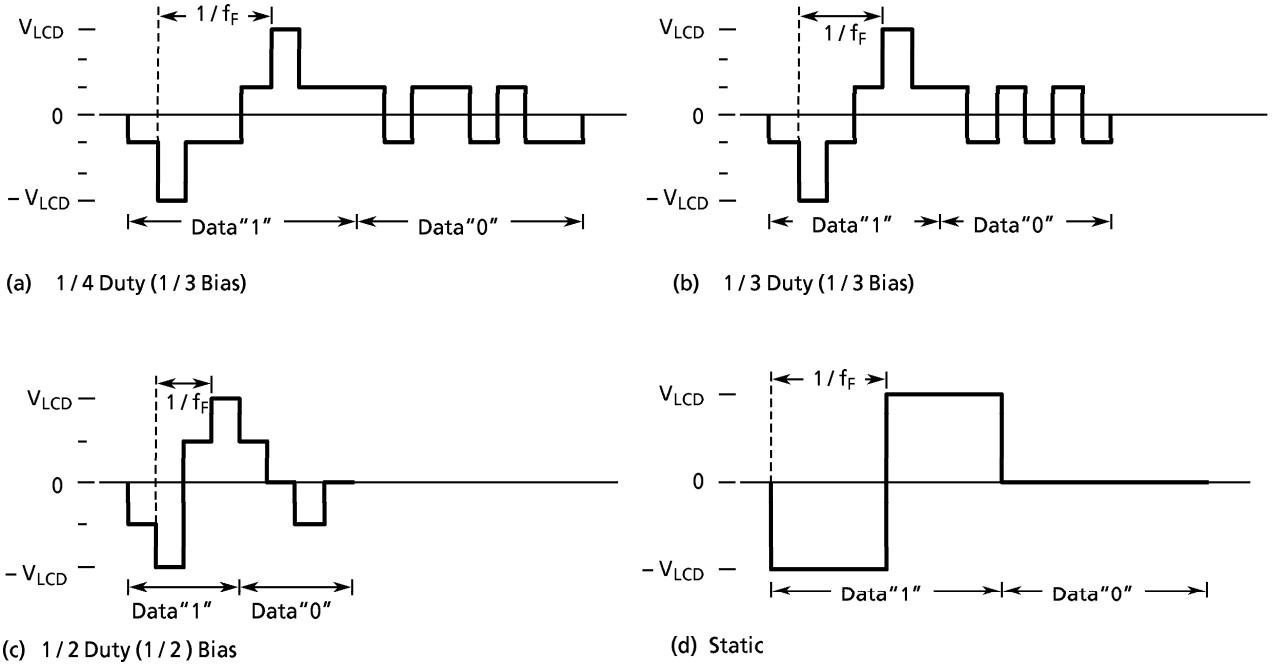
DTY	Selection of driving methods
00 :	1/4 Duty (1/3 Bias)
01 :	1/3 Duty(1/3 Bias)
10 :	1/2 Duty(1/2 Bias)
11 :	Static

Note. fc ;Basic clock frequency

Figure 2-9. LCD driver control command register

(1) Driving methods of LCD driver

4 kinds of driving methods can be selected by DTY (bits 1 and 0 of command register). Figure 2-11 shows driving waveforms for LCD.



Note. f_F *; LCD Frame frequency* V_{LCD} *; LCD drive voltage (* $= V_{DD}-V_{LC}$*)*

Figute 2-10. LCD drive waveform (Voltage COM-SEG)

(2) Frame frequency

Frame frequency is set according to the drive method and base frequency as shown in the following table 2-5.

It is possible to select base frequency (either one of 2 kind frequencies obtained from the driver) by SLF (bit 0 of command register 1).

Table 2-5. Setting of LCD frame frequency

Base frequency [Hz] \ Frame Frequency	Frame Frequency [Hz] 1 / 4 Duty	1 / 3 Duty	1 / 2 Duty	Static
$\frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$	$\frac{4}{3} \cdot \frac{fc}{2^{15}}$	$\frac{4}{2} \cdot \frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$
At fc = 4.19 MHz	128	171	256	128
$\frac{fc}{2^{14}}$	$\frac{fc}{2^{14}}$	$\frac{4}{3} \cdot \frac{fc}{2^{14}}$	$\frac{4}{2} \cdot \frac{fc}{2^{14}}$	$\frac{fc}{2^{14}}$
At fc = 2.1 MHz	128	171	256	128

Note. fc; Basic clock frequency [Hz]

(3) LCD drive voltage

The LCD drive voltage (V_{LCD}) is given by the difference in potential (V_{DD}-VLC) befween pins VDD and VLC. Therefore, when the CPU operating voltage and LCD drive voltage are the same, the VLC pin is connected to the VSS pin.

The LCD light only when the difference in potential between the segment output and common output is $\pm V_{LCD}$, and turn off at all other times.

During reset, the power switch of the LCD driver is turned off automatically, shutting off the VLC voltage. Both the segment output and common output become VDD level at this time and the LCD turn off.

The power switch is turned on to supply VLC voltage to the LCD driver by setting EDSP (bits 2 and 3 of the command register 2) to "11_B". After that, the power switch will not turn off even during blanking (setting EDSP to "01_B") and the VLC voltage continues to flow.

The power switch is turned off during hold operation low power consumption by turning off the LCD. When hold operation is released, the status in effect immediately before the hold operation is reinstated.

2.5.3 LCD Display Operation

(1) Display data setting

Display data are stored to the display data area (Max. 24 words) in the data memory.

The display data area is set using DBA (bits 1 to 3 of command register 1). During reset, the display data area is set to addresses $80\text{-}97_H$.

The display data stored to the display data area are read automatically and sent to the LCD driver by the hardware. The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display data area with a program. The table look-up instruction is mainly used for this overwriting.

Figure 2-11 shows the correspondence between the display data area and the SEG/COM pins. The LCD light when the display data is "1" and turn off when "0".

The number of segment which can be driven differs depending on the LCD drive method, therefore, the number of display data area bits used to store the data also differs. (Refer to Table 2-6) Consequently, data memory not used to store display data and data memory for which the addresses are not connected to LCD can be used to store ordinary user's processing data.

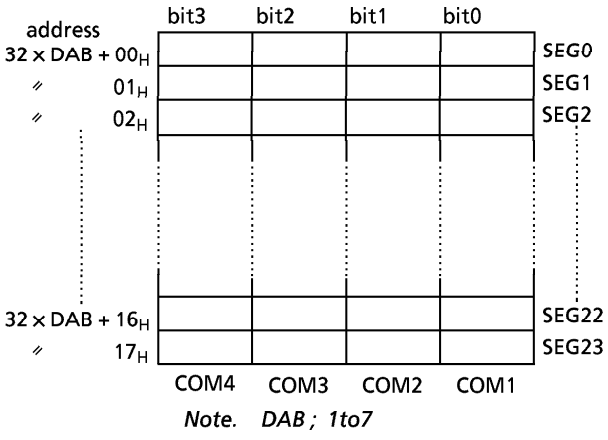


Figure 2-11. The corresponndence between the display data area and the SEG/COM pins.

Table 2-6. The data memory bits that are used for driving method and storing display data.

Driving methods	bit3	bit2	bit1	bit0
1 / 4 Duty	COM4	COM3	COM2	COM1
1 / 3 Duty	–	COM3	COM2	COM1
1 / 2 Duty	–	–	COM2	COM1
Static	–	–	–	COM1

Note. –; The data memory bits that are not used for storing display data.

(2) Transfer of display data

The display data stored to the display data area are automatically transferred to the LCD driver. The processing is performed in the following sequence.

① The LCD driver issues a display data send request to the CPU.

② When the instruction (or timer/counter processing, interrupt receive processing) currently being executed is completed, the CPU reads out the data for one cycle and sends it to the LCD driver.

The data sending cycle is generated when the VLC voltage is being applied to the LCD driver. That is, after reset is canceled, it is not generated until EDSP is set to "11_B". Table 2-7 shows the data sending cycle generation frequency. when LCD display is enabled, the virtual instruction execution speed drops. For example, when SLF = 0 and using 1/4 duty drive, this would be 2.05 μs for an instruction execution speed of 2 μs.

Table2-7. Frequency of data sending cycle insertion.

SLF	Driving method	Frequency of data sending cycle insertion
0	Static drive	24 times in 4,096 instruction cycles.
	Except static drive	24 times in 1,024 instruction cycles.
1	Static drive	24 times in 2,048 instruction cycles.
	Except static drive	24 times in 512 instruction cycles.

(3) Blanking

Blanking is applied by setting EDSP to "01_B" and turns off the LCD by outputting the non light operation level to the COM pin. The SEG pin continuously outputs the signal level in accordance with the display data and drive method.

With static drive, no voltage is applied between the COM and SEG pins when the LCD is turned off by data (display data cleared to "0"), but the COM pin output becomes constant at the $V_{LCD}/2$ level when turning off the LCD by blanking, so the COM and SEG pins are then driven by $V_{LCD}/2$.

2.5.4 Control methods of LCD driver

(1) Initial Setting

Flow chart of intial setting is shown Figure 2-13.

Example : When operating the 47C423A with 1/4 duty LCDs using a frame frequency of fc/2^{15} [Hz] (display data area at addresses 80-97_H).

```
LD      A,#0000B   ; Set the 1/4 duty drive
OUT     A,%OP1B
LD      A,#1000B   ; Setting of base frequency, display area in
                     the data memory.
OUT     A,%OP1A
 :                 ; Setting of clear or intial value of display
                     area in the memory.
 :
LD      A,#1100B   ; Display enable (Release of branking)
OUT     A,%OP1B
 :
```

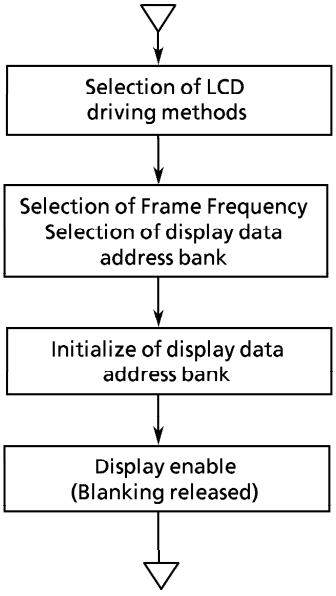


Figure 2-12. Initial set of LCD driver

(2) Store of display data

Normally, display data are kept permanently in the program memory and are then stored to the display data area by the table look-up instruction. In relation to examples of drive output, the technical data sheets for the 47C221A/421A shall also be refferd to.

This can be explained using numerical display with 1/4 duty LCD as an example. The COM and SEG connections to the LCD are shown in Figure 2-13 and the display data are shown in Table 2-8. Programming example for displaying numerals corresponding to BCD data stored at address 10_H in the data memory is shown below. The display data area is at addresses 20_H and 21_H.

```
        LD          HL,  #0FCH      ; To set the DC
        LD          A,   10H
        ST          A,   @HL+
        ST          #DTBL / 16,@HL+
        ST          #DTBL / 256,@HL+
        LD          HL,  #20H       ; Store of display data
        LDL         A,   @DC
        ST          A,   @HL+
        LDH         A,   @DC+
        ST          A,   @HL+
         ⋮
DTBL   :DATA        11011111B,   00000110B,
                    11100011B,   10100111B,
                    00110110B,   10110101B,
                    11110101B,   00010111B,
                    11110111B,   10110111B
```

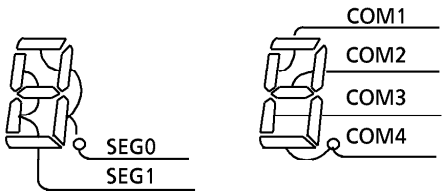


Figure 2-13. Example of COM and SEG connections

Table 2-8. Example of display data (1/4 Duty LCD)

Numeral	Display	Display data		Numeral	Display	Display data	
		Upper	Lower			Upper	Lower
0	0.	1101	1111	5	5	1011	0101
1	1	0000	0110	6	6	1111	0101
2	2	1110	0011	7	7	0001	0111
3	3	1010	0111	8	8	1111	0111
4	4	0011	0110	9	9	1011	0111

Table 2-9 shows the same numerical display used in Table 2-8, but using 1/2 duty LCD. The connections of the COM and SEG pins to the LCD are shown in Figure 2-14.

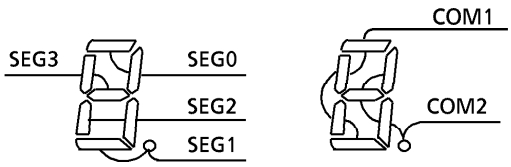


Figure 2-14. Example of COM and SEG connections

Table 2-9. Example of display data (1 / 2 Duty LCD)

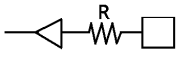
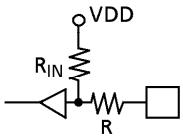
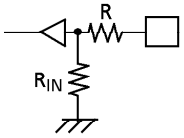
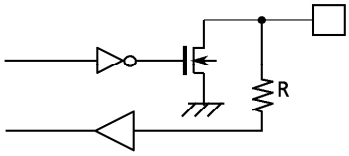
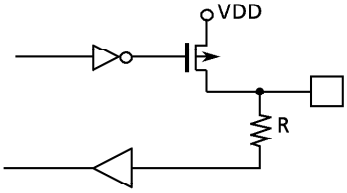
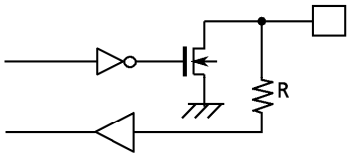
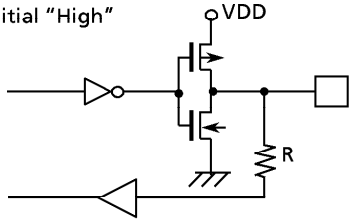
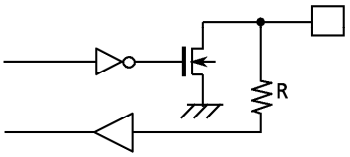
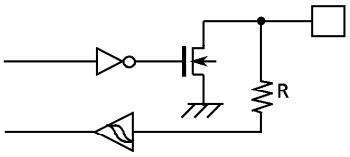
Numeral	Display data				Numeral	Display data			
	Upper		Lower			Upper		Lower	
0	**01	**11	**01	**11	5	**11	**10	**01	**01
1	**00	**10	**00	**10	6	**11	**11	**01	**01
2	**10	**10	**01	**11	7	**01	**10	**00	**11
3	**10	**01	**01	**11	8	**11	**11	**01	**11
4	**11	**10	**00	**10	9	**11	**10	**01	**11

*Note. * ; don't care*

Input / Output Circuitry

(1) Control pins
Input / Output circuitries of the 47C423A control pins are similar to the 47C400B.

(2) I/O Ports
The input/output circuitries of the 47C423A I/O port are shown below, any one of the circuitries can be shown by a code (GA to GF) as mask option.

<table>
<tr><th>Port</th><th>I/O</th><th colspan="3">input/output Circuitry (Code)</th><th></th></tr>
<tr><td rowspan="2">K0</td><td rowspan="2">Input</td><td>GA, GD</td><td>GB, GE</td><td>GC, GF</td><td rowspan="2">pull-up / pull-down resistor
R_{IN} = 70 kΩ (typ.)
R = 1 kΩ(typ.)</td></tr>
<tr><td> 
</td><td> 
</td><td> 
</td></tr>
<tr><td>R40
R41</td><td>I/O</td><td colspan="3"> 
</td><td>Sink open drain output
Initial “Hi-Z”
High current
I_{OL} = 20 mA (typ.)
R = 1 kΩ (typ.)</td></tr>
<tr><td>R42
R43</td><td>I/O</td><td colspan="3"> 
</td><td>Source open drain output
Initial “Hi-Z”
High current
I_{OH} = – 20 mA (typ.)
R = 1 kΩ (typ.)</td></tr>
<tr><td rowspan="2">R5
R6</td><td rowspan="2">I/O</td><td colspan="2">GA, GB, GC</td><td>GD, GE, GF</td><td rowspan="2">Sink open drain
or push-pull output
R = 1 kΩ (typ.)</td></tr>
<tr><td colspan="2">Initial “Hi-Z”
 
</td><td>Initial “High”
 
</td></tr>
<tr><td>R7</td><td>I/O</td><td colspan="3"> 
</td><td>Sink open drain output
Initial “Hi-Z”
R = 1 kΩ (typ.)</td></tr>
<tr><td>R8
R9</td><td>I/O</td><td colspan="3"> 
</td><td>Sink open drain output
Initial “Hi-Z”
Hysteresis input
R = 1 kΩ (typ.)</td></tr>
</table>

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.5 to 7	V
Supply Voltage (LCD drive)	V_{LC}		– 0.5 to V_{DD} + 0.5	V
Input Voltage	V_{IN}		– 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	– 0.5 to 10	
Output Current (Per 1pin)	I_{OUT1}	Except port R4	3.2	mA
	I_{OUT2}	Ports R40,R41	30	
	I_{OUT3}	Ports R42,R43	– 30	
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperture (time)	T_{sld}		260 (10 s)	℃
Strorage Temperture	T_{stg}		– 55 to 125	℃
Operating Temperature	T_{opr}		– 30 to 70	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, T_{opr} = – 30 to 70 ℃)

PARAMETER	SYMBOL	PINS	CONDISIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the Hold mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc			0.4	4.2	MHz

Note1. Input Voltage V_{IH3}, V_{IL3} in the HOLD mode.

Note2. fc : 1MHz is recommended as minimum frequency when SLF = 1. And 2MHz is when SLF = 0

D.C. CHARACTERISTICS

(V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	μA
	I_{IN2}	Open drain R port					
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5 V, V_{IN} = 0.4 V	—	—	– 2	mA
Input Registance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain port R	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Output High Current	I_{OH}	Ports R42, R43	V_{DD} = 4.5 V, V_{OL} = 3.5 V	– 15	– 20	—	mA
Output Low Current	I_{OL}	Ports R40, R41	V_{DD} = 4.5 V, V_{OL} = 1.0 V	15	20	—	mA
Segment Output Low Registance	R_{OS1}	SEG pin	V_{DD} = 5 V, V_{DD} – V_{LC} = 3 V	—	10	—	kΩ
Common Output Low Registance	R_{OC1}	COM pin					
Segment Output High Resistance	R_{OS2}	SEG pin		—	70	—	kΩ
Common Output High Resistance	R_{OC2}	COM pin					
Segment/Common Output Registance	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V, V_{LC} = V_{SS} fc = 4 MHz	—	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5 V.

Note2. Input Current IIN1 : The current through resistor is not included, when the input resistor (pull-up / pull-down) is contained.

Note3. Output resistance R_{OS}, R_{OC} : indicates the on resistance during level switching.

Note4. $V_{O2/3}$: indicates 2/3 level output voltage when driving at 1/4 or 1/3 duty.
$V_{O1/2}$: indicates 1/2 level output voltage for 1/2 duty or static drive.
$V_{O1/3}$: indicates 1/3 level output voltage when driving at 1/4 or 1/3 duty.

Note5. Supply Current : V_{IN} = 5.3 V / 0.2 V.
When K0 port has A built-in input resister, current value in that at time of open. Further voltage level at R port is valind.

Note 6. When using LCD, it is necessary to consider values of $R_{OS1/2}$ and $R_{OC1/2}$.

Note 7. Times for SEG / COM output resistance switching on :
R_{OS1}, R_{OC1} : $2^3/fc$ (s)
R_{OS2}, R_{OC2} : $1/(n \cdot f_F)$ (1/n : duty, f_F : frame frequency)

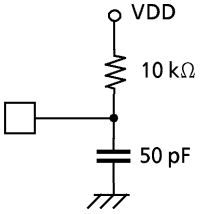
AC CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

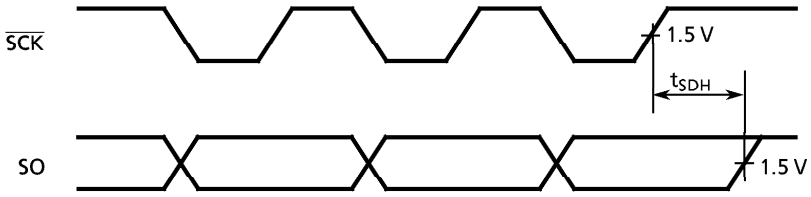
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
INSTRUCTION Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock pulse width	t_{WCH}	For external clock operation	80	—	—	ns
Low level Clock pulse width	t_{WCL}					
HEC Input Frequency	f_{HEC}	ECIN Input	—	—	fc	Hz
Shift data Hold Time	t_{SDH}		0.5 t_{cy} – 300	—	—	ns

Note. Shift data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



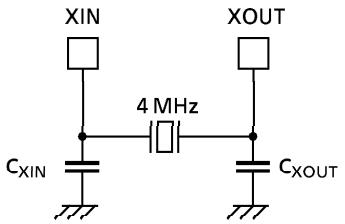
Serial port (completion of transmission)



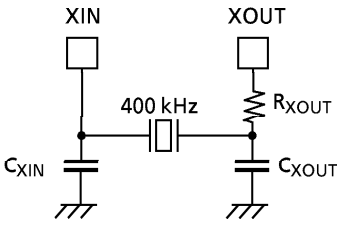
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

(1) 4 MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20 pF

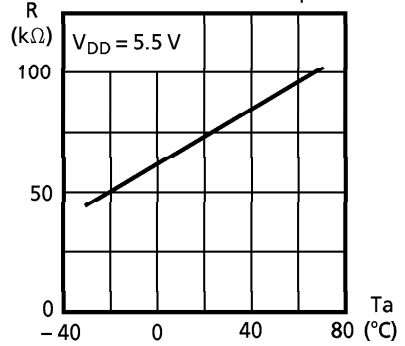


(2) 400 kHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ

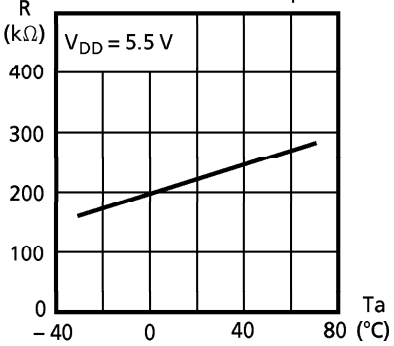


TYPICAL CHARACTERISTICS

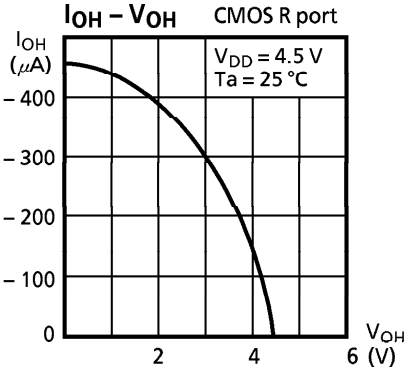
R – Ta K0 port



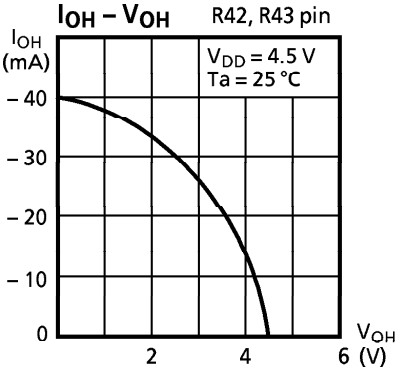
R – Ta $\overline{\text{RESET}}$ pin



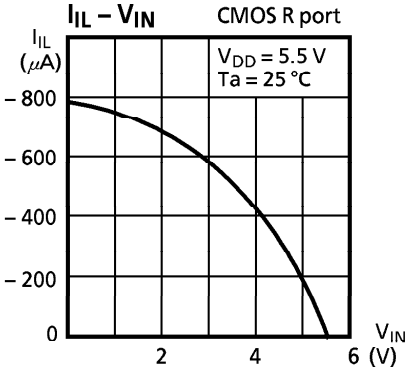
I_{OH} – V_{OH} CMOS R port



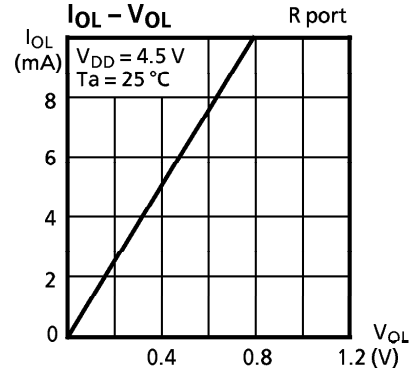
I_{OH} – V_{OH} R42, R43 pin



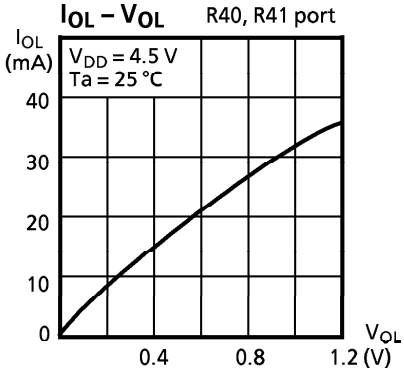
I_{IL} – V_{IN} CMOS R port



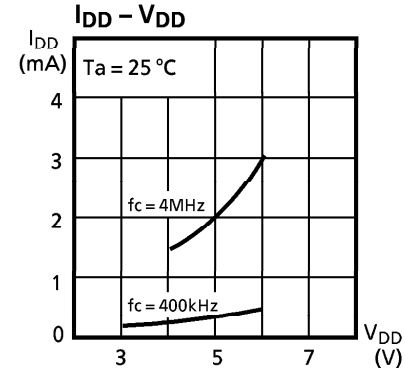
I_{OL} – V_{OL} R port



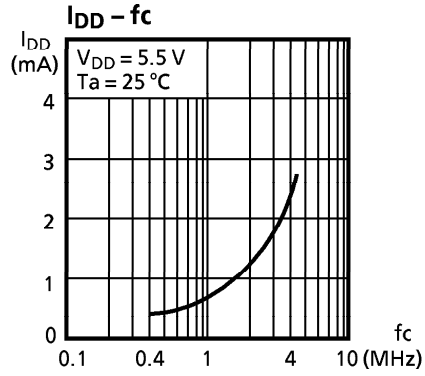
I_{OL} – V_{OL} R40, R41 port



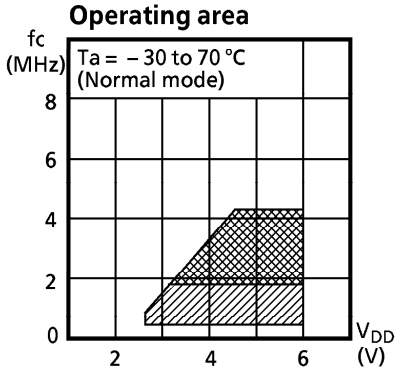
I_{DD} – V_{DD}



I_{DD} – fc



Operating area



(▨ ; LCD operation)

Note. fc : 1 MHz is recommended as minimum frequency when SLF = 1. And 2 MHz is when SLF = 0