

MH8V7245BWZTJ -5, -6

HYPER PAGE MODE 603979776 - BIT (8388608 - WORD BY 72 - BIT) DYNAMIC RAM

DESCRIPTION

The MH8V7245BWZTJ is 8388608-word x 72-bit dynamic ram module. This consist of nine industry standard 8M x 8 dynamic RAMs in TSOP and one industry standard EEPROM in TSSOP.

The mounting of TSOPs and TSSOP on a card edge dual in-line package provides any application where high densities and large of quantities memory are required.

This is a socket-type memory module ,suitable for easy interchange or addition of module.

FEATURES

Type name	/RAS access time (max.ns)	/CAS access time (max.ns)	Address access time (max.ns)	/OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.W)
MH8V7245BWZTJ-5	50	13	25	13	84	3.51
MH8V7245BWZTJ-6	60	15	30	15	104	2.93

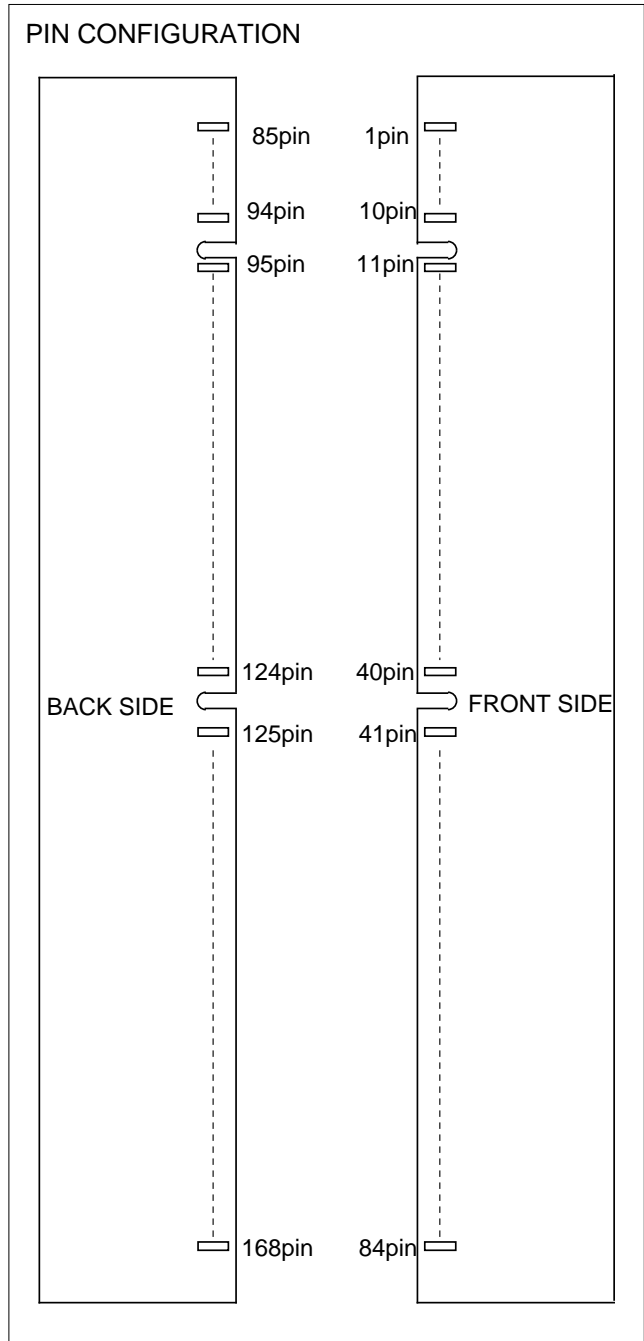
- Utilizes industry standard 8M x 8 RAMs in TSOP and industry standard EEPROM in TSSOP
- 168-pin (84-pin dual dual in-line package)
- Single +3.3V(±0.3V) supply operation
- Low stand-by power dissipation
16.2mW(Max) LVCMOS input level
- Low operation power dissipation
MH8V7245BWZTJ -5 4.22W(Max)
MH8V7245BWZTJ -6 3.89W(Max)
- All input are directly LVTTTL compatible
- All output are three-state and directly LVTTTL compatible
- Includes(0.22uF x 9) decoupling capacitors
- 4096 refresh cycle every 64ms
- Hyper-page mode,Read-modify-write, /CAS before /RAS refresh,Hidden refresh capabilities
- Gold plating contact pads

Row Address	A0 ~ A11
Column Address	A0 ~ A10

APPLICATION

Main memory unit for computers , Microcomputer memory

PIN CONFIGURATION



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PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	/OE2	86	DQ32	128	DU
3	DQ1	45	/RAS2	87	DQ33	129	NC
4	DQ2	46	/CAS2	88	DQ34	130	/CAS6
5	DQ3	47	/CAS3	89	DQ35	131	/CAS7
6	Vcc	48	/WE2	90	Vcc	132	DU
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE0	69	DQ24	111	DU	153	DQ56
28	/CAS0	70	DQ25	112	/CAS4	154	DQ57
29	/CAS1	71	DQ26	113	/CAS5	155	DQ58
30	/RAS0	72	DQ27	114	NC	156	DQ59
31	/OE0	73	Vcc	115	DU	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC	81	NC	123	NC	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	DU	167	SA2
42	DU	84	Vcc	126	DU	168	Vcc

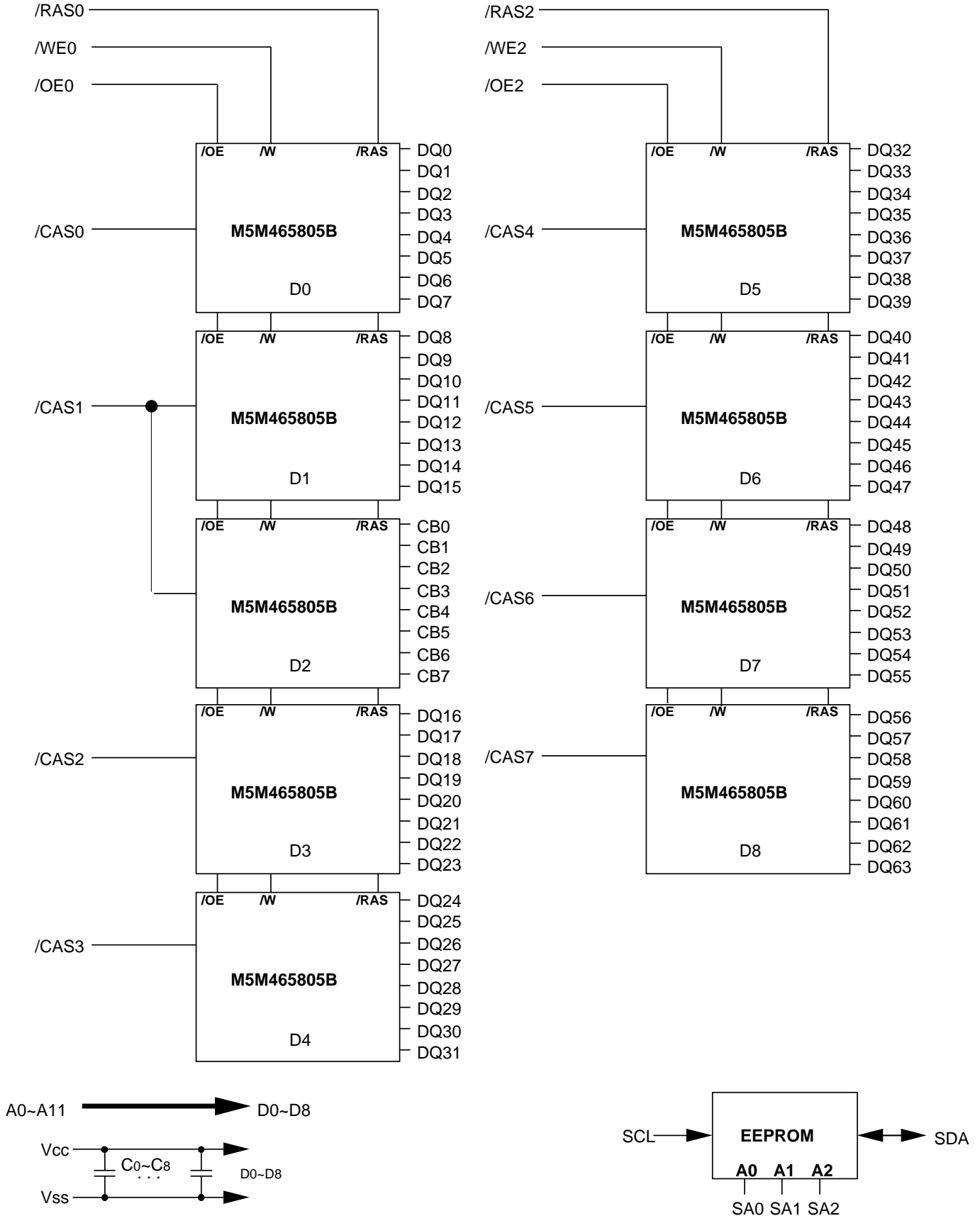
NC: No Connect

DU: Don't Use

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BLOCK DIAGRAM



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Serial Presence Detect Table

Byte	Function described	SPD entry data	SPD DATA(hex)
0	Defines # bytes written into serial memory at module mfr	128	80
1	Total # bytes of SPD memory device	256 Bytes	08
2	Fundamental memory type	EDO	02
3	# Row Addresses on this assembly	A0-A11	0C
4	# Column Addresses on this assembly	A0-A10	0B
5	# Module Banks on this assembly	1BANK	01
6	Data Width of this assembly...	x72	48
7	... Data Width continuation	0	00
8	Voltage interface standard of this assembly	LVTTTL	01
9	RAS# access time of this assembly	-5	50ns
		-6	60ns
10	CAS# access time of this assembly	-5	13ns
		-6	15ns
11	DIMM Configuration type (Non-parity,Parity,ECC)	ECC	02
12	Refresh Rate/Type	Normal : 15.625us	00
13	DRAM width,Primary DRAM	x8	08
14	Error Checking DRAM data width	x8	08
15 - 20	Superset Information (may be used in future)	option	00
21	DRAM Module Attributes	non-buffered,non-registered	00
22 - 26	Superset Information (may be used in future)	option	00
27	Precharge to Active Minimum	-5	30ns
		-6	40ns
28	Row Active to Row Active Min.	N/A	00
29	RAS to CAS Delay Min	14ns	0E
30	Active to Precharge Min	-5	50ns
		-6	60ns
31	Density of each bank on module	64MByte	10
32 - 35	Superset Information (may be used in future)	option	00
36 - 61	Superset Information (may be used in future)	option	00
62	SPD Revision	rev 1.0	01
63	Checksum for bytes 0-62	Check sum for -5	AB
		Check sum for -6	CB
64 - 71	Manufactures Jedec ID code per JEP-108E	MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location	Miyoshi,Japan	01
		Tajima,Japan	02
		NC,USA	03
		Germany	04
73 - 90	Manufactures Part Number	MH8V7245BWZTJ-5	4D4838563732343542575A544A2D35202020
		MH8V7245BWZTJ-6	4D4838563732343541575A544A2D36202020
91 - 92	Revision Code	PCB revision	rrrr
93 - 94	Manufacturing date	year/week code	yyww
95 - 98	Assembly Serial Number	serial number	sssssss
99 -125	Manufacture Specific Data	option	00
126	Intel specification frequency	N/A	00
127	Intel specification CAS# Latency support	N/A	00
128+	Unused storage locations	open	00

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FUNCTION

The MH8V7245BWZTJ provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., Hyper page mode, /CAS before /RAS refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	/RAS	/CAS	/W	/OE	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
/CAS before /RAS refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5~ 4.6	V
IO	Output current		50	mA
Pd	Power dissipation	Ta=25°C	9	W
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.0		Vcc+0.3	V
VIL	Low-level input voltage	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS

(Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
VOH	High-level output voltage	IOH=-2.0mA	2.4		Vcc	V
VOL	Low-level output voltage	IOL=2.0mA	0		0.4	V
IOZ	Off-state output current	Q floating 0V VOUT Vcc	-10		10	µA
II	Input current (except /CAS)	0V VIN Vcc+0.3, Other input pins=0V	-90		90	µA
II (CAS)	Input current (/CAS)	0V VIN Vcc+0.3, Other input pins=0V	-20		20	µA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4,5)	/RAS, /CAS cycling tRC=tWC=min. output open	- 5		1170	mA
			- 6		1080	
ICC2	Supply current from Vcc , stand-by	/RAS=/CAS =VIH, output open			9	mA
		/RAS=/CAS=WE Vcc -0.2, output open			4.5	
ICC4(AV)	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	/RAS=VIL, /CAS cycling tPC=min. output open	- 5		900	mA
			- 6		810	
ICC6(AV)	Average supply current from Vcc /CAS before /RAS refresh mode (Note 3,5)	/CAS before /RAS refresh cycling tRC=min. output open	- 5		1170	mA
			- 6		1080	

Note 2: Current flowing into an IC is positive, out is negative.

3: Icc1 (AV), Icc3 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Under condition of column address being changed once or less while /RAS=VIL and /CAS=VIH

CAPACITANCE (Ta = 0~70°C, Vcc = 3.3V±0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI (/CAS)	Input capacitance, /CAS input	Vi=Vss f=1MHZ Vi=25mVrms			20	pF
CI	Input capacitance, except /CAS input				80	pF
C(DQ)	Input/Output capacitance, DATA				15	pF
C(SCL)	Input capacitance, SPD clock				9	pF
C(SDA)	Input/Output capacitance, SPD DATA				9	pF
C(SA0~3)	Input capacitance, SPD address				7	pF

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SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits				Unit
		- 5		- 6		
		Min	Max	Min	Max	
tCAC	Access time from /CAS (Note 7,8)		13		15	ns
tRAC	Access time from /RAS (Note 7,9)		50		60	ns
tAA	Column address access time (Note 7,10)		25		30	ns
tCPA	Access time from /CAS precharge (Note 7,11)		28		33	ns
tOEA	Access time from /OE (Note 7)		13		15	ns
tOHC	Output hold time from /CAS	5		5		ns
tOHR	Output hold time from /RAS (Note 13)	5		5		ns
tCLZ	Output low impedance time /CAS low (Note 7)	5		5		ns
tOEZ	Output disable time after /OE high (Note 12)		13		15	ns
tWEZ	Output disable time after /WE high (Note 12)		13		15	ns
tOFF	Output disable time after /CAS high (Note 12,13)		13		15	ns
tREZ	Output disable time after /RAS high (Note 12,13)		13		15	ns

Note 6: An initial pause of 500us is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing /CAS before /RAS refresh).

Note the /RAS may be cycled during the initial pause. And any 8 /RAS or /RAS /CAS cycles are required after prolonged periods (greater than 64 ms) of /RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 1 TTL load and 100pF, VOH=2.4V(IOH=-2mA) and VOL=0.4V(IOL=-2mA).

The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that tRCD tRCD(max), tASC tASC(max) and tCP tCP(max).

9: Assumes that tRCD tRCD(max) and tRAD tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

10: Assumes that tRAD tRAD(max) and tASC tASC(max).

11: Assumes that tCP tCP(max) and tASC tASC(max).

12: tOEZ (max), tWEZ(max), tOFF(max) and tREZ(max) defines the time at which the output achieves the high impedance state (IOUT ± 10uA) and is not reference to VOH(min) or VOL(max).

13: Output is disabled after both /RAS and /CAS go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tREF	Refresh cycle time		64		64	ms
tRP	/RAS high pulse width	30		40		ns
tRCD	Delay time, /RAS low to /CAS low (Note16)	14	37	14	45	ns
tCRP	Delay time, /CAS high to /RAS low	5		5		ns
tRPC	Delay time, /RAS high to /CAS low	0		0		ns
tCPN	/CAS high pulse width	8		10		ns
tRAD	Column address delay time from /RAS low (Note17)	10	25	12	30	ns
tASR	Row address setup time before /RAS low	0		0		ns
tASC	Column address setup time before /CAS low (Note18)	0	10	0	13	ns
tRAH	Row address hold time after /RAS low	8		10		ns
tCAH	Column address hold time after /CAS low	8		10		ns
tDZC	Delay time, data to /CAS low (Note19)	0		0		ns
tDZO	Delay time, data to /OE low (Note19)	0		0		ns
tRDD	Delay time, /RAS high to data (Note20)	13		15		ns
tCDD	Delay time, /CAS high to data (Note20)	13		15		ns
tODD	Delay time, /OE high to data (Note20)	13		15		ns
tT	Transition time (Note21)	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD tRAD(max) and tASC tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD tRCD(max) and tASC tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

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Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tRC	Read cycle time	84		104		ns
tRAS	/RAS low pulse width	50	10000	60	10000	ns
tCAS	/CAS low pulse width	8	10000	10	10000	ns
tCSH	/CAS hold time after /RAS low	35		40		ns
tRSH	/RAS hold time after /CAS low	13		15		ns
tRCS	Read Setup time after /CAS high	0		0		ns
tRCH	Read hold time after /CAS low (Note 22)	0		0		ns
tRRH	Read hold time after /RAS low (Note 22)	0		0		ns
tRAL	Column address to /RAS hold time	25		30		ns
tCAL	Column address to /CAS hold time	13		18		ns
tORH	/RAS hold time after /OE low	13		15		ns
tOCH	/CAS hold time after /OE low	13		15		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tWC	Write cycle time	84		104		ns
tRAS	/RAS low pulse width	50	10000	60	10000	ns
tCAS	/CAS low pulse width	8	10000	10	10000	ns
tCSH	/CAS hold time after /RAS low	35		40		ns
tRSH	/RAS hold time after /CAS low	13		15		ns
tWCS	Write setup time before /CAS low (Note 24)	0		0		ns
tWCH	Write hold time after /CAS low	8		10		ns
tCWL	/CAS hold time after /W low	8		10		ns
tRWL	/RAS hold time after /W low	8		10		ns
tWP	Write pulse width	8		10		ns
tDS	Data setup time before /CAS low or /W low	0		0		ns
tDH	Data hold time after /CAS low or /W low	8		10		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note23)	109		133		ns
tRAS	/RAS low pulse width	75	10000	89	10000	ns
tCAS	/CAS low pulse width	38	10000	44	10000	ns
tCSH	/CAS hold time after /RAS low	70		82		ns
tRSH	/RAS hold time after /CAS low	38		44		ns
tRCS	Read setup time before /CAS low	0		0		ns
tCWD	Delay time, /CAS low to /W low (Note24)	28		32		ns
tRWD	Delay time, /RAS low to /W low (Note24)	65		77		ns
tAWD	Delay time, address to /W low (Note24)	40		47		ns
tOEH	/OE hold time after /W low	13		15		ns

Note 23: tRWC is specified as $tRWC(\min)=tRAC(\max)+tODD(\min)+tRWL(\min)+tRP(\min)+4t$.

24: tWCS, tCWD, tRWD, tAWD and tCPWD are specified as reference points only. If tWCS tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD tCWD(min), tRWD tRWD (min), tAWD tAWD(min) and tCPWD tCPWD(min) (for Hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until /CAS or /OE goes back to VIH) is indeterminate.

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Hyper Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by /OE or /W) (Note 25)

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time	20		25		ns
tHPRWC	Hyper page mode read write/read modify write cycle time	55		66		ns
tDOH	Output hold time from /CAS low	5		5		ns
tRAS	/RAS low pulse width for read write cycle (Note26)	65	100000	77	100000	ns
tCP	/CAS high pulse width (Note27)	8	13	10	16	ns
tCPRH	/RAS hold time after /CAS precharge	28		33		ns
tCPWD	Delay time, /CAS precharge to W low (Note24)	43		50		ns
tCHOL	Hold time to maintain the data Hi-Z until /CAS access	7		7		ns
tOEPE	/OE Pulse width (Hi-Z control)	7		7		ns
tWPE	/W Pulse width (Hi-Z control)	7		7		ns
tHCWD	Delay time, /CAS low to /W low after read	28		32		ns
tHAWD	Delay time, Address to /W low after read	40		47		ns
tHPWD	Delay time, /CAS precharge to /W low after read	43		50		ns
tHCOD	Delay time, /CAS low to /OE high after read	13		15		ns
tHAOD	Delay time, Address to /OE high after read	25		30		ns
tHPOD	Delay time, /CAS precharge to /OE high after read	28		33		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

26: tRAS(min) is specified as two cycles of /CAS input are performed.

27: tCP(max) is specified as a reference point only. If tCP tCP(max), access time is controlled exclusively by tCAC.

/CAS before /RAS Refresh Cycle (Note 28)

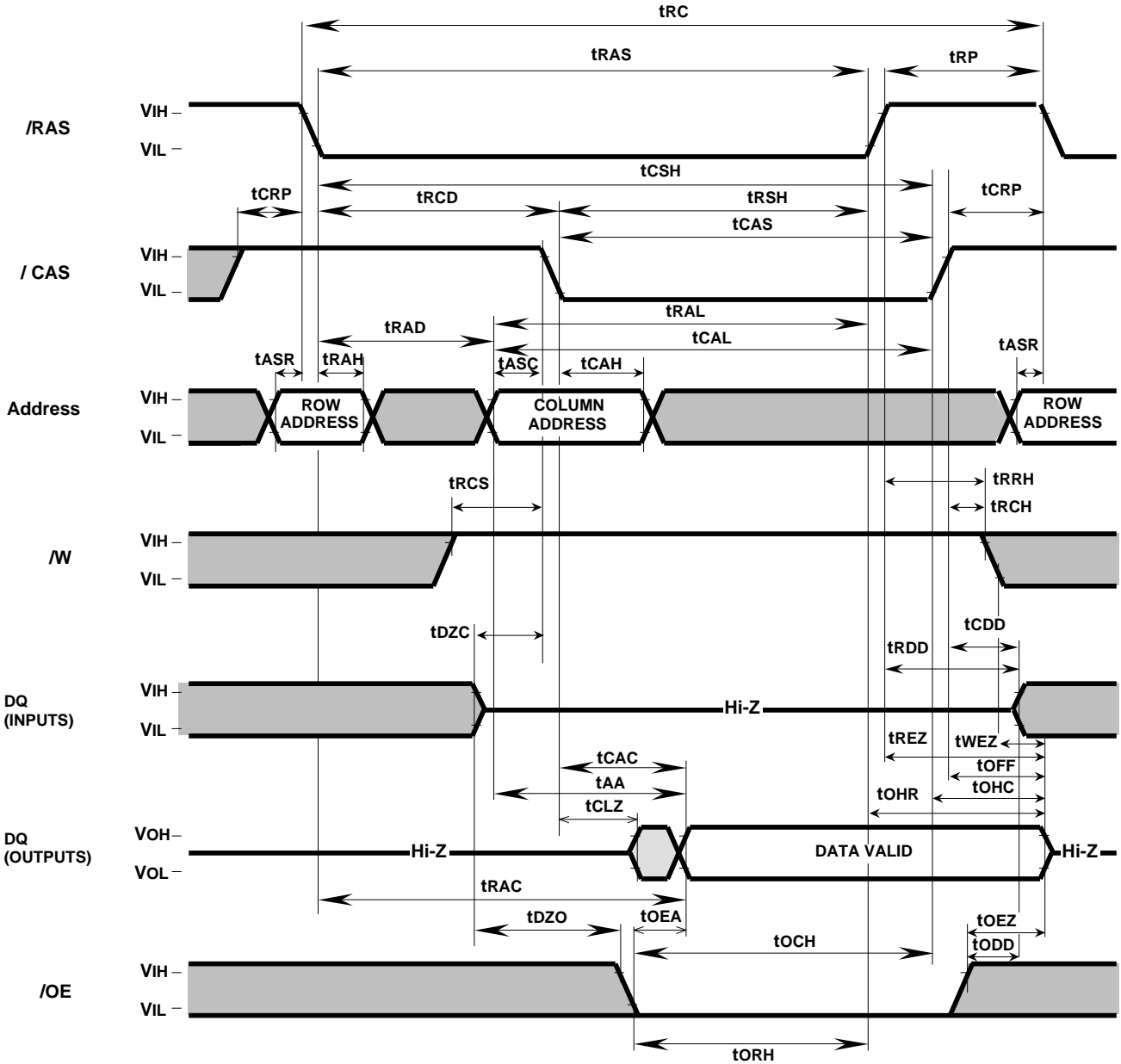
Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tCSR	/CAS setup time before /RAS low	5		5		ns
tCHR	/CAS hold time after /RAS low	10		10		ns
tRSR	Read setup time before /RAS low	10		10		ns
tRHR	Read hold time after /RAS low	10		10		ns



Note 28: Eight or more /CAS before /RAS cycles instead of eight /RAS cycles are necessary for proper operation of /CAS before /RAS refresh mode.

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Timing Diagrams (Note 29) Read Cycle

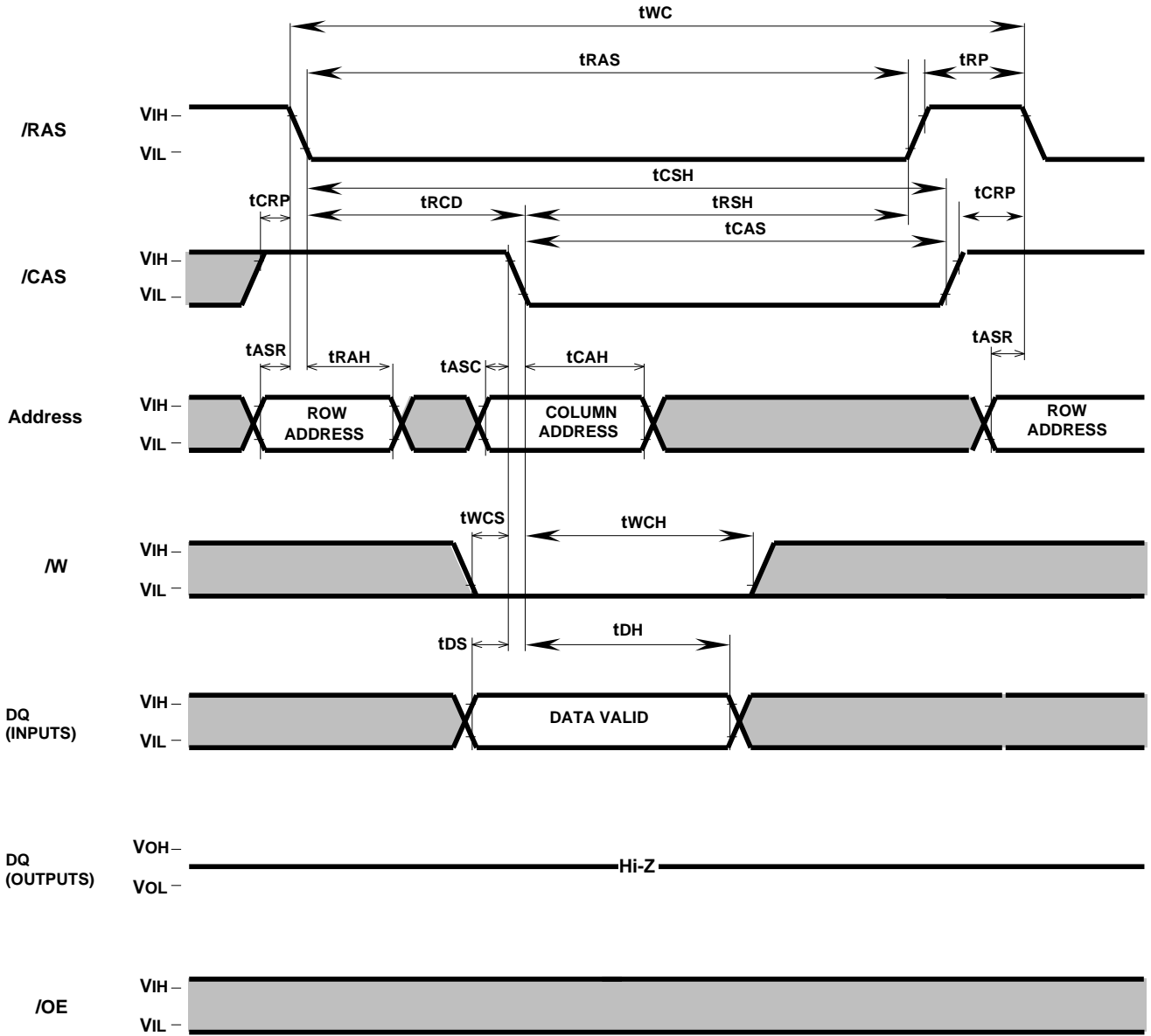


Note 29  Indicates the don't care input.
 $V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$
 Indicates the invalid output.

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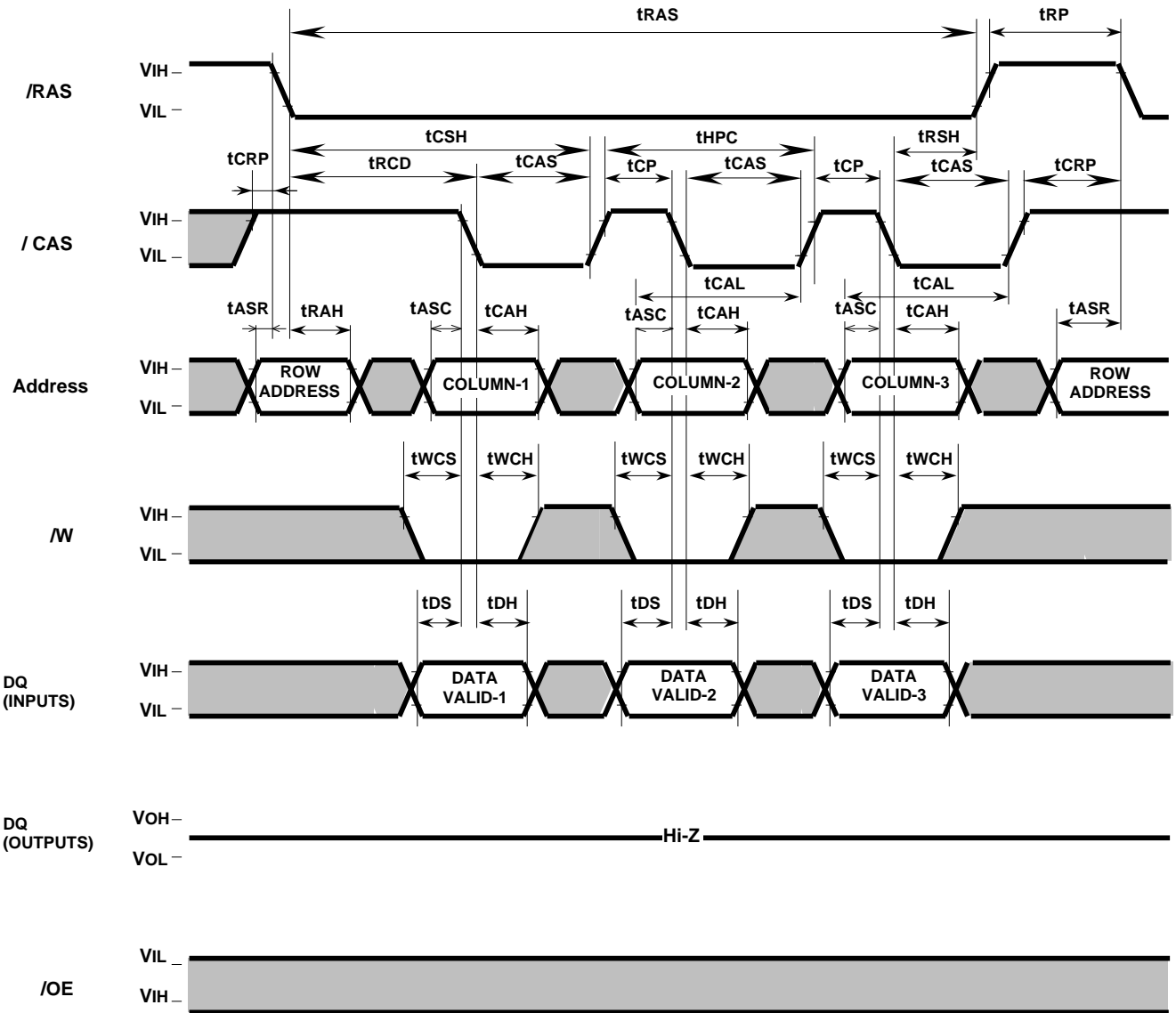
Early Write Cycle



MH8V7245BWZTJ -5, -6

HYPER PAGE MODE 603979776 - BIT (8388608 - WORD BY 72 - BIT) DYNAMIC RAM

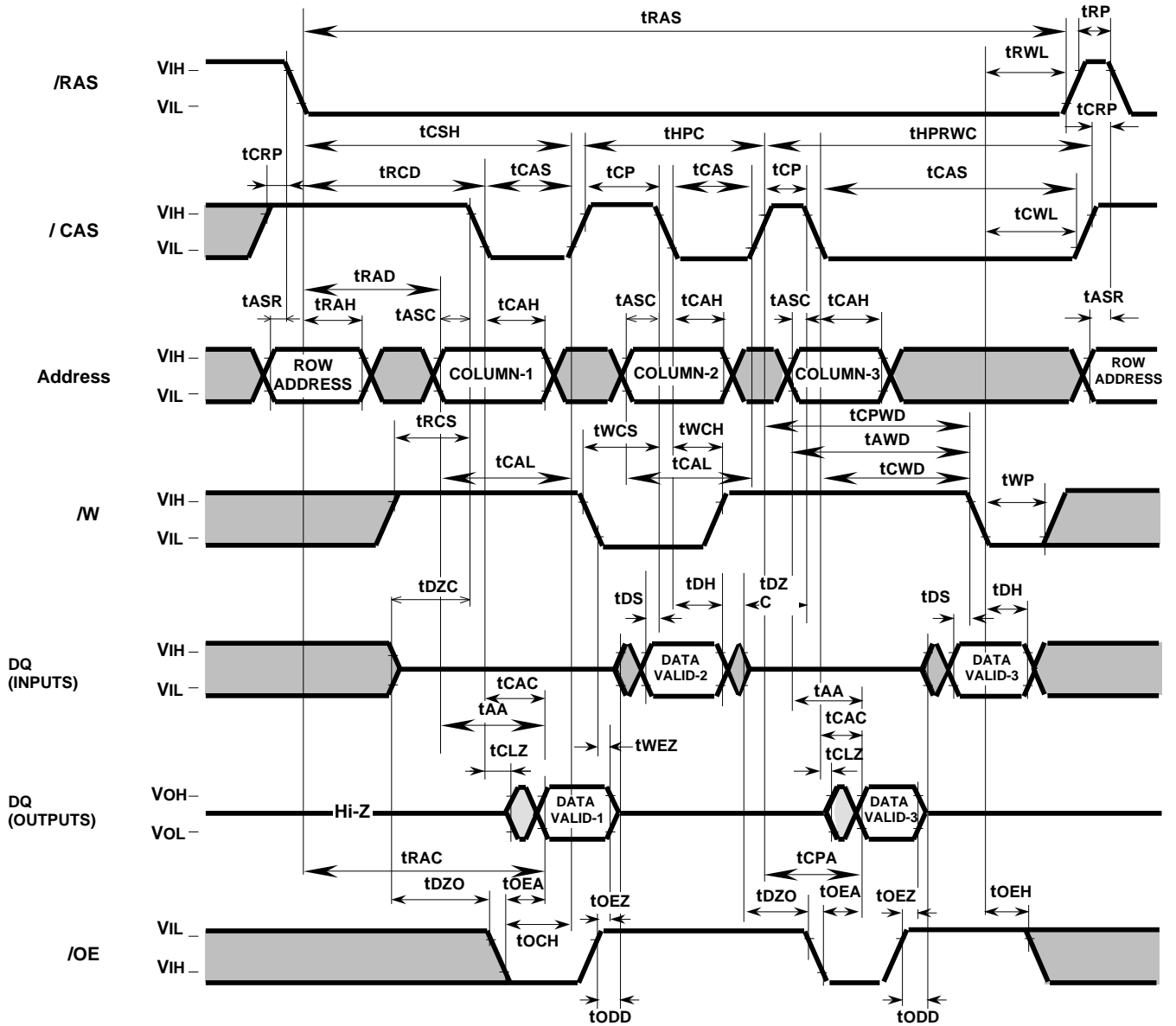
Hyper Page Mode Early Write Cycle



MH8V7245BWZTJ -5, -6

HYPER PAGE MODE 603979776 - BIT (8388608 - WORD BY 72 - BIT) DYNAMIC RAM

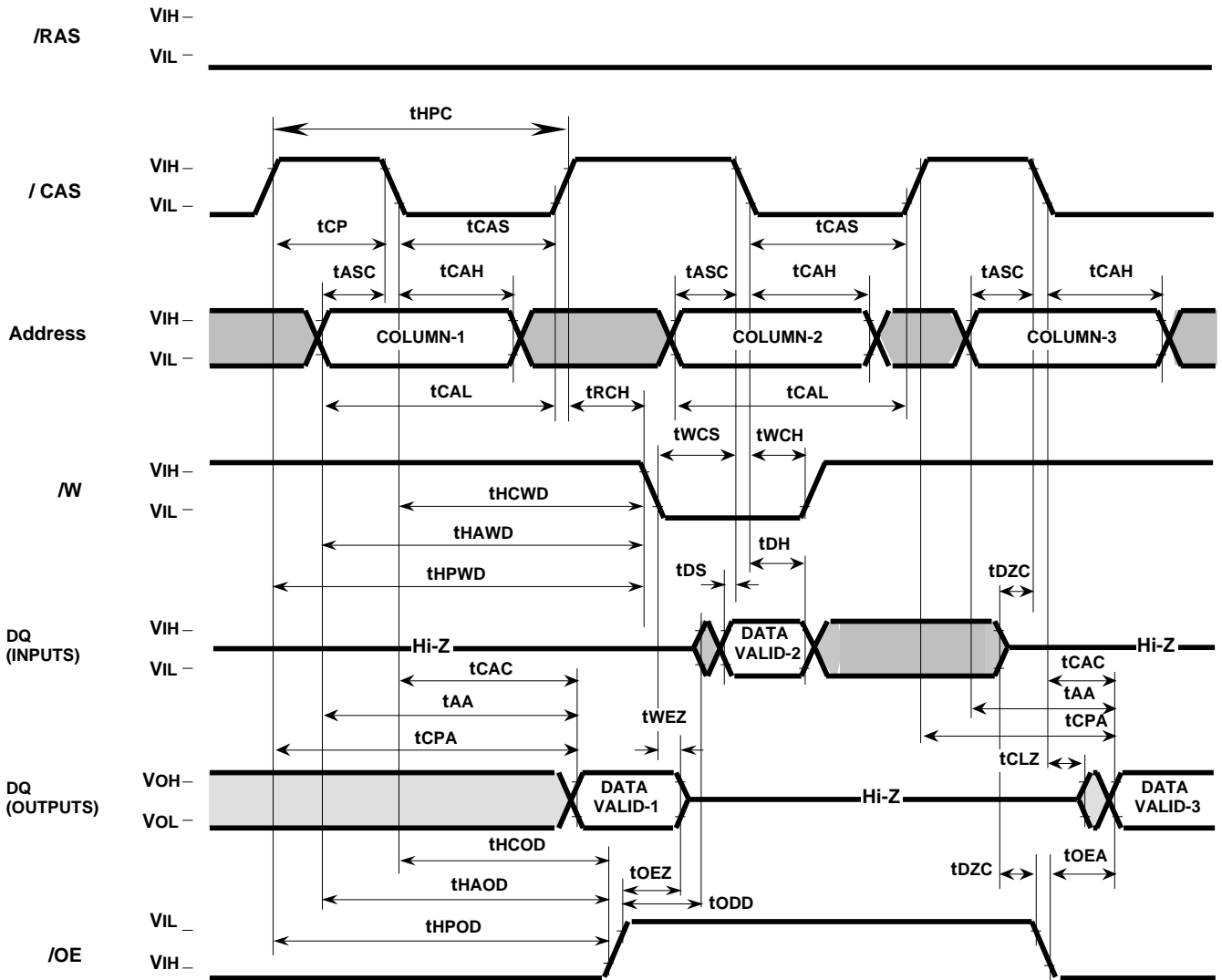
Hyper Page Mode Mix Cycle (1)



MH8V7245BWZTJ -5, -6

HYPER PAGE MODE 603979776 - BIT (8388608 - WORD BY 72 - BIT) DYNAMIC RAM

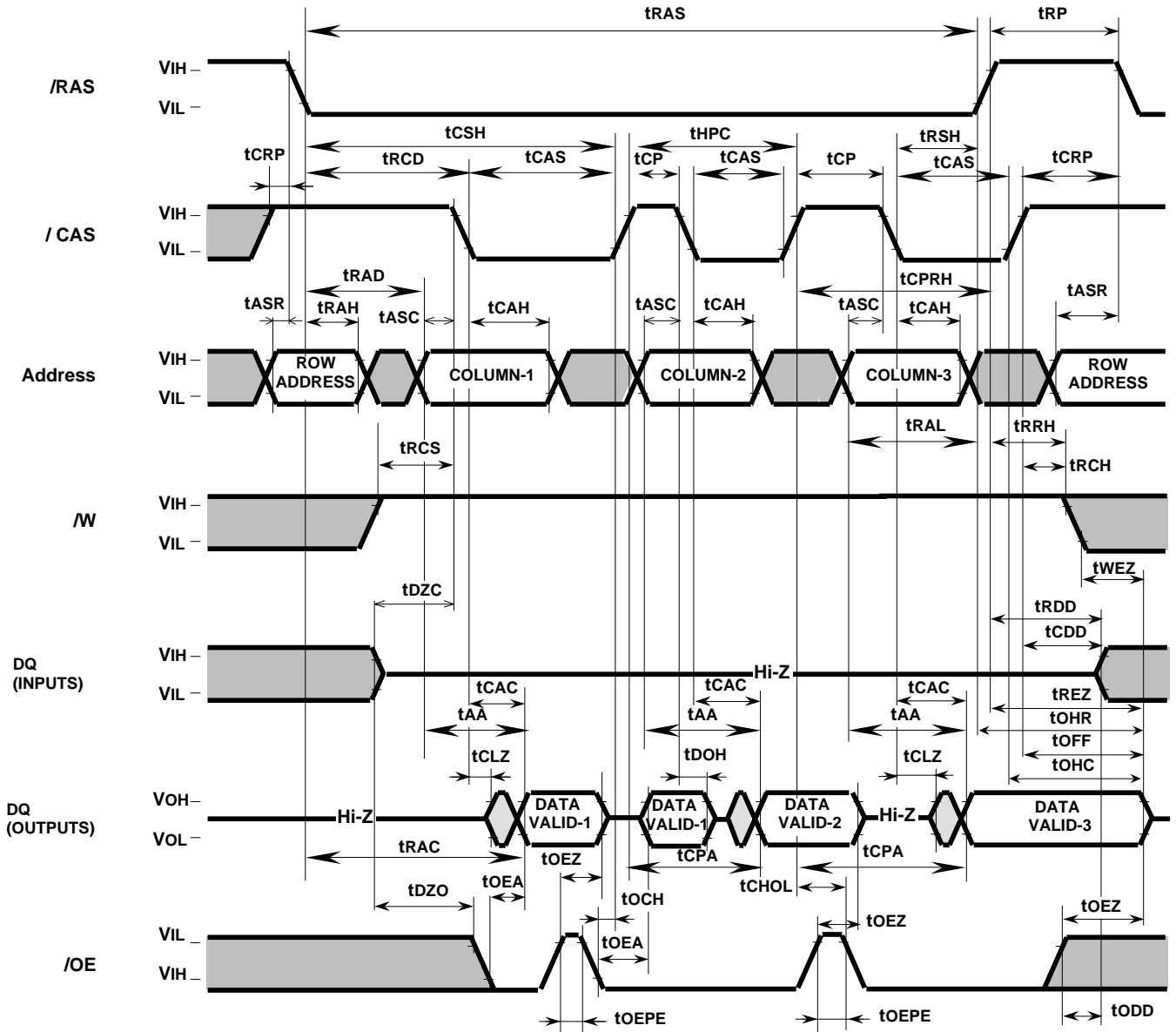
Hyper Page Mode Mix Cycle (2)



MH8V7245BWZTJ -5, -6

HYPER PAGE MODE 603979776 - BIT (8388608 - WORD BY 72 - BIT) DYNAMIC RAM

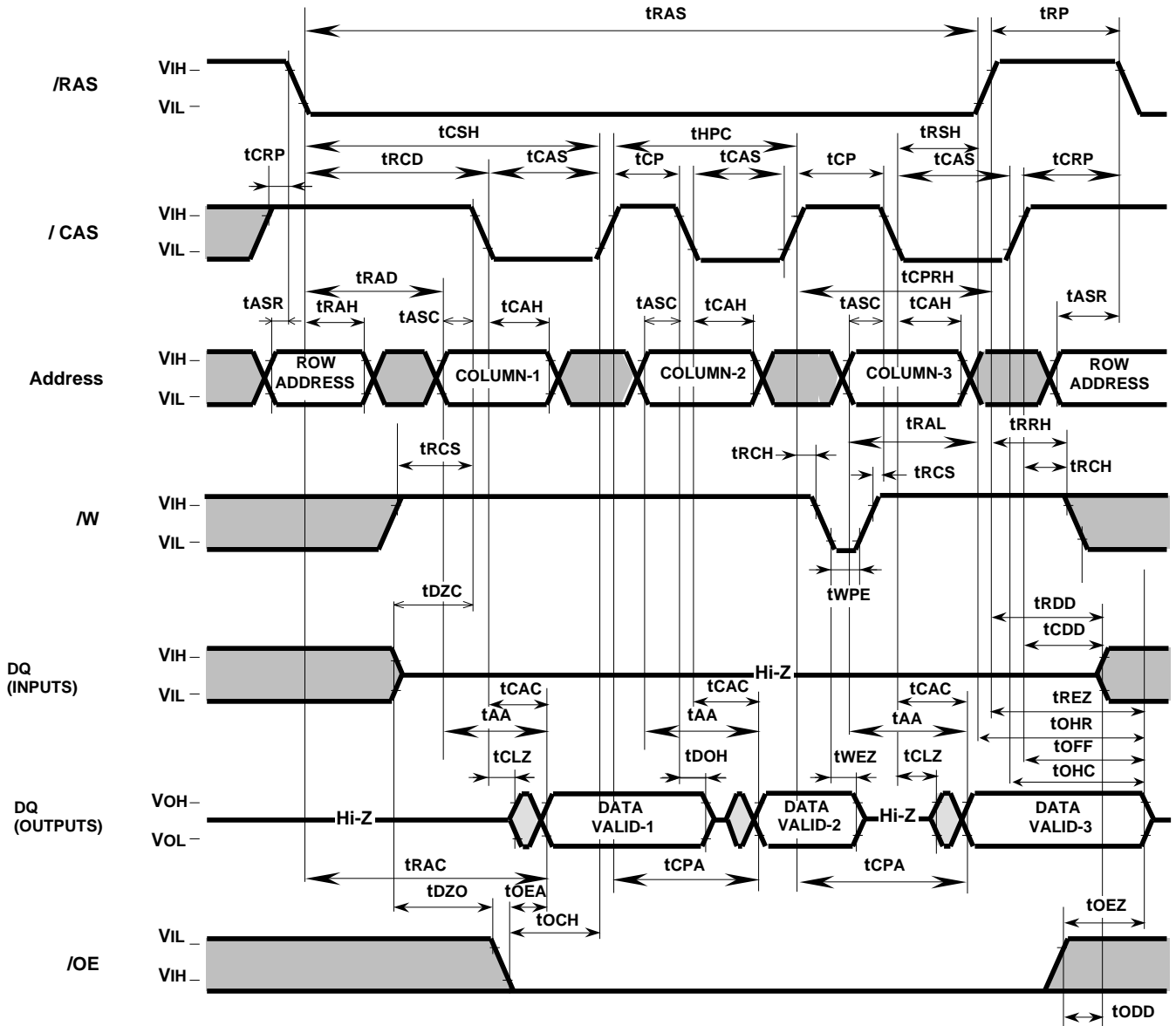
Hyper Page Mode Read Cycle (Hi-Z control by \overline{OE})



MH8V7245BWZTJ -5, -6

HYPER PAGE MODE 603979776 - BIT (8388608 - WORD BY 72 - BIT) DYNAMIC RAM

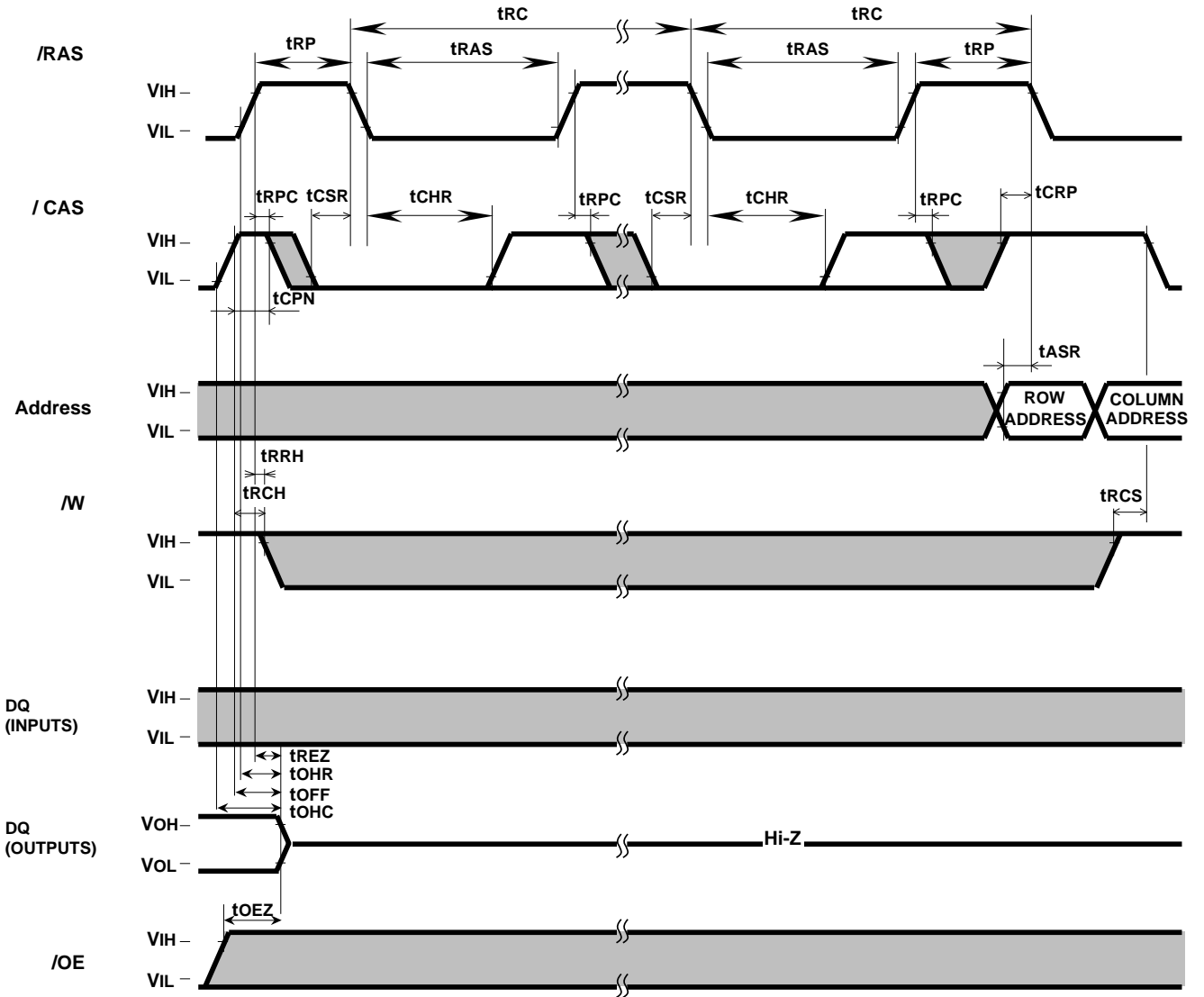
Hyper Page Mode Read Cycle (Hi-Z control by \overline{W})



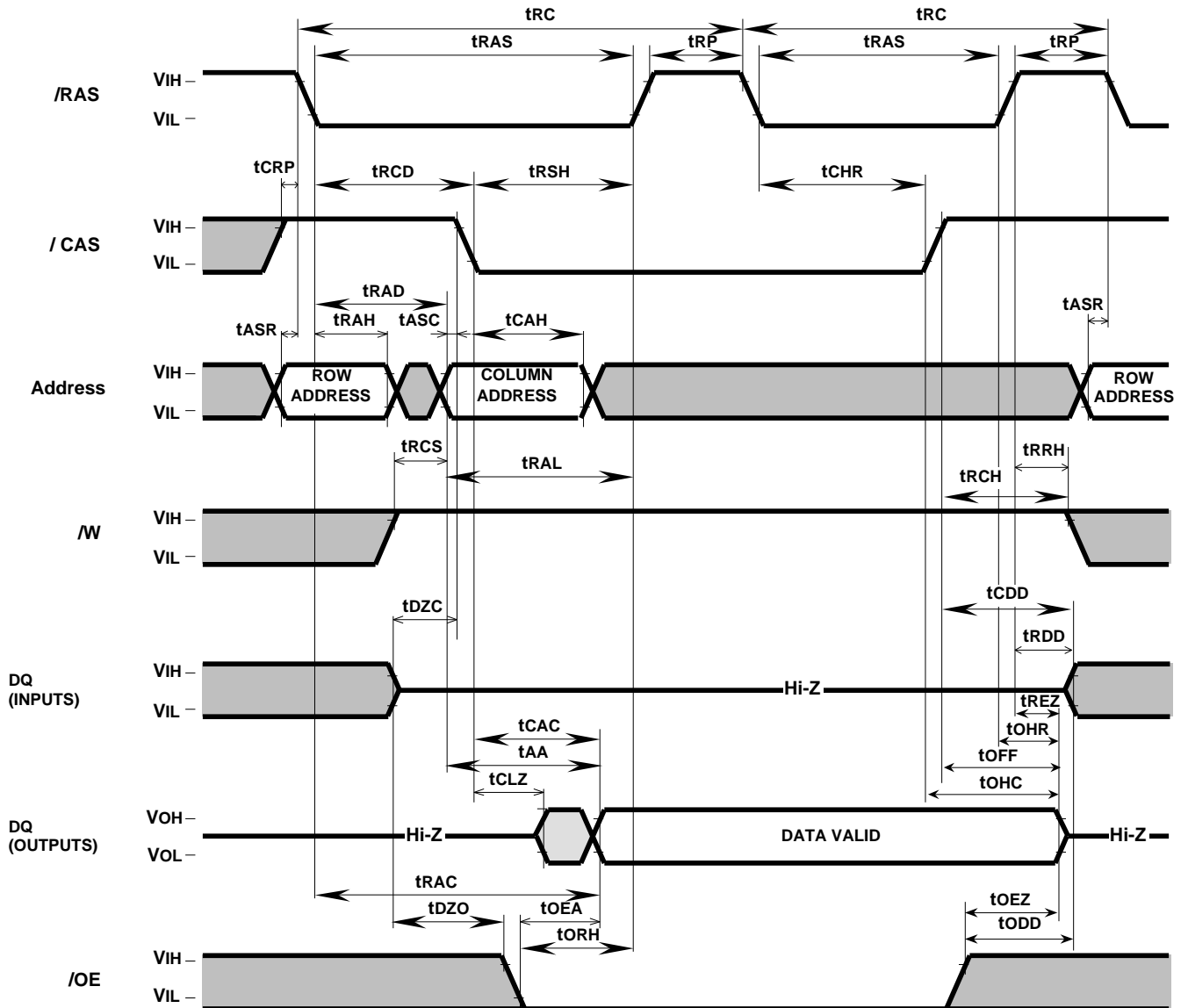
MH8V7245BWZTJ -5, -6

HYPER PAGE MODE 603979776 - BIT (8388608 - WORD BY 72 - BIT) DYNAMIC RAM

/CAS before /RAS Refresh Cycle



Hidden Refresh Cycle (Read) (Note 31)



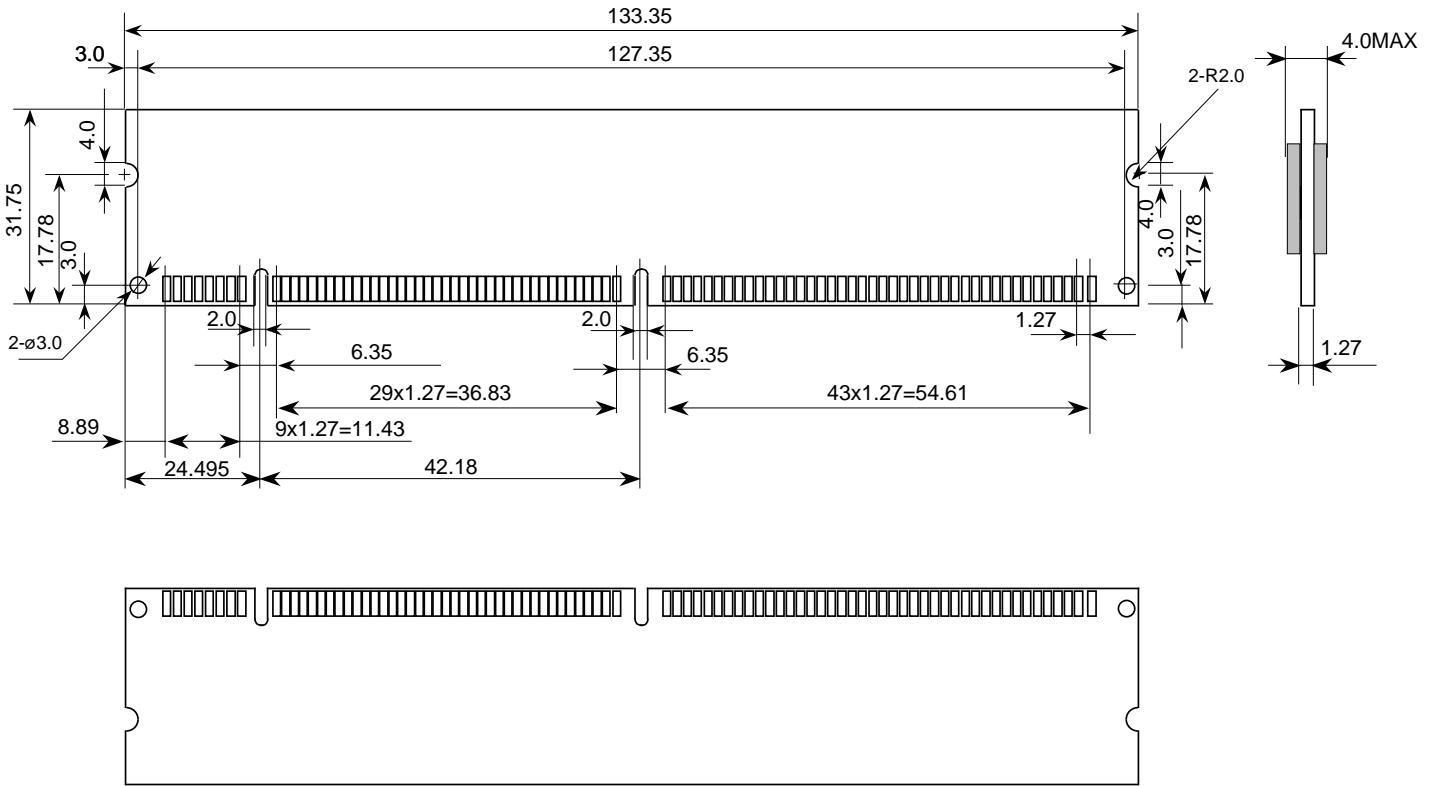
Note 31: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

MH8V7245BWZTJ -5, -6

HYPER PAGE MODE 603979776 - BIT (8388608 - WORD BY 72 - BIT) DYNAMIC RAM

Unit:mm

Package outline



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