JTAG Test Sequencer

Description

The AS91L1002 device provides a solution to perform stand alone IEEE1149.1 tests with out any third party test hardware.

The device executes tests that have been translated from the Serial Vector Format (SVF) to the compact binary format, BVI which is stored in a Flash memory. Upon completion of the test run the user is presented with PASS/FAIL information, thus enabling a high degree of confidence in the operation of the PCB.

The AS91L1002 can be controlled by using one of two different sources: a power-on reset circuit or a front panel switch. Any one of these can cause the AS91L1002 to execute tests that have been loaded into the Flash memory. When the AS91L1002 is running and performing the tests, status lines are fed off chip to enable the user to hold the PCB in a safe state until completion of the tests.

When the tests have completed, the status of the execution is presented off chip through a status line to indicate the PASS/FAIL condition.

Key Features

- Performs IEEE1149.1 tests in standalone mode without any 3rd Party test hardware
- Eliminates the need for firmware development, thereby speeding up time to market
- AS91L1002 can be used to perform self tests on multiple PCBs on a system in parallel
- Pinout and feature set compatible (complete second source) with the Firecron JTS02 device
- Available in a 100-pin LQFP or a 100-pin FPBGA lead free package

Device Block Diagram

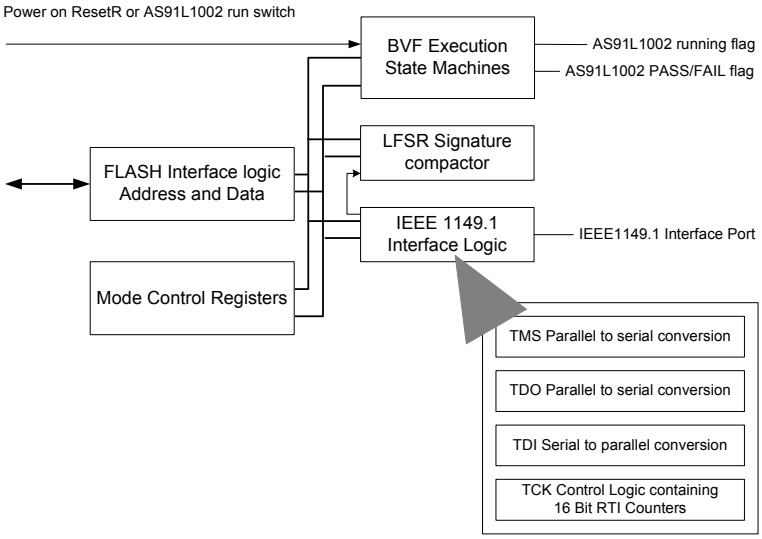


Figure 1 - AS91L1002 JTAG Test Sequencer

BIST Sequencer Power On Operation

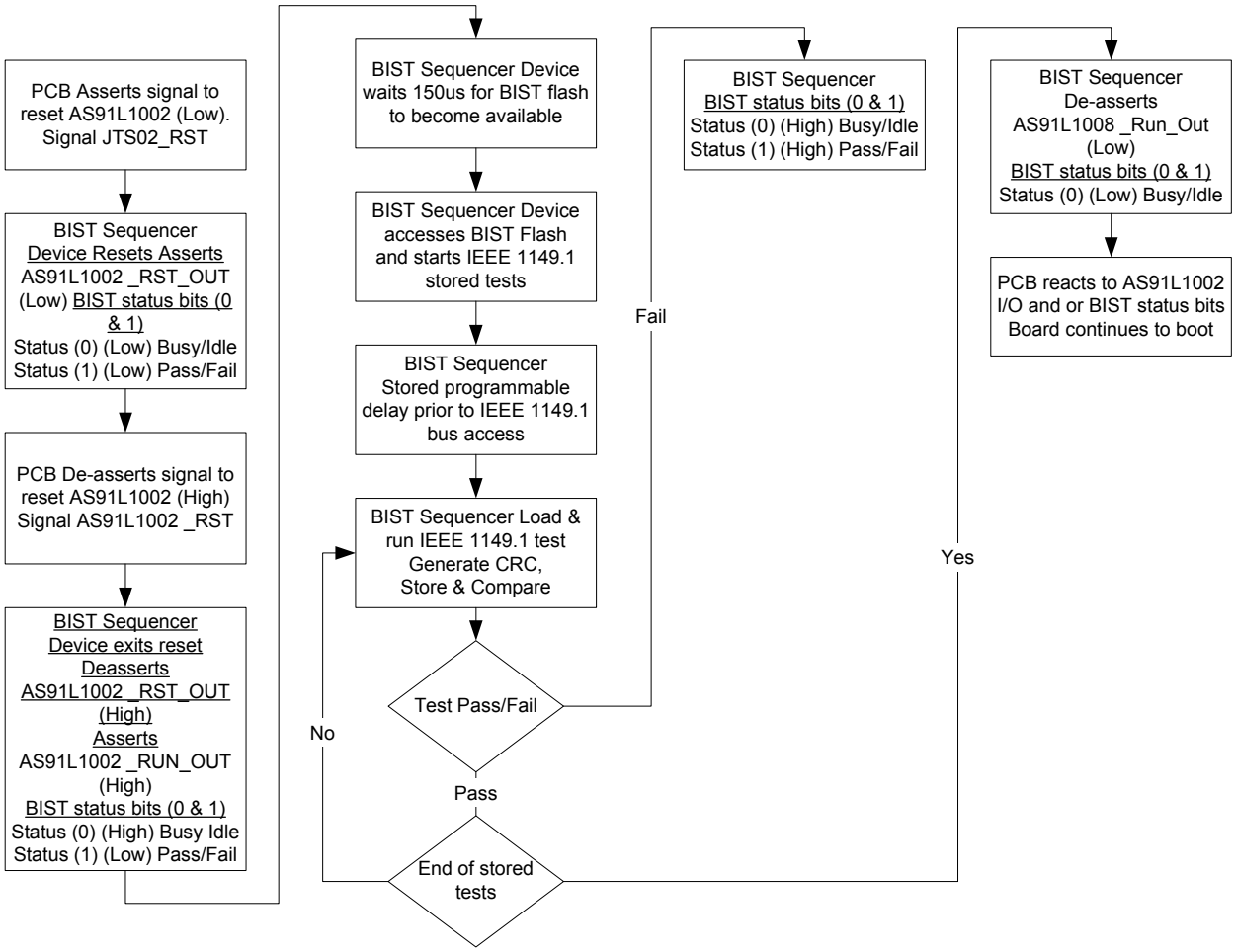


Figure 2 - AS91L1002 Power On Sequence

The AS91L1002 does not require a microprocessor to operate and run IEEE1149.1 tests. It can be used to perform diagnostics on the PCB. In systems with multiple cards, all cards can simultaneously execute self tests without processor intervention, thereby significantly reducing test time. AS91L1002 utilizes IEEE1149.1 tests generated by industry standard ATPG tools, thereby eliminating the need for custom firmware development resulting in faster time to market.

In the AS91L1002, the IEEE1149.1 test preparation is a two-step process. The first step is to convert the industry standard SVF format into the compact Alliance binary BVF file. One or more IEEE1149.1 tests represented as Alliance BVF files can then be further compressed into an Alliance BVI file which is then exported to a binary file for programming into the flash device, and then used by the AS91L1002 for test execution.

The user is able to specify the TCK rate for each individual test execution based on a programmable divider within the AS91L1002, along with a programmable test start delay time based upon the number of TCKs.

These features enable multiple tests to be stored, in the AS91L1002 test flash. It allows each test to operate at different TCK rate, and allows for sufficient settling time before each test starts to ensure that the PCB is in a stable condition.

Signal Description

PIN NAME	PIN NUMBER LQFP	PIN NUMBER FPBGA	DESCRIPTION
TOE	88	B6	Test Output Enable: When this signal is taken to logic '0', all I/O on the device is placed in HighZ.
POR	14	F4	Power on Reset: This signal when taken to logic '0' causes the AS91L1002 to reset. When the signal returns to logic '1' the AS91L1002 starts test execution.
SW_RUN	10	E3	Switch AS91L1002 Run: This signal when taken to logic '0' causes the AS91L1002 to reset. When the signal returns to logic '1' the AS91L1002 starts test execution.
OSC_IN	16	F1	Oscillator Input: Provides the master clock into the AS91L1002, Max freq 66 MHz.
BUSY_IDLE	25	K1	BUSY IDLE: This output indicates the state of the AS91L1002. When High, it indicates that the AS91L1002 is active.
PASS_FAIL	24	J1	PASS FAIL: This output provides status of the test execution. When at logic'1' after test execution the stored IEEE1149.1 test has failed due to data errors.
FLASH_ADD[0..23]	70, 69, 67, 65, 64, 63, ,61, 60, 57, 28, 29, 30, 31, 32, 35, 36, 37, 40, 41, 42, 45, 46, 47, 48	D10, D9, E8, E10, E9, F7, F10, F9, G10, J2, K3, J3, H4, J4, H5, J5, K5, K6, J6, H6, J7, H7, J8, K8	FLASH ADD: These outputs provide the address pins to the flash device that is used to store the IEEE1149.1 tests.
FLASH_DB[0..15]	72, 75, 76, 78, 79, 80, 81, 83, 84, 85, 92, 93, 94, 96, 97, 98	C9, C10, B10, A9, A8, B8, A7, B7, C7, C6, C5, C4, B4, A4, B3, A3	FLASH DB: These inputs provide the stored IEEE1149.1 test data within the flash device to the AS91L1002 sequencer.
FLASH_RD	50	K10	FLASH READ: This output provides an active '0' signal to indicate that the AS91L1002 wishes to read data from the flash device.
TRST	22	H2	TRST: This output signal provides the IEEE1149.1 TRST signal for the devices to be tested.
TMS	21	G2	TMS: This output signal provides the IEEE1149.1 TMS signal for the devices to be tested.
TCK	87	A6	TCK: This output signal provides the IEEE1149.1 TCK signal for the devices to be tested. The clock frequency is based upon the frequency of oscillator to the AS91L1002 and is programmable for each tests execution.

PIN NAME	PIN NUMBER LQFP	PIN NUMBER FPBGA	DESCRIPTION
TDO	20	G1	TDO: This output signal provides the IEEE1149.1 data for the devices to be tested. It should be connected to the TDI pin on the first device in the IEEE1149.1 chain.
TDI	19	G3	TDI: This input signal receives the IEEE1149.1 data from the devices to be tested. It should be connected to the TDO pin on the last device in the IEEE1149.1 chain.
DEVICE_TCK	62	F8	Silicon TAP Port Signal
DEVICE_TDI	4	A1	Silicon TAP Port Signal
DEVICE_TDO	73	A10	Silicon TAP Port Signal
DEVICE_TMS	15	F3	Silicon TAP Port Signal
Signal Ground	55,56, 89, 38, 86, 11, 26, 43, 59, 74, 95, 2, 17, 90	J9,G9,B5, D6, G5, C3, D7, E5, F6, G4,H8, A5, F2, B1	
3.3 V Supply	39, 91,23, 3, 18, 34, 51, 66, 82,54	H9, C8, D4, E6, F5, G7, H3, H1, D5, G6	

Table 1 - Signal Description

Signal Functions

Signal Name	Signal Function
TRST	TRST: This output signal provides the IEEE1149.1 TRST signal for the devices to be tested.
TOE	Test Output Enable: When this signal is taken to logic ‘0’ all I/O on the device is placed in HighZ.
TMS	TMS: This output signal provides the IEEE1149.1 TMS signal for the devices to be tested.
TDO	TDO: This output signal provides the IEEE1149.1 data for the devices to be tested. It should be connected to the TDI pin on the first device in the IEEE1149.1 chain.
TDI	TDI: This input signal receives the IEEE1149.1 data from the devices to be tested. It should be connected to the TDO pin on the last device in the IEEE1149.1 chain.
TCK	TCK: This output signal provides the IEEE1149.1 TCK signal for the devices to be tested. The clock frequency is based upon the frequency of oscillator to the AS91L1002 and is programmable for each tests execution.
SW_RUN	Switch AS91L1002 Run: This signal when taken to logic ‘0’ causes the AS91L1002 to reset. When the signal returns to logic ‘1’ the AS91L1002 starts test execution.
RST_OUT	RESET OUT: This output signal pulses low before the start of each test execution. It is used to reset the Flash device to ensure that they are in a stable state before the AS91L1002 access the stored data.
POR	Power on Reset: This signal when taken to logic ‘0’ causes the AS91L1002 to reset. When the signal returns to logic ‘1’ the AS91L1002 starts test execution.
PASS_FAIL	PASS FAIL: This output provides status of the test execution. When at logic’1’ after test execution, the stored IEEE1149.1 test has failed due to data errors.
OSC_IN	Oscillator Input: Provides the master clock into the AS91L1002, Max freq 66 MHz.
FLASH_RD	FLASH READ: This output provides an active ‘0’ signal to indicate that the AS91L1002 wishes to read data from the flash device.
FLASH_DB[0..15]	FLASH DB: These inputs provide the stored IEEE1149.1 test data within the flash.
FLASH_ADD[0..23]	FLASH ADD: These outputs provide the address pins to the flash device that is used to store the IEEE1149.1 tests.
BUSY_IDLE	BUSY IDLE: This output indicates the state of the AS91L1002. When High, it indicates the AS91L1002 is active.

Table 2 - Signal Functions

Absolute Maximum Ratings

Parameter	Maximum Range
Supply Voltage (Vcc)	-0.3V to 5.5V
DC Input Voltage (Vi)	-0.5V to Vcc +0.5V
Max sink current when Vi = -0.5V	-20mA
Max source current when Vi = Vcc + 0.5V	+20mA
Max Junction Temperature with power applied Tj	+125 degrees C
Max Storage temperature	-55 to +150 degree C

Table 3 - Absolute Maximum Ratings

Note: Stress above the stated maximum values may cause irreparable damage to the device, correct operation of the device at these values is not guaranteed.

Recommended Operating Conditions

Parameter	Operating Range
Supply Voltage (Vcc)	3.0V to 3.6V
Input Voltage (Vi)	0V to Vcc
Output Voltage (Vo)	0V to Vcc
Operating Temperature (Ta) Commercial	0 C to 70 C
Industrial (Ta)	-40 deg C to +85 deg C, 3.00V to 3.6V

Table 4 - Recommended Operating Conditions

DC Electrical Characteristics

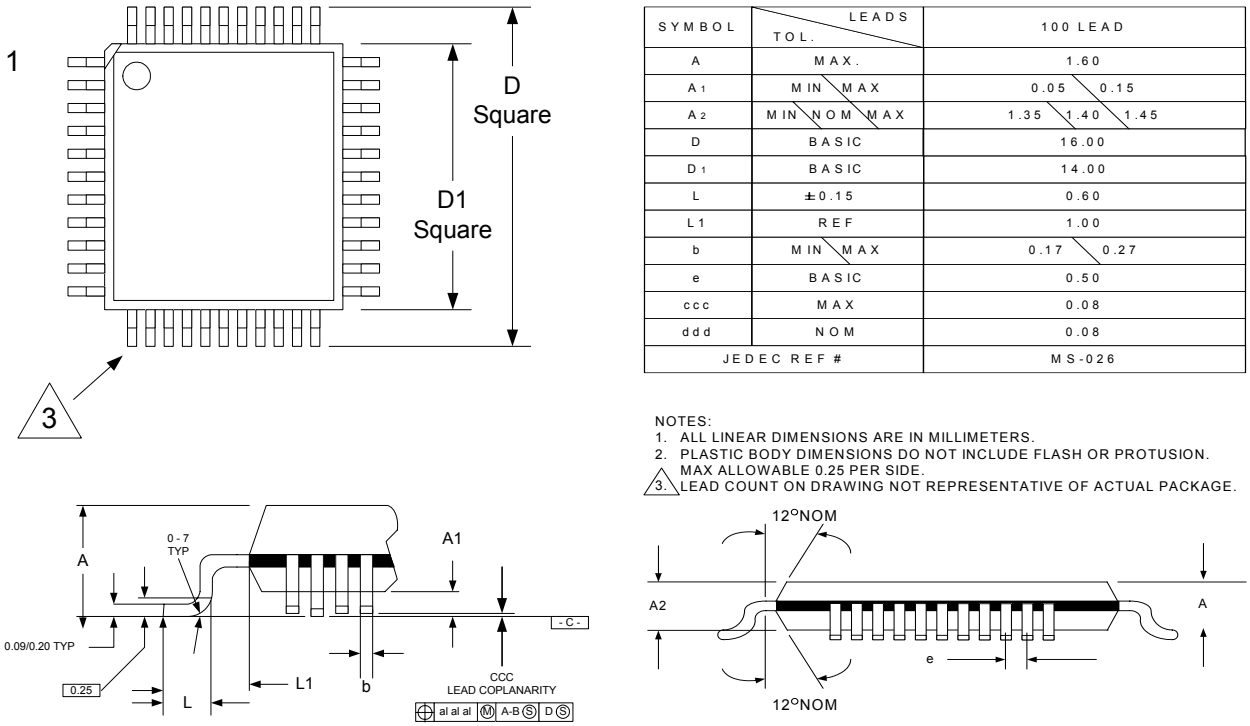
Symbol	Parameter	Min	Max	Condition
V_{IH}	Minimum High Input Voltage	2.0	5.25	
V_{IL}	Maximum Low Input Voltage	-0.3V	0.8V	
Symbol	**Parameter**		**Value**	**Condition**
V_{OH}	Minimum High Output Voltage		2.4V	Ioh=24mA or 8mA as defined by pin
V_{OL}	Minimum Low Output Voltage		0.4V	Iol=24mA or 8mA as defined by pin
I_{oz}	Tristate output leakage		-10 or 10 mA	

Symbol	Parameter	Min	Max	Condition
I_{cc}	Maximum quiescent supply current		2mA	
I_{ccd}	Maximum dynamic supply current		80mA	TCK freq equal to 10 MHz

Table 5 - AS91L1002 DC Electrical Characteristics

Packaging Information

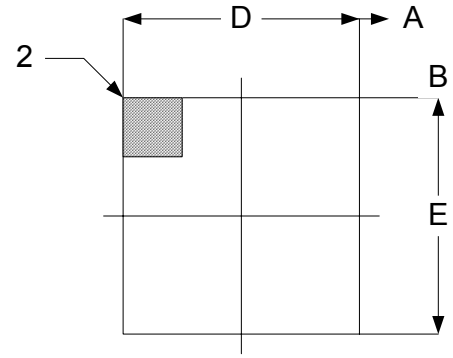
The AS91L1002 is available in a 100-pin LQFP or a 100-pin FPBGA lead free package.



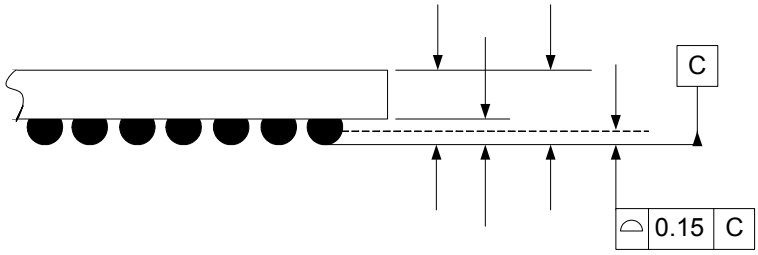
SYMBOL	LEADS / TOL.	100 LEAD
A	MAX.	1.60
A1	MIN / MAX	0.05 / 0.15
A2	MIN / NOM / MAX	1.35 / 1.40 / 1.45
D	BASIC	16.00
D1	BASIC	14.00
L	±0.15	0.60
L1	REF	1.00
b	MIN / MAX	0.17 / 0.27
e	BASIC	0.50
ccc	MAX	0.08
ddd	NOM	0.08
JEDEC REF #		MS-026

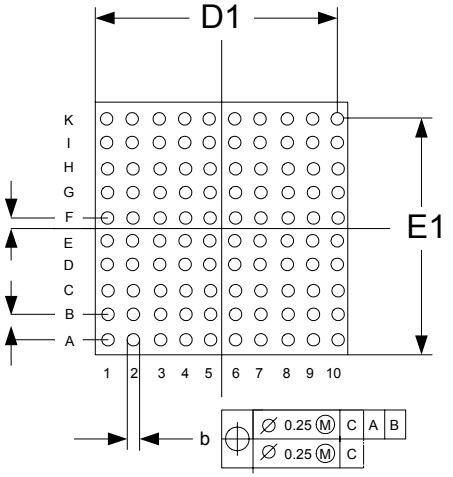
NOTES:
1. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
2. PLASTIC BODY DIMENSIONS DO NOT INCLUDE FLASH OR PROTUSION. MAX ALLOWABLE 0.25 PER SIDE.
3. LEAD COUNT ON DRAWING NOT REPRESENTATIVE OF ACTUAL PACKAGE.

Figure 4 - LQFP-100



Revisions			
REV.	DESCRIPTION	ECN	DATE
A	Initial document release.	91253	12-04-01
B	Updated ball coplanarity limits from 0.20mm to 0.15mm.		





DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	--	--	1.70
A1	0.30	--	--
A2	0.25	--	1.10
b	0.50	0.60	0.70
D	11.00 BSC		
D1	9.00 BSC		
E	11.00 BSC		
E1	9.00 BSC		
e	1.00		
PACKAGE NUMBER	FBGA0100-11F		
JEDEC REF #	MO-192 VAR. AAC-1		

Figure 5 - FPBGA-100

Device Selector Guide and Ordering Information

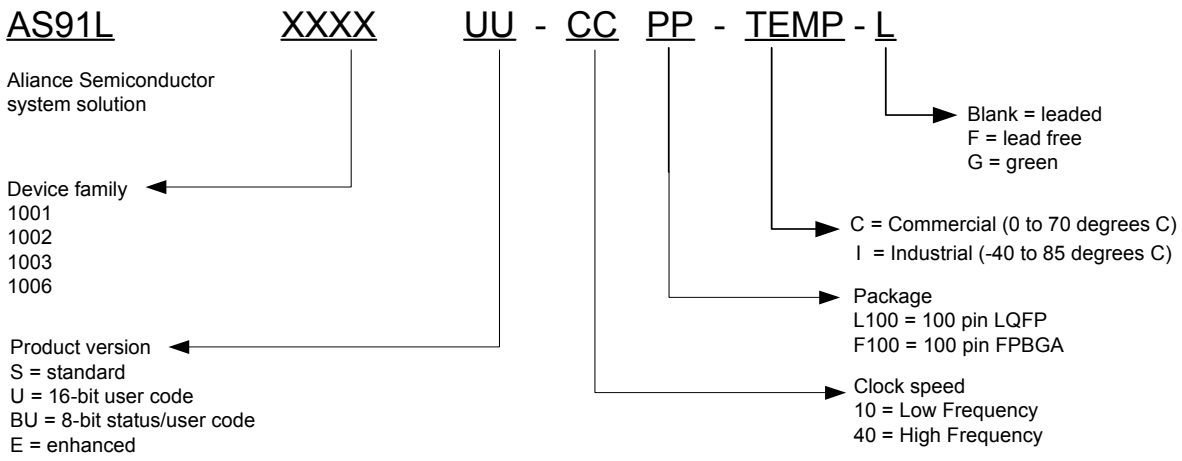


Figure 6 - Part Numbering Guide

Part Number	Description	Availability
AS91L1002S – 10L100-C	JTAG Test Sequencer, 100-pin LQFP package, commercial	now
AS91L1002S – 10L100-I	JTAG Test Sequencer, 100-pin LQFP package, industrial	now
AS91L1002S – 10F100-C	JTAG Test Sequencer 100-pin FPBGA package, commercial	Please Contact Alliance Semiconductor
AS91L1002S – 10F100-I	JTAG Test Sequencer 100-pin FPBGA package, industrial	Please Contact Alliance Semiconductor

Table 6 - Valid Part Number Combination

Device Master	Description	Package Options	
		FPBGA-100 (1mm pitch)	LQFP-100
AS91L1001	JTAG Test Controller	x	x
AS91L1002	JTAG Test Sequencer	x	x
AS91L1003U	3-Port Gateway	x	x
AS91L1006BU	6-Port Gateway	x	x

Table 7 - JTAG Controller Product Family