Application Note

TECHNICAL CONSIDERATIONS FOR MIGRATING CS5460-BASED DESIGN TO CS5460A-BASED DESIGN

1. INTRODUCTION

This application note briefly describes several minor functional differences between the CS5460 and the CS5460A. These functional differences may need to be considered by a designer when attempting to use the CS5460A as a drop-in replacement for the CS5460 (in a CS5460-based design). The CS5460 and CS5460A are pin-to-pin compatible devices, manufactured in the same SSOP package. Under default operating conditions (just after initial power on), the CS5460A is functionally equivalent to the CS5460, with the exception of the functional differences listed in this document. Any adjustments that may need to be made to a CS5460-based design, in order to accommodate CS5460A as a drop-in replacement for CS5460, are usually very minor. In most cases, no adjustments will be necessary at all. For more detailed information about these functional differences, e-mail customer support at: **powermeter@crystal.cirrus.com**.

2. SUMMARY OF DIFFERENCES

1) Frequency of pulses issued from the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins, during a "burst" of output pulses, is twice the frequency of the pulse burst frequency of the CS5460.

2) Pulse duration of the pulses issued from the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins, during a "burst" of output pulses, is ½ of CS5460's pulse duration (for a given Pulse-Rate Register setting).

3) The "B2" bit position, in the 8-bit Calibration Command, could be set to either logic "1" or logic "0" in the CS5460, with no change in the calibration sequence that is to be executed. In the CS5460A, this bit setting is relevant to the particular type of calibration sequence that will be executed.

4) The "RMS Overflow" Error that existed in the CS5460 does not exist in the CS5460A. Therefore, the designer can (if desired) often increase the accuracy and/or linearity and/or dynamic range available for the voltage, current, power, energy results, *if* provisions had specifically been made in the original CS5460 design to avoid the RMS Overflow situation. However, such a revision is *not* mandatory.

5) Pin #8 of the CS5460 has no functionality, but pin #8 *does* have functionality on the CS5460A. If the designer left pin #8 as a "No Connect" or if pin #8 was grounded in the original CS5460-based design, then no circuit change is necessary when replacing CS5460 with CS5460A.

6) For both the CS5460 and CS5460A, there is a slight time shift imposed between the voltage and current waveforms, due to the A/D conversion process. In the CS5460, the effective time shift imposed on the input voltage signal (with respect to the input current signal) is ~9.3 µs when the phase compensation bits (PC bits) are at the default setting of "0000". In the CS5460A, this time shift is reduced to ~1.0 µs when the PC bits are at the default setting of "0000000". Also, as the reader can see, the number of PC bits has changed from 4 to 7. Also, the amount of time shift per PC bit was changed to ~1.85 µs per bit.

SMART
Analog™