Precision Low Power Single-Supply JFET Amplifier

AD8627*

FEATURES

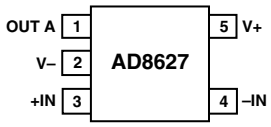
SC70 Package
Very Low I_B: 1 pA Max
Single-Supply Operation: 5 V to 26 V
Dual-Supply Operation: ±2.5 V to ±13 V
Rail-to-Rail Output
Low Supply Current: 630 μA Typ
Low Offset Voltage: 500 μV Max
Unity Gain Stable
No Phase Reversal

APPLICATIONS

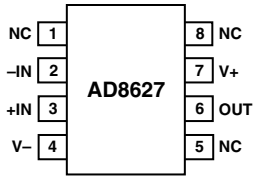
Photodiode Amplifier
ATE
Line Powered/Battery Powered Instrumentation
Industrial Controls
Automotive Sensors
Precision Filters
Audio

PIN CONFIGURATIONS

5-Lead SC70
(KS Suffix)



8-Lead SOIC
(RN Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The AD8627 is a precision JFET input amplifier. It features true single-supply operation, low power consumption, and rail-to-rail output. The outputs remain stable with capacitive loads of over 500 pF; the supply current is less than 630 μA. Applications for the AD8627 include photodiode transimpedance amplification, ATE reference level drivers, battery management, both line powered and portable instrumentation, and remote sensor signal conditioning including automotive sensors.

The AD8627's ability to swing nearly rail-to-rail at the input and rail-to-rail at the output enables it to be used to buffer CMOS DACs, ASICs, and other wide output swing devices in single-supply systems.

The 5 MHz bandwidth and low offset are ideal for precision filters.

The AD8627 is fully specified over the extended industrial (–40°C to +125°C) temperature range and is available in both 5-lead SC70 and 8-lead SOIC surface mount packages. The SC70 packaged parts are available in tape and reel only.

REV. 0

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AD8627–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@V_S = 5 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.05	0.5	mV
		–40°C < T_A < +125°C			1	mV
Input Bias Current	I_B			0.25	1	pA
		–40°C < T_A < +125°C			500	pA
Input Offset Current	I_{OS}				0.5	pA
		–40°C < T_A < +125°C			25	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.5 V	66	87		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to 4.5 V	100	230		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		4.96			V
		I_L = 2 mA, –40°C < T_A < +125°C	4.90			V
Output Voltage Low	V_{OL}				0.04	V
		I_L = 2 mA, –40°C < T_A < +125°C			0.08	V
Output Current	I_{OUT}			±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 5 V to 26 V	80	104		dB
Supply Current	I_{SY}			630	800	µA
		–40°C < T_A < +125°C			800	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			5		V/µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	$Ø_O$			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.9		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		17.5		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.4		fA/$\sqrt{Hz}$

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@V_S = ±13 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.35	0.75	mV
		–40°C < T_A < +125°C			1.75	mV
Input Bias Current	I_B			0.25	1	pA
		–40°C < T_A < +125°C			500	pA
Input Offset Current	I_{OS}				0.5	pA
		–40°C < T_A < +125°C			25	pA
Input Voltage Range			–13		+11	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –13 V to +10 V	76	105		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = –11 V to +11 V	150	310		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		+12.96			V
	V_{OH}	I_L = 2 mA, –40°C to +125°C	+12.92			V
Output Voltage Low	V_{OL}				–12.96	V
	V_{OL}	I_L = 2 mA, –40°C to +125°C			–12.92	V
Output Current	I_{OUT}			±15		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±13 V	80	104		dB
Supply Current	I_{SY}			710	900	µA
		–40°C < T_A < +125°C			900	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			5		V/µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	$Ø_O$			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n	f = 1 kHz		0.5		fA/$\sqrt{\text{Hz}}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 27 V
Input Voltage . . . . . V_{S-} to V_{S+}
Differential Input Voltage . . . . . ±Supply Voltage
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
RN Package . . . . . –65°C to +125°C
Operating Temperature Range . . . . . –40°C to +125°C
Junction Temperature Range
RN Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

*Absolute maximum ratings apply at 25°C, unless otherwise noted.

Package Type	θ_{JA}*	θ_{JC}	Unit
5-Lead SC70 (KS)	376	126	°C/W
8-Lead SOIC (RN)	158	43	°C/W

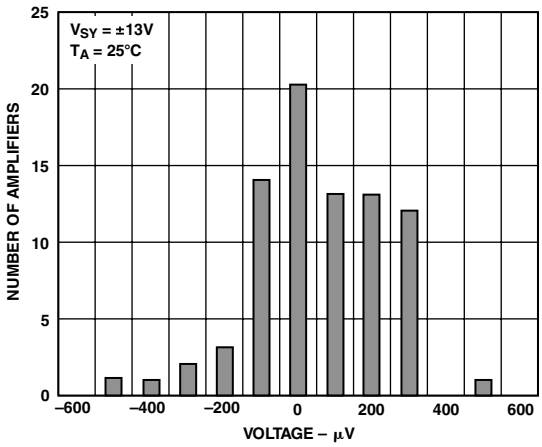
*θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface mount packages.

ORDERING GUIDE

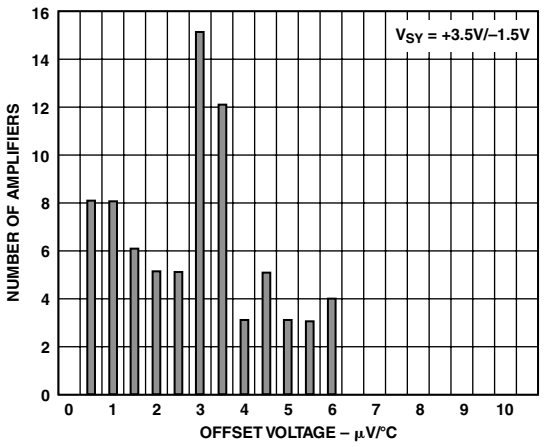
Model	Temperature Range	Package Description	Package Option	Branding Information
AD8627AKS-Reel	–40°C to +125°C	5-Lead SC70	KS-5	B9A
AD8627AKS-Reel7	–40°C to +125°C	5-Lead SC70	KS-5	B9A
AD8627AR	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8627AR-Reel	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8627AR-Reel7	–40°C to +125°C	8-Lead SOIC	RN-8	

CAUTION

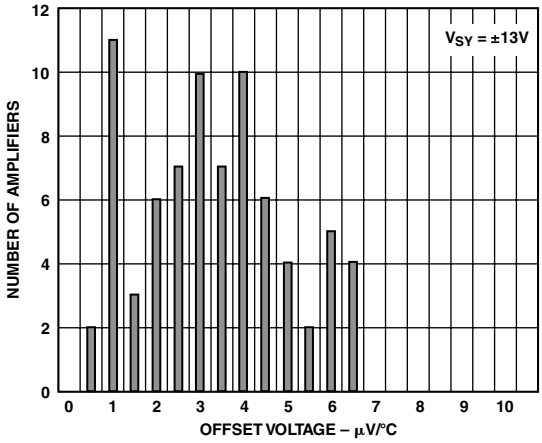
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8627 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



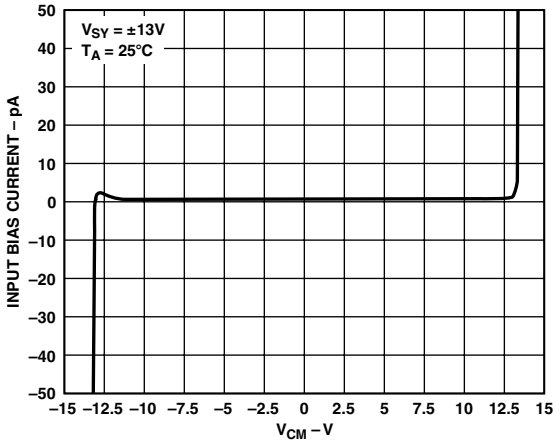
TPC 1. Input Offset Voltage



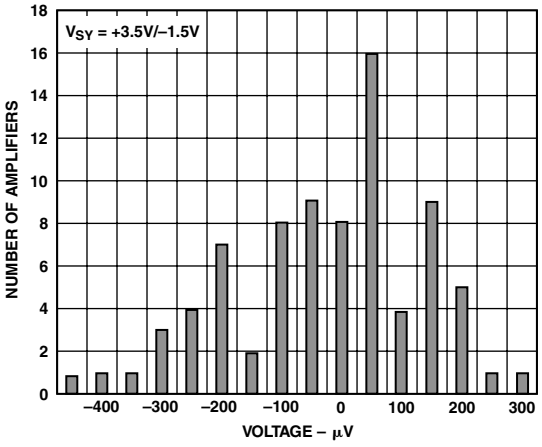
TPC 4. Offset Voltage Drift



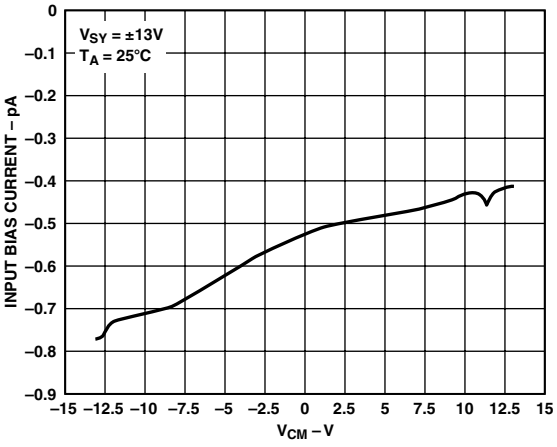
TPC 2. Offset Voltage Drift



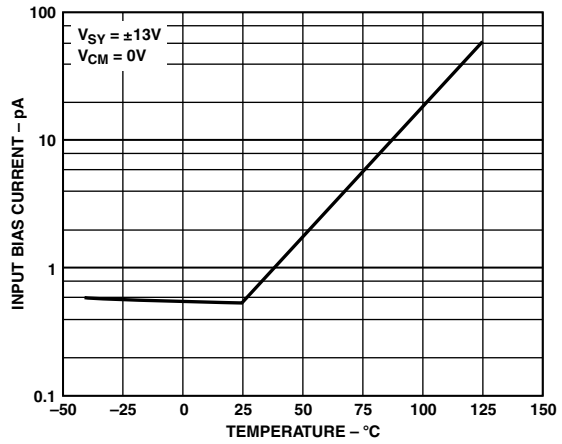
TPC 5a. Input Bias Current vs. V_{CM}



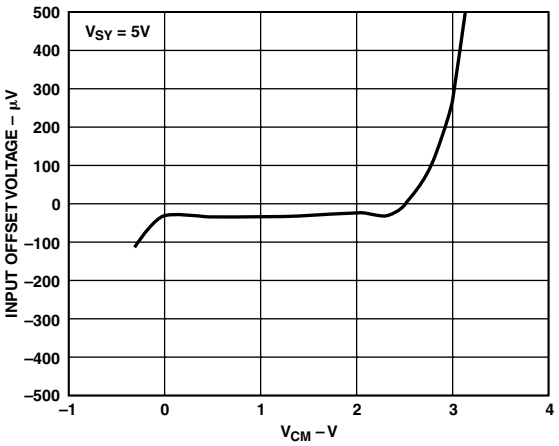
TPC 3. Input Offset Voltage



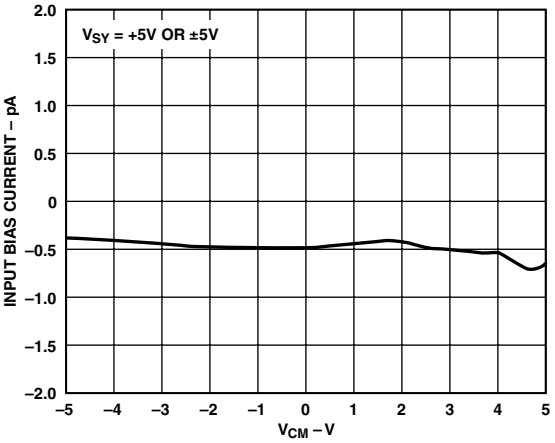
TPC 5b. Input Bias Current vs. V_{CM}



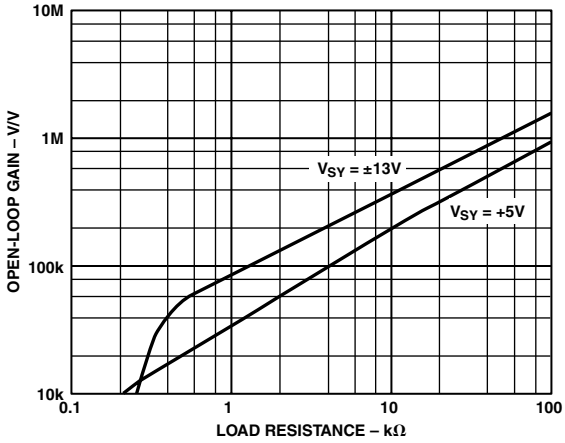
TPC 6. Input Bias Current vs. Temperature



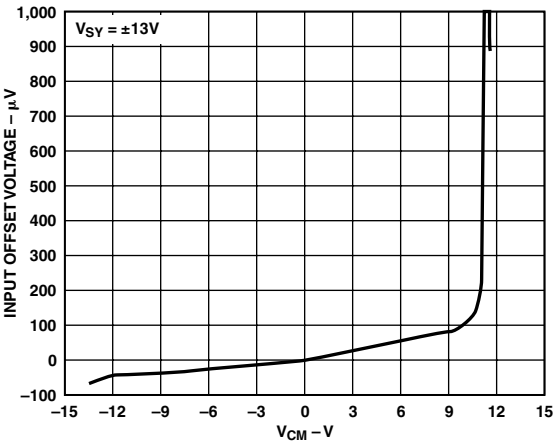
TPC 9. Input Offset Voltage vs. V_{CM}



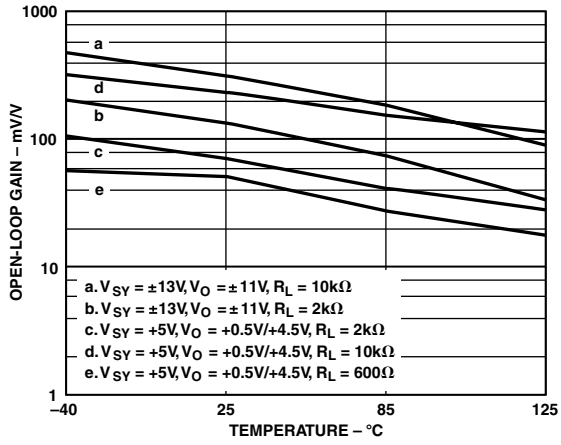
TPC 7. Input Bias Current vs. V_{CM}



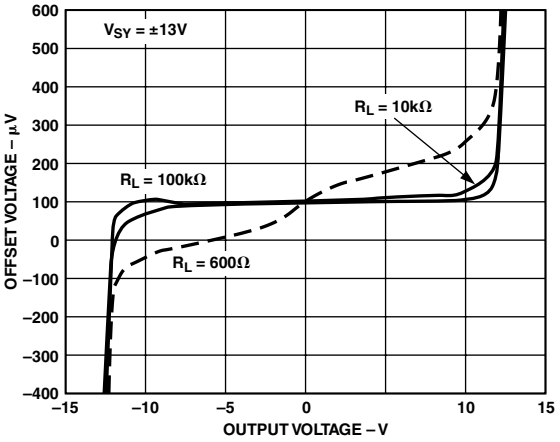
TPC 10. Open-Loop Gain vs. Load Resistance



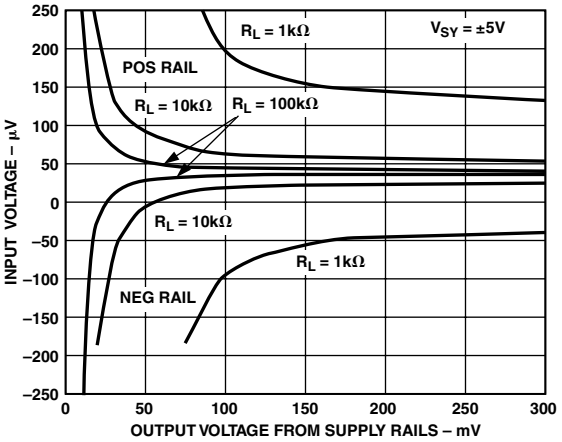
TPC 8. Input Offset Voltage vs. V_{CM}



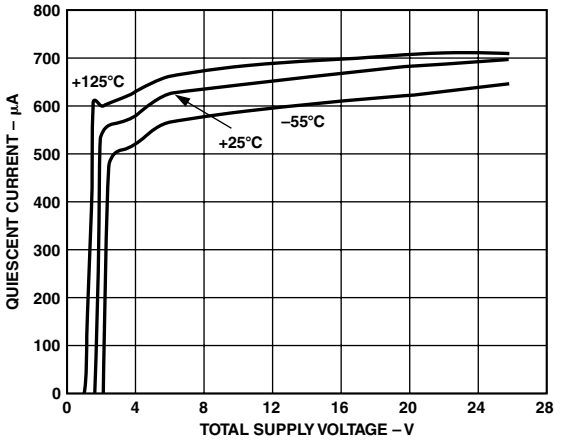
TPC 11. Open-Loop Gain vs. Temperature



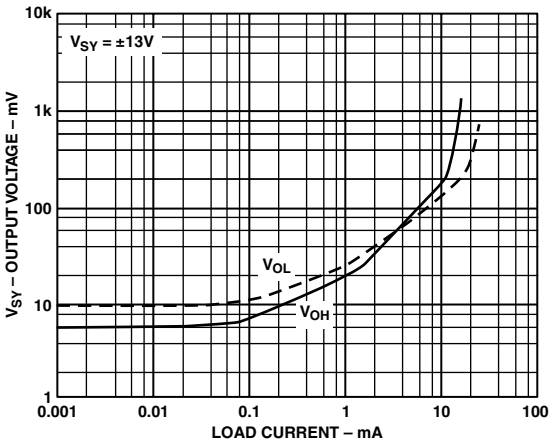
TPC 12. Input Error Voltage vs. Output Voltage for Resistive Loads



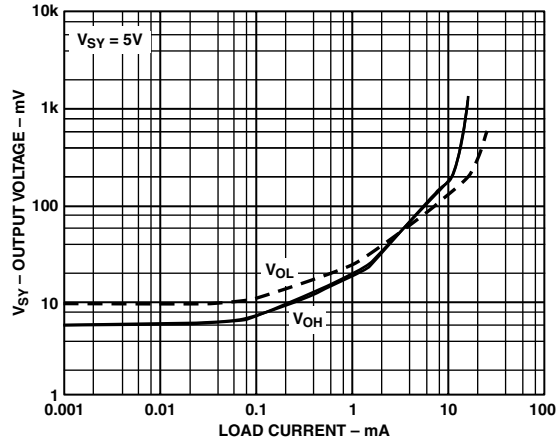
TPC 13. Input Error Voltage vs. Output Voltage within 300 mV of Supply Rails



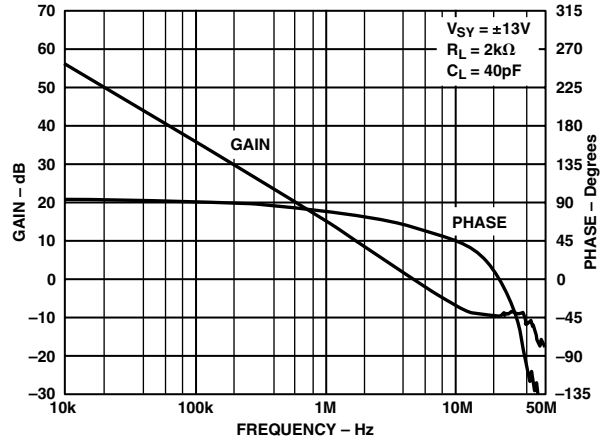
TPC 14. Quiescent Current vs. Supply Voltage at Different Temperatures



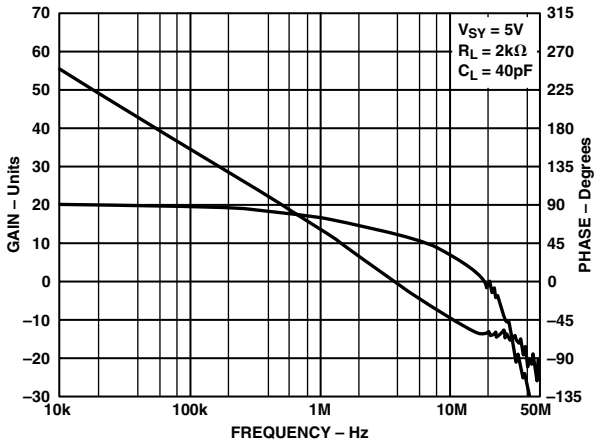
TPC 15. Output Saturation Voltage vs. Load Current



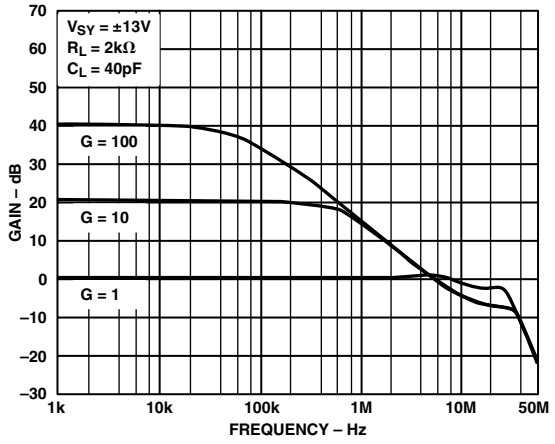
TPC 16. Output Saturation Voltage vs. Load Current



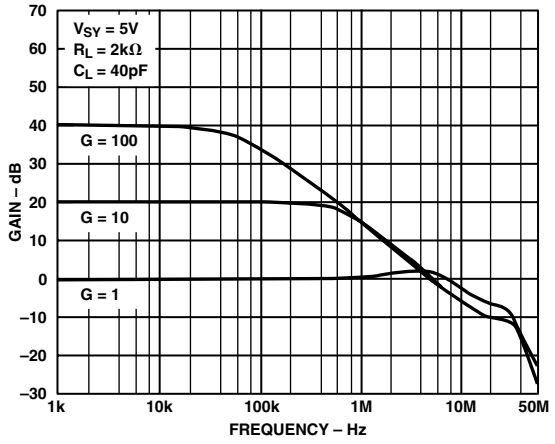
TPC 17. Open-Loop Gain and Phase Margin vs. Frequency



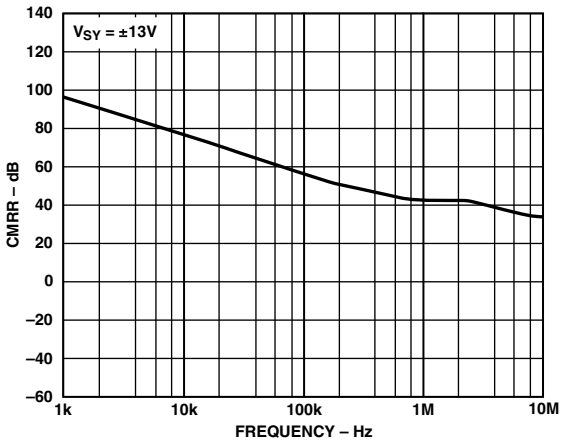
TPC 18. Open-Loop Gain and Phase Margin vs. Frequency



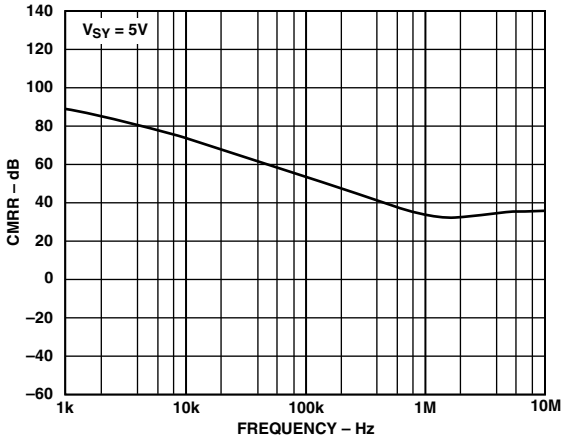
TPC 19. Closed-Loop Gain vs. Frequency



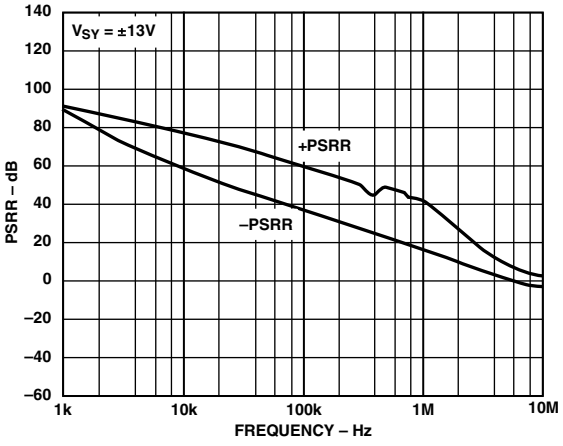
TPC 20. Closed-Loop Gain vs. Frequency



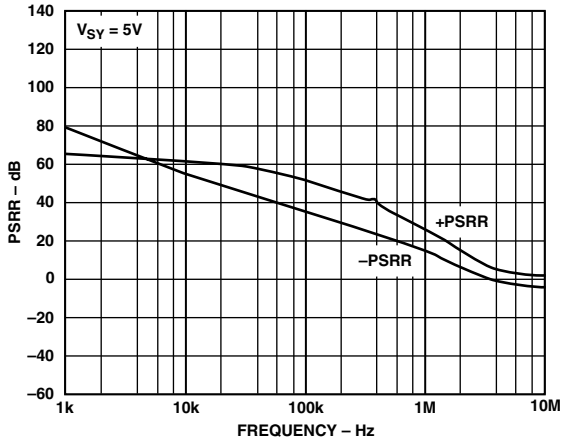
TPC 21. CMRR vs. Frequency



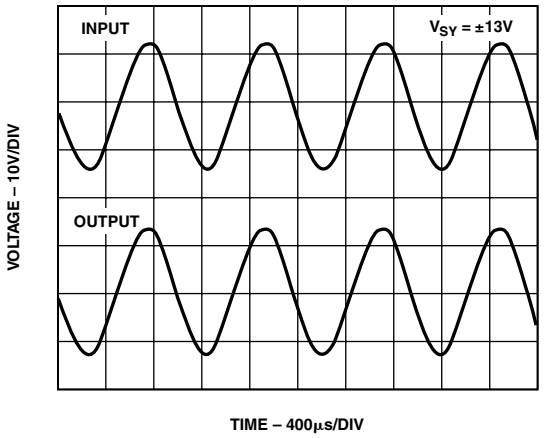
TPC 22. CMRR vs. Frequency



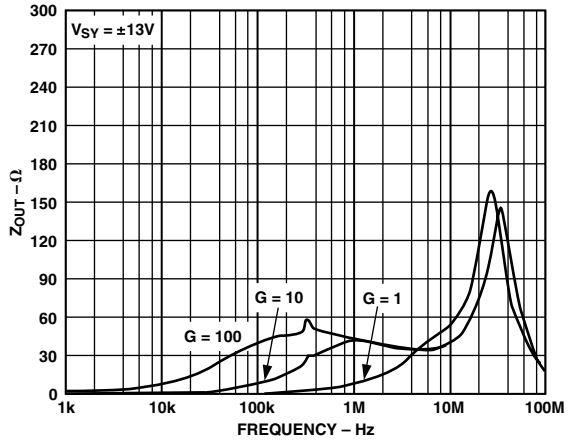
TPC 23. PSRR vs. Frequency



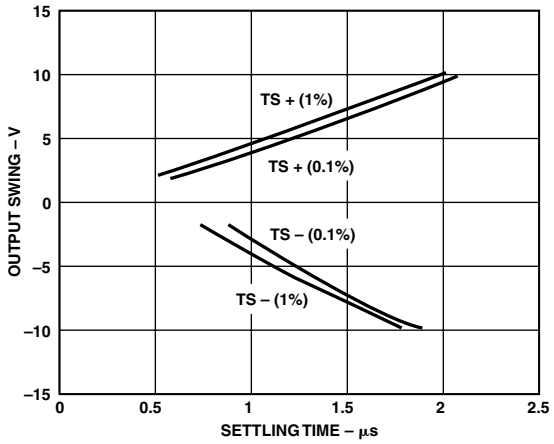
TPC 24. PSRR vs. Frequency



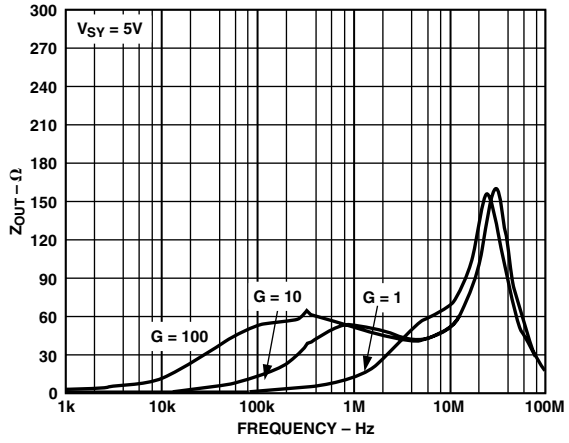
TPC 27. No Phase Reversal



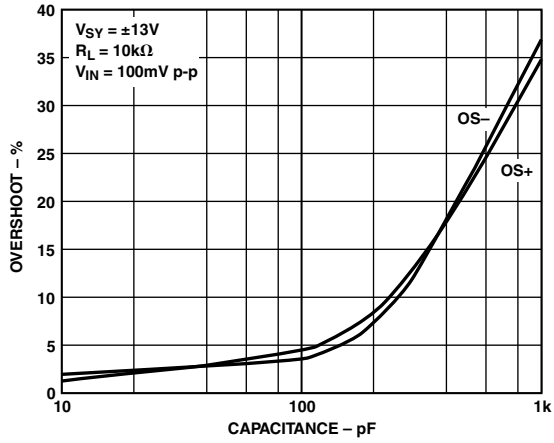
TPC 25. Output Impedance vs. Frequency



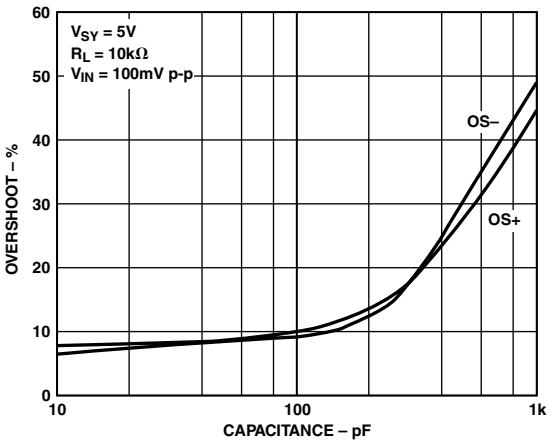
TPC 28. Output Swing and Error vs. Settling Time



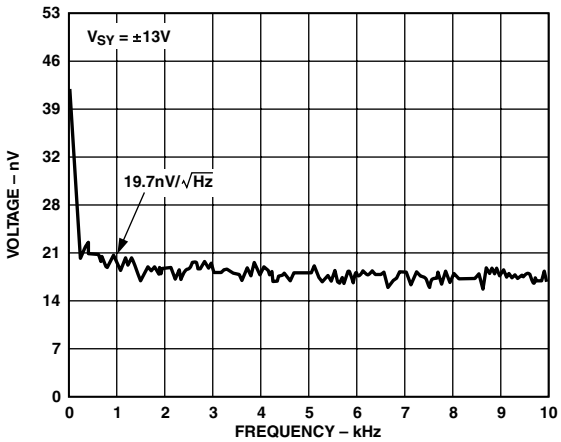
TPC 26. Output Impedance vs. Frequency



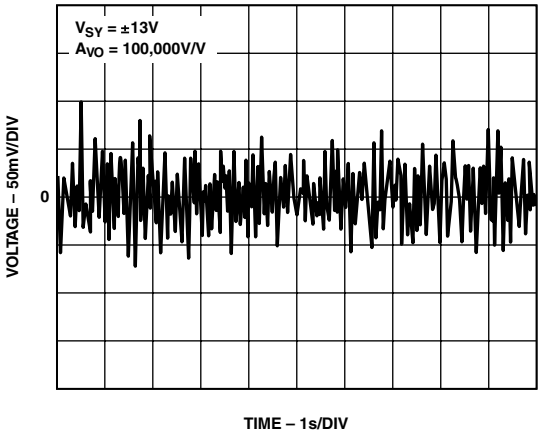
TPC 29. Small Signal Overshoot vs. Load Capacitance



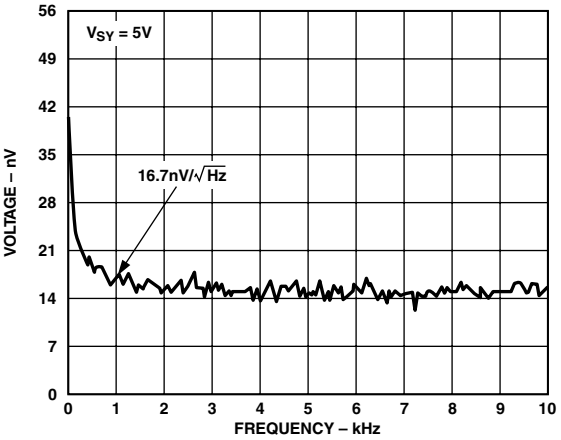
TPC 30. Small Signal Overshoot vs. Load Capacitance



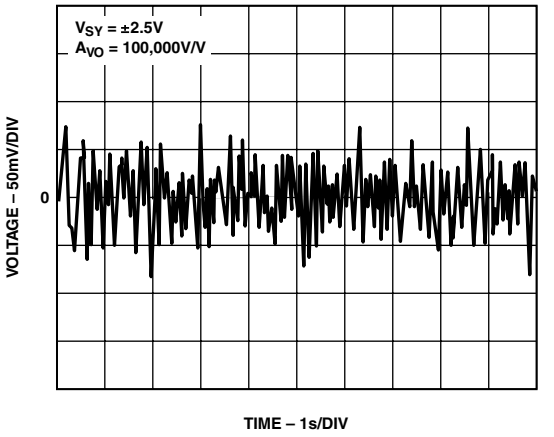
TPC 33. Voltage Noise Density



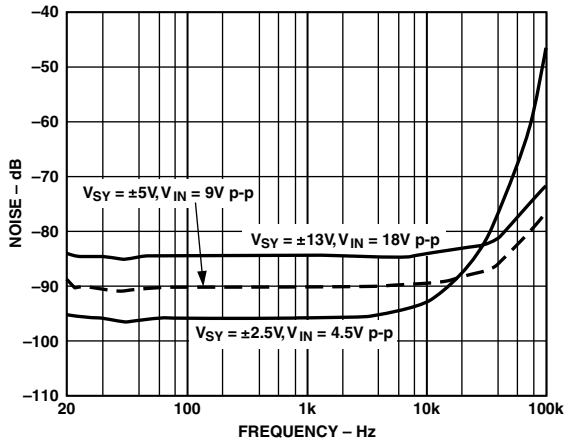
TPC 31. 0.1 Hz to 10 Hz Noise



TPC 34. Voltage Noise Density



TPC 32. 0.1 Hz to 10 Hz Noise



TPC 35. Total Harmonic Distortion + Noise vs. Frequency

APPLICATIONS

The AD8627 is one of the smallest and lowest cost JFETs offered. It has true single-supply capability and has an input voltage range that extends below the negative rail, allowing the part to accommodate input signals below ground. The rail-to-rail output of the AD8627 provides the maximum dynamic range in many applications. The AD8627 uses n-channel JFETs to provide a low offset, low noise, high impedance input stage. The input common-mode voltage extends from 0.2 V below $-V_S$ to 2 V below $+V_S$. Driving the input of the amplifier, configured in unity gain buffer, closer than 2 V to the positive rail will cause an increase in common-mode voltage error as illustrated in TPC 13 and a loss of amplifier bandwidth. This loss of bandwidth causes the rounding of the output waveforms shown in Figures 1a and 1b, which have inputs that are 1 V and 0 V from $+V_S$, respectively.

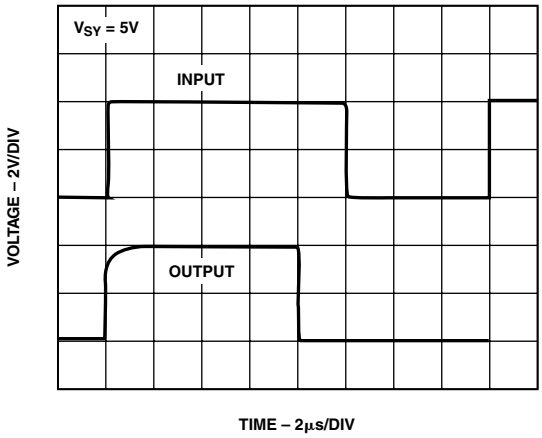


Figure 1a. Unity Gain Follower Response to 0 V to 4 V Step

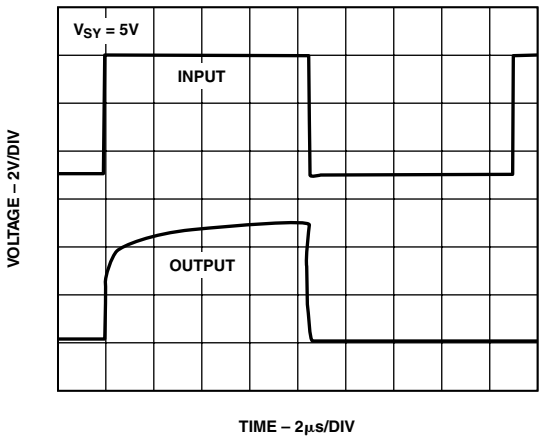


Figure 1b. Unity Gain Follower Response to 0 V to 5 V Step

The AD8627 will not experience phase reversal with input signals close to the positive rail, as shown in TPC 27. For input voltages greater than $+V_{SY}$, a resistor in series with the AD8627's noninverting input will prevent phase reversal at the expense of greater input voltage noise. This current limiting resistor should also be used if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage will be applied to the AD8627 when $\pm V_{SY} = 0$. Either of these conditions will damage the amplifier if the condition exists for more than 10 seconds. A 100 kΩ resistor allows the amplifier to withstand up to 10 V of continuous overvoltage, while increasing the input voltage noise by a negligible amount.

The AD8627 can safely withstand input voltages 15 V below $-V_{SY}$, as long as the total voltage between the positive supply and the input terminal is less than 26 V. Figures 2a, 2b, and 2c show the AD8627 in different configurations accommodating signals close to the negative rail. The amplifier input stage typically maintains picoamp level input currents across that input voltage range.

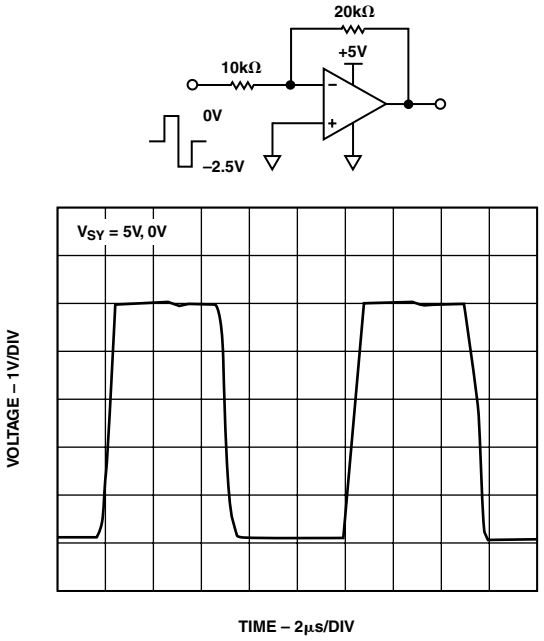


Figure 2a. Gain of Two Inverter Response to 2.5 V Step, Centered –1.25 V Below Ground

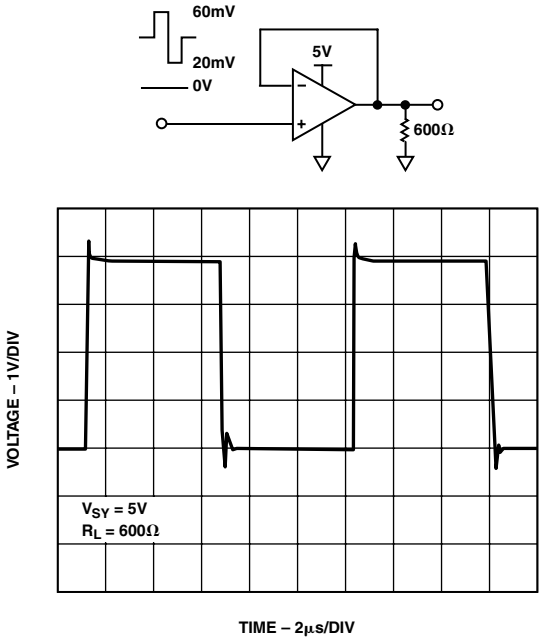


Figure 2b. Unity Gain Follower Response to 40 mV Step, Centered 40 mV Above Ground

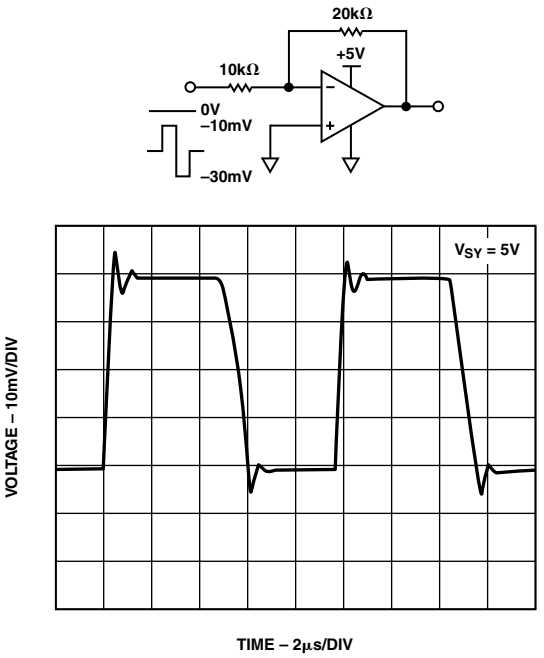


Figure 2c. Gain of Two Inverter Response to 20 mV Step, Centered 20 mV Below Ground

The AD8627 is designed for 16 nV/$\sqrt{\text{Hz}}$ wideband input voltage noise and maintains low noise performance to low frequencies, as shown in TPC 33. This noise performance, along with the AD8627's low input current and current noise, means that the AD8627 contributes negligible noise for applications with large source resistances.

The AD8627 has a unique bipolar rail-to-rail output stage that swings within 5 mV of the rail when up to 2 mA of current is drawn. At larger loads, the drop-out voltage increases as shown in TPC 15 and 16. The AD8627's wide bandwidth and fast slew rate allows it to be used with faster signals than previous single-supply JFETs. Figure 3 shows the response of AD8627, configured in unity gain, to a V_{IN} of 20 V p-p at 50 kHz. The FPBW of the part is close to 100 kHz.

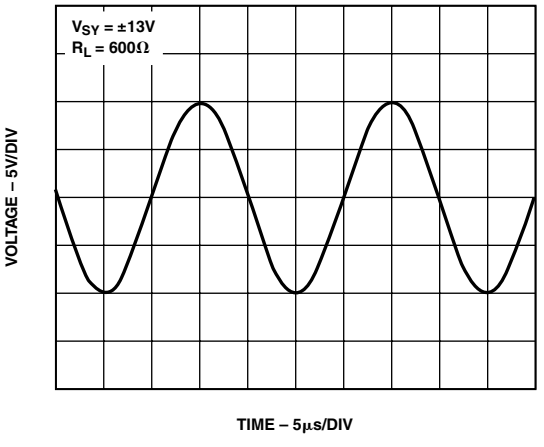


Figure 3. Unity Gain Follower Response to 20 V, 50 kHz Input Signal

Minimizing Input Current

The AD8627 is guaranteed to 1 pA max input current with a ±13 V supply voltage at room temperature. Careful attention to how the amplifier is used will maintain or possibly better this performance. The amplifier's operating temperature should be kept as low as possible. Like other JFET input amplifiers, the AD8627's input current will double for every 10°C rise in junction temperature, as illustrated in TPC 6. On-chip power dissipation will raise the device operating temperature, causing an increase in input current. Reducing supply voltage to cut power dissipation will reduce the AD8627's input current. Heavy output loads can also increase chip temperature; maintaining a minimum load resistance of 1 kΩ is recommended.

The AD8627 is designed for mounting on PC boards. Maintaining picoampere resolution in those environments requires a lot of care. Both the board and the amplifier's package have finite resistance. Voltage differences between the input pins and other pins as well as PC board metal traces will possibly cause parasitic currents larger than the AD8627's input current unless special precautions are taken. For proper board layout where you can get the best result, refer to the ADI website for proper layout seminar material. Two common methods of minimizing parasitic leakages that should be used are guarding of the input lines and maintaining adequate insulation resistance.

Contaminants such as solder flux on the board's surface and the amplifier's package can greatly reduce the insulation resistance between the input pin and those traces with supply or signal voltages. Both the package and the board must be kept clean and dry.

Photodiode Preamplifier Application

The low input current and offset voltage levels of the AD8627, together with its low voltage noise, make this amplifier an excellent choice for preamplifiers used in sensitive photodiode applications. In a typical photovoltaic preamp circuit, shown in Figure 4, the output of the amplifier is equal to:

$$V_{OUT} = -ID(Rf) = -Rp(P)Rf$$

where

ID = photodiode signal current (A)

Rp = photodiode sensitivity (A/W)

Rf = value of the feedback resistor, in Ω

P = light power incident to photodiode surface, in W

The amplifier's input current, I_B, will contribute an output voltage error that will be proportional to the value of the feedback resistor. The offset voltage error, V_{OS}, will cause a small current error due to the photodiode's finite shunt resistance, R_D. The resulting output voltage error, V_E, is equal to:

$$V_E = \left(1 + \frac{Rf}{R_D}\right)V_{OS} + Rf(I_B)$$

A shunt resistance on the order of 100 MΩ is typical for a small photodiode. Resistance R_D is a junction resistance that will typically drop by a factor of two for every 10°C rise in temperature. In the AD8627, both the offset voltage and drift are low, which helps minimize these errors. With I_B values of 1 pA and V_{OS} of 50 mV, V_E for Figure 4 is very negligible. Also the circuit in Figure 4 results in an SNR value of 95 dB for a signal bandwidth of 30 kHz.

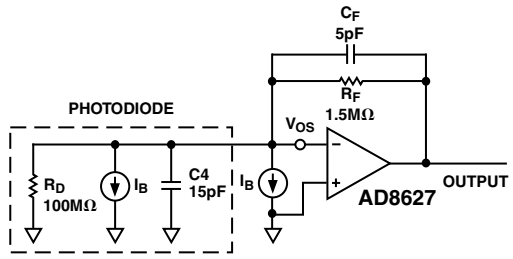


Figure 4. A Photodiode Model Showing DC Error

Output Amplifier for Digital-to-Analog Converters (DACs)
Many system designers use amplifiers as buffers on the output of amplifiers to increase the DAC's output driving capability. The high resolution current output DACs need high precision amplifiers on their output as current to voltage converters (I/V). Additionally, many DACs operate with a single supply of 5 V. In a single-supply application, selection of a suitable op amp may be more difficult as the output swing of the amplifier does not usually include the negative rail, in this case AGND. This can result in some degradation of the DAC's specified performance unless the application does not use codes near zero. The selected op amp needs to have very low offset voltage—for a 14-bit DAC, the DAC LSB is 300 μV with a 5 V reference—to eliminate the need for output offset trims. Input bias current should also be very low as the bias current multiplied by the DAC output impedance (around 10 kΩ in some cases) will add to the zero code error. Rail-to-rail input and output performance is desired. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code independent, but in order to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The AD8627, with very high input impedance, I_B of 1 pA, and fast slew rate, is an ideal amplifier for these types of applications. A typical configuration with a popular DAC is shown in Figure 5. In these situations, the amplifier adds another time constant to the system, increasing the settling time of the output. The AD8627, with 5 MHz of BW, helps in achieving a faster effective settling time of the combined DAC and amplifier.

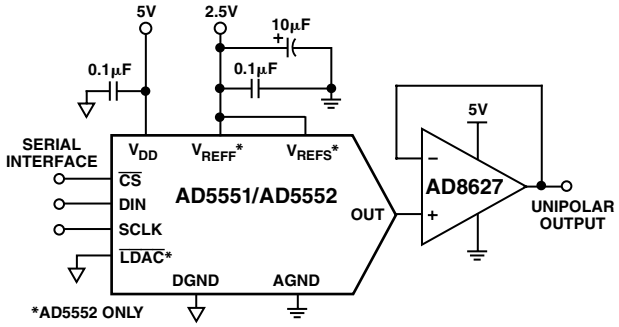


Figure 5. Unipolar Output

In applications with full four-quadrant multiplying capability or a bipolar output swing, the circuit in Figure 6 can be used. In this circuit, the first and second amplifiers provide a total gain of 2, which increases the output voltage span to 20 V. Biasing the external amplifier with a 10 V offset from the reference voltage results in a full four-quadrant multiplying circuit.

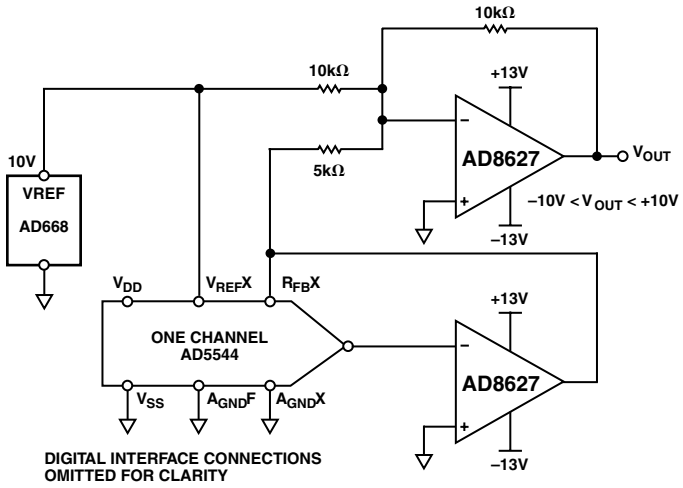


Figure 6. Four-Quadrant Multiplying Application Circuit

Eight-Pole Sallen Key Low-Pass Filter

The AD8627's high input impedance and dc precision make it a great selection for active filters. Due to the very low bias current of the AD8627, high value resistors can be used to construct low frequency filters. The AD8627's picoamp level input currents contribute minimal dc errors. Figure 7 shows an example, a 10 Hz eight-pole Sallen Key Filter constructed using the AD8627. Different numbers of the AD8627 can be used depending on the desired response, which is shown in Figure 8. The high value used for R1 minimizes interaction with signal source resistance. Pole placement in this version of the filter minimizes the Q associated with the lower pole section of the filter. This eliminates any peaking of the noise contribution of resistors in the preceding sections, minimizing the inherent output voltage noise of the filter.

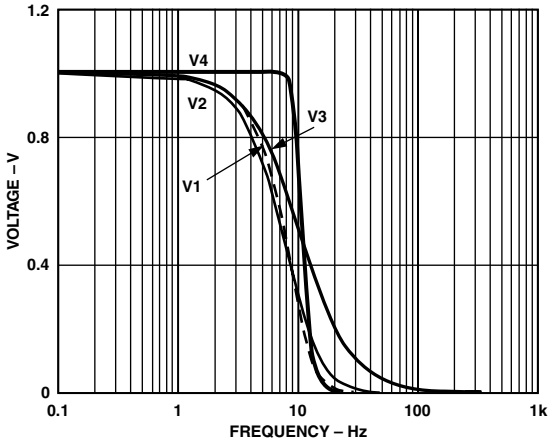


Figure 8. Frequency Response Output at Different Stages of the Low-Pass Filter

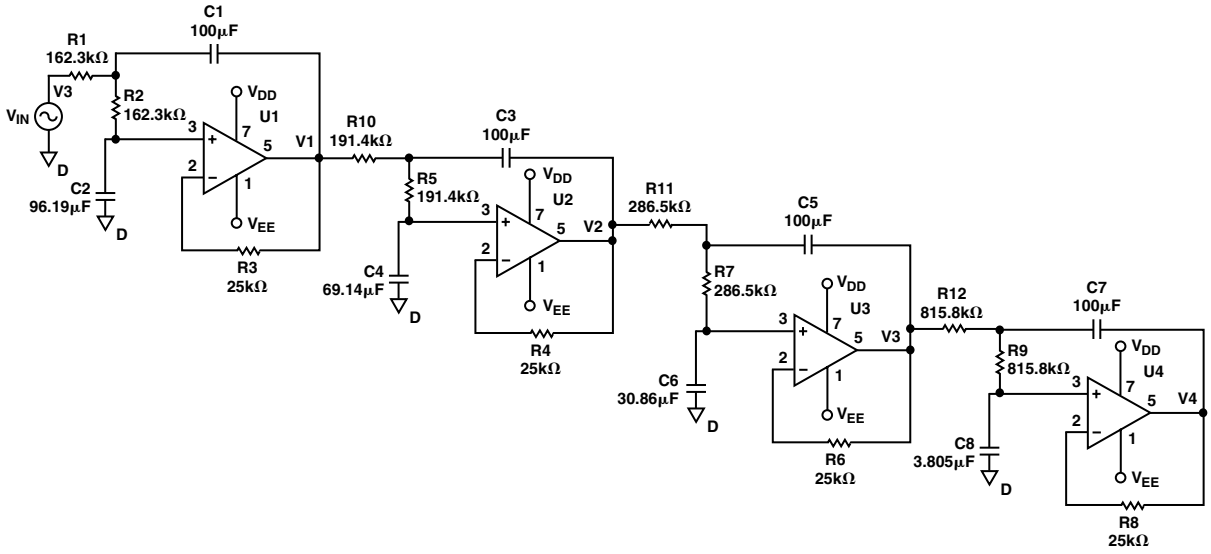
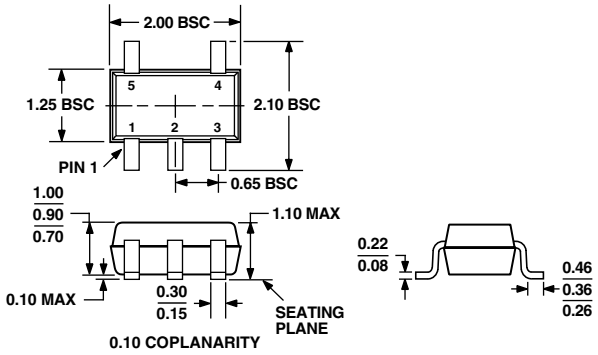


Figure 7. 10 Hz, Eight-Pole Sallen Key Low-Pass Filter

OUTLINE DIMENSIONS

5-Lead Plastic Surface Mount Package [SC70]
(KS-5)

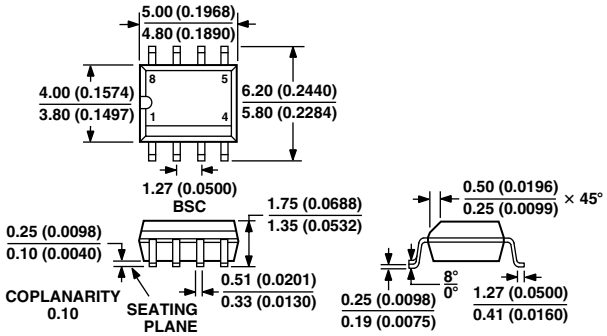
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203AA

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(RN-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

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