STL20NM20N

N-CHANNEL 200V - 0.11Ω - 20A PowerFLAT™ ULTRA LOW GATE CHARGE MDmesh™ II MOSFET

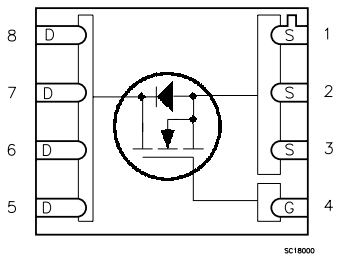
TARGET DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STL20NM20N	200 V	< 0.13 Ω	20 A

- WORLDWIDE LOWEST GATE CHARGE
- TYPICAL $R_{DS}(on)$ = 0.11Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- LOW GATE RESISTANCE
- LOW INPUT CAPACITANCE
- HIGH dv/dt and AVALANCHE CAPABILITIES

PowerFLAT™(6x5)
(Chip Scale Package)

INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

This 200V MOSFET with a new advanced layout brings all unique advantages of MDmesh technology to lower voltages. The device exhibits worldwide lowest gate charge for any given on-resistance.Its use is therefore ideal as primary switch in isolated DC-DC converters for Telecom and Computer applications.Used in combination with secondary-side low-voltage STripFET™ products, it contributes to reducing losses and boosting efficiency.The new PowerFLAT™ package allows a significant reduction in board space without compromising performance.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density allowing system miniaturization and higher efficiencies

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STL20NM20N	L20NM20N	PowerFLAT	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source Voltage	± 30	V
I_D (2)	Drain Current (continuous) at T_C = 25°C (Steady State) Drain Current (continuous) at T_C = 100°C	20 12.5	A A
I_{DM} (3)	Drain Current (pulsed)	80	A
P_{TOT} (2)	Total Dissipation at T_C = 25°C (Steady State)	2.5	W
P_{TOT} (4)	Total Dissipation at T_C = 25°C (Steady State)	80	W
	Derating Factor (2)	0.02	W/°C
dv/dt (5)	Peak Diode Recovery voltage slope	10	V/ns

THERMAL DATA

Symbol	Parameter	Typ.	Max.	Unit
Rthj-F	Thermal Resistance Junction-Foot (Drain)		1.56	°C/W
Rthj-amb (2)	Thermal Resistance Junction-ambient	35	50	°C/W
T_j T_{stg}	Max. Operating Junction Temperature Storage Temperature	–55 to 150		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	TBD	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 35 V)	TBD	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30 V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.5	4.2	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 2 A		0.11	0.13	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (6)	Forward Transconductance	V_{DS} = 15 V, I_D = 2 A		1.4		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		670 180 12		pF pF pF
$C_{oss\ eq.}$ (*)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		TBD		pF
R_G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		TBD		Ω

(*) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 100 V, I_D = 2 A R_G = 4.7Ω V_{GS} = 10 V (see test circuit, Figure 3)		TBD TBD		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 160 V, I_D = 4 A, V_{GS} = 10 V		19 3.5 11		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-Voltage RiseTime Fall Time Cross-Over Time	V_{DD} = 100 V, I_D = 2 A, R_G = 4.7Ω, V_{GS} = 10 V (see test circuit, Figure 3)		TBD TBD TBD		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				20	A
I_{SDM} (3)	Source-drain Current (pulsed)				80	A
V_{SD} (6)	Forward On Voltage	I_{SD} = 2 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 2 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 25°C (see test circuit, Figure 5)		89 300 6.5		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 2 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150°C (see test circuit, Figure 3)		TBD TBD TBD		ns nC A

Note: 1. Current Limited by Package. The value is rated according to $R_{thj\text{-}F}$.
2. When Mounted on FR-4 Board of 1inch^2, 2 oz Cu
3. Pulse width limited by safe operating area
4. The value is rated according to $R_{thj\text{-}F}$.
5. $I_{SD} \le 20A$, di/dt ≤ 400A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le T_{JMAX}$
6. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Fig. 1: Switching Times Test Circuit For Resistive Load

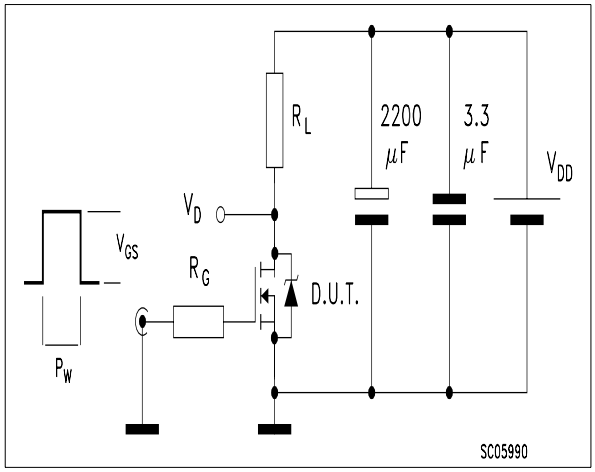


Fig. 2: Gate Charge test Circuit

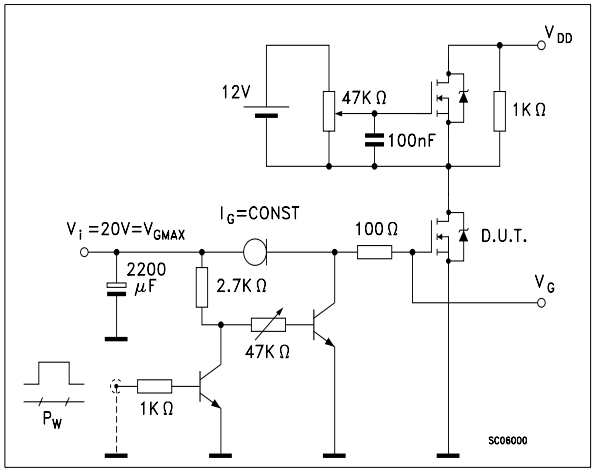
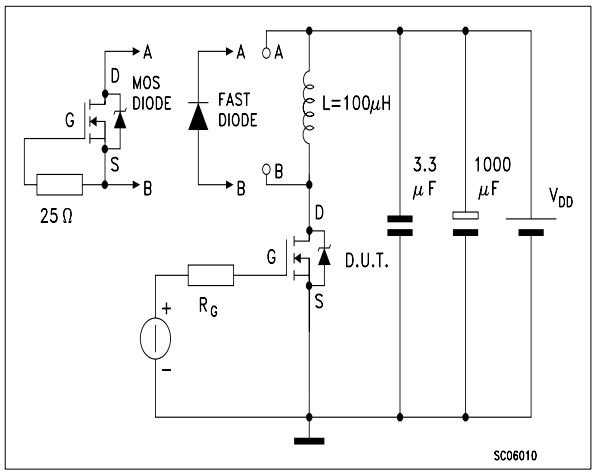


Fig. 3: Test Circuit For Diode Recovery Behaviour



PowerFLAT™(6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80		1.00	0.031		0.039
A1		0.02			0.001	
b	0.35		0.47	0.014		0.018
C		1.61			0.063	
D		5.00			0.197	
D2	4.15		4.25	0.163		0.167
E		6.00			0.236	
E2	3.55		3.65	0.140		0.144
e		1.27			0.049	
F		1.99			0.078	
G		2.20			0.086	
H		0.40			0.015	
I		0.219			0.0086	
L	0.70		0.90	0.028		0.035