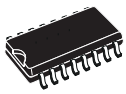
74LVQ161

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

- HIGH SPEED:
  f_{MAX} = 180 MHz (TYP.) at V_{CC} = 3.3 V
- COMPATIBLE WITH TTL OUTPUTS
- LOW POWER DISSIPATION:
  I_{CC} = 4 µA (MAX.) at T_A=25°C
- LOW NOISE:
  V_{OLP} = 0.3V (TYP.) at V_{CC} = 3.3V
- 75Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 12mA (MIN) at V_{CC} = 3.0 V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2V to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 161
- IMPROVED LATCH-UP IMMUNITY



SOP

TSSOP

ORDER CODES

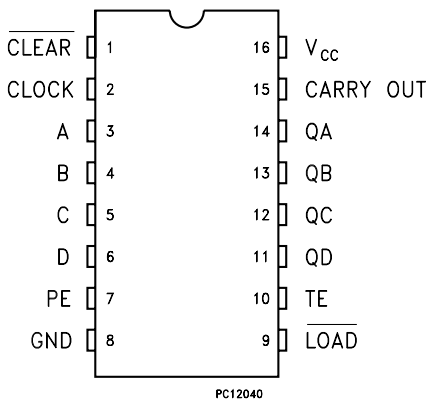
PACKAGE	TUBE	T & R
SOP	74LVQ161M	74LVQ161MTR
TSSOP		74LVQ161TTR

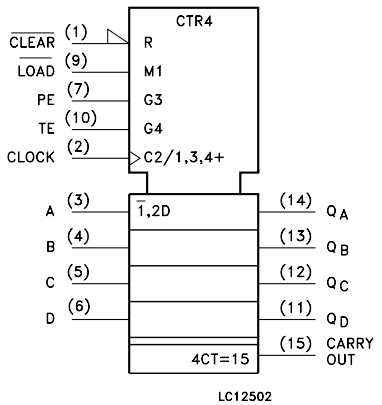
DESCRIPTION

The 74LVQ161 is a low voltage CMOS SYNCHRONOUS PRESETTABLE COUNTER fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and low noise 3.3V applications. It is a 4 bit binary counter with Asynchronous Clear.

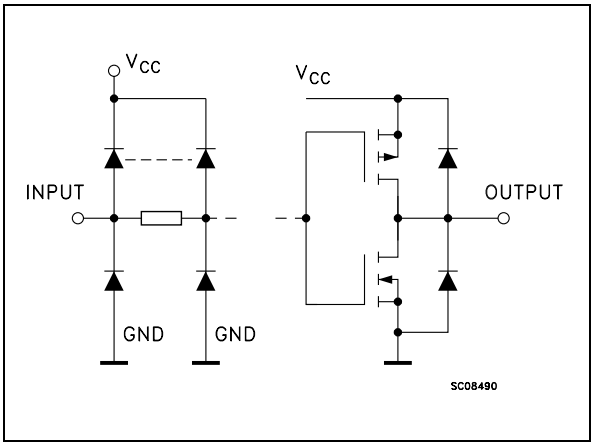
The circuit have four fundamental modes of operation, in order of preference: synchronous reset, parallel load, count-up and hold. Four control inputs, Master Reset (CLEAR), Parallel Enable Input (PE) and Count Enable Carry Input (TE), determine the mode of operation as shown in the Truth Table. A LOW signal on CLEAR overrides counting and parallel loading and sets all outputs on LOW state. A LOW signal on LOAD overrides counting and allows information on Parallel Data Qn inputs to be loaded into the flip-flops on the next rising edge of CLOCK. With LOAD and CLEAR, PE and TE permit counting when both are high. Conversely, a LOW signal on either PE and TE inhibits counting. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

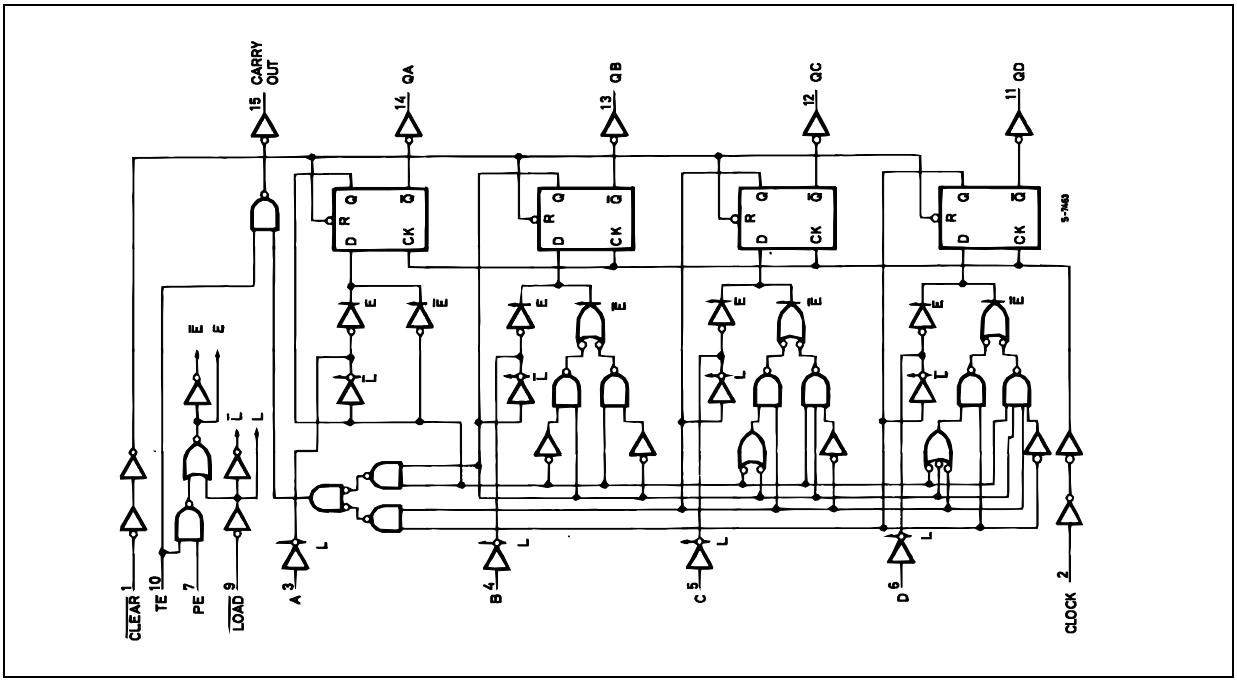
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Asynchronous Master Reset
2	CLOCK	Clock Input (LOW to HIGH Edge Trigger)
3, 4, 5, 6	A, B, C, D	Data Inputs
7	PE	Count Enable Input
10	TE	Count Enable Carry Input
9	$\overline{\text{LOAD}}$	Parallel Enable Input
14, 13, 12, 11	QA to QD	Flip-Flop Outputs
15	CARRY OUT	Terminal Count Output
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

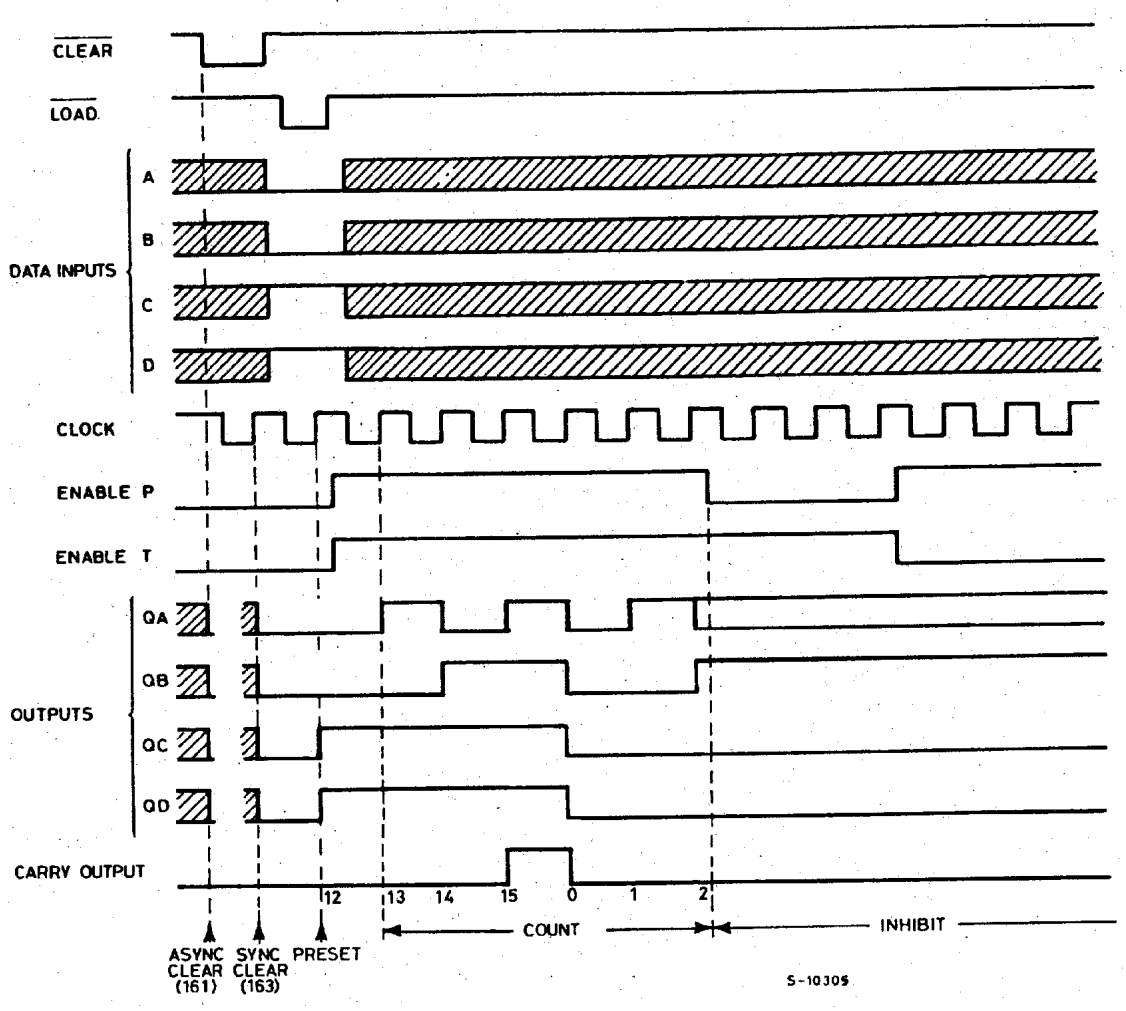
INPUTS					OUTPUTS				FUNCTION
$\overline{\text{CLEAR}}$	$\overline{\text{LOAD}}$	PE	TE	CK					
L	X	X	X	X	L	L	L	L	RESET TO "0"
H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↓	NO CHANGE				NO COUNT

X : Don't Care; A, B, C, D; Logic level of data input; CARRY OUT : TE x QA x QB x QC x QD

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 300	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time V_{CC} = 3.0V (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V
2) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	3.0 to 3.6		2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	3.0	I_O=-50 µA	2.9	2.99		2.9		2.9		V
			I_O=-12 mA	2.58			2.48		2.48		
			I_O=-24 mA				2.2		2.2		
V_{OL}	Low Level Output Voltage	3.0	I_O=50 µA		0.002	0.1		0.1		0.1	V
			I_O=12 mA		0	0.36		0.44		0.44	
			I_O=24 mA					0.55		0.55	
I_I	Input Leakage Current	3.6	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	3.6	V_I = V_{CC} or GND			4		40		40	µA
I_{OLD}	Dynamic Output Current (note 1, 2)	3.6	V_{OLD} = 0.8 V max				36		25		mA
I_{OHD}			V_{OHD} = 2 V min				-25		-25		mA

1) Maximum test duration 2ms, one output loaded at time
2) Incident wave switching is guaranteed on transmission lines with impedances as low as 75Ω

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C_L = 50 pF		0.3	0.8					V
V_{OLV}				-0.8	-0.3						
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2							V
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					V

1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input $t_r = t_f$ = 3ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q	2.7			8.0	13.0		15.0		17.0	ns
		3.3(*)			6.8	9.5		11.0		12.5	
t_{PLH} t_{PHL}	Propagation Delay Time CK to CARRY OUT	2.7			9.1	14.0		16.0		18.5	ns
		3.3(*)			7.5	10.5		12.0		14.0	
t_{PLH} t_{PHL}	Propagation Delay Time TE to CARRY OUT	2.7			5.6	10.0		11.5		13.0	ns
		3.3(*)			4.7	8.0		9.5		10.5	
t_{PHL}	Propagation Delay Time CLR to Q	2.7			8.0	12.0		15.0		17.0	ns
		3.3(*)			6.1	9.5		11.0		12.5	
t_{PHL}	Propagation Delay Time CLR to CARRY OUT	2.7			8.0	14.0		16.0		18.5	ns
		3.3(*)			6.7	10.5		12.0		14.0	
$t_{W(L)}$	CLR Pulse Width, LOW (LOAD)	2.7		4.0	1.9		4.0		4.0		ns
		3.3(*)		3.0	1.9		3.0		3.0		
t_W	CLOCK Pulse Width, HIGH or LOW	2.7		4.0	1.9		4.0		4.0		ns
		3.3(*)		3.0	1.9		3.0		3.0		
t_s	Setup Time HIGH or LOW (INPUT to CLOCK)	2.7		5.0	2.5		5.0		5.0		ns
		3.3(*)		4.0	2.1		4.0		4.0		
t_h	Hold Time HIGH or LOW (INPUT to CLOCK)	2.7		1	-1.3		1		1		ns
		3.3(*)		0.5	-1.0		0.5		0.5		
t_s	Setup Time HIGH or LOW (LOAD to CLOCK)	2.7		3.0	1.5		3.0		3.0		ns
		3.3(*)		2.5	1.2		2.5		2.5		
t_h	Hold Time HIGH or LOW (LOAD to CLOCK)	2.7		1	-0.6		1		1		ns
		3.3(*)		0.5	-0.5		0.5		0.5		
t_s	Setup Time HIGH or LOW (PE or TE to CLOCK)	2.7		7.0	3.4		7.0		7.0		ns
		3.3(*)		6.0	3.0		6.0		6.0		
t_h	Hold Time HIGH or LOW (PE or TE to CLOCK)	2.7		0	-2.6		0		0		ns
		3.3(*)		0	-2.2		0		0		
t_{REM}	Recovery Time CLR to CK	2.7		1	-0.8		1		1		ns
		3.3(*)		0.5	-0.6		0.5		0.5		
f_{MAX}	Maximum Clock Frequency	2.7		100	150		80		60		MHz
		3.3(*)		120	180		100		80		
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note1, 2)	2.7			0.5	1.0		1.0		1.0	ns
		3.3(*)			0.5	1.0		1.0		1.0	

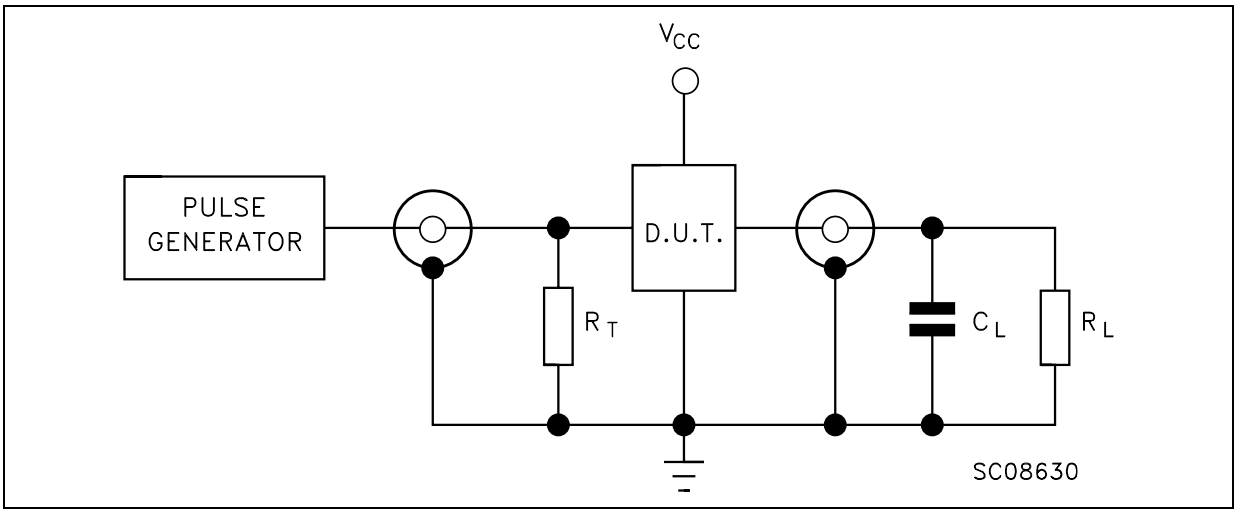
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)
2) Parameter guaranteed by design
(*) Voltage range is 3.3V ± 0.3V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	3.3			4						pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10MHz		16						pF

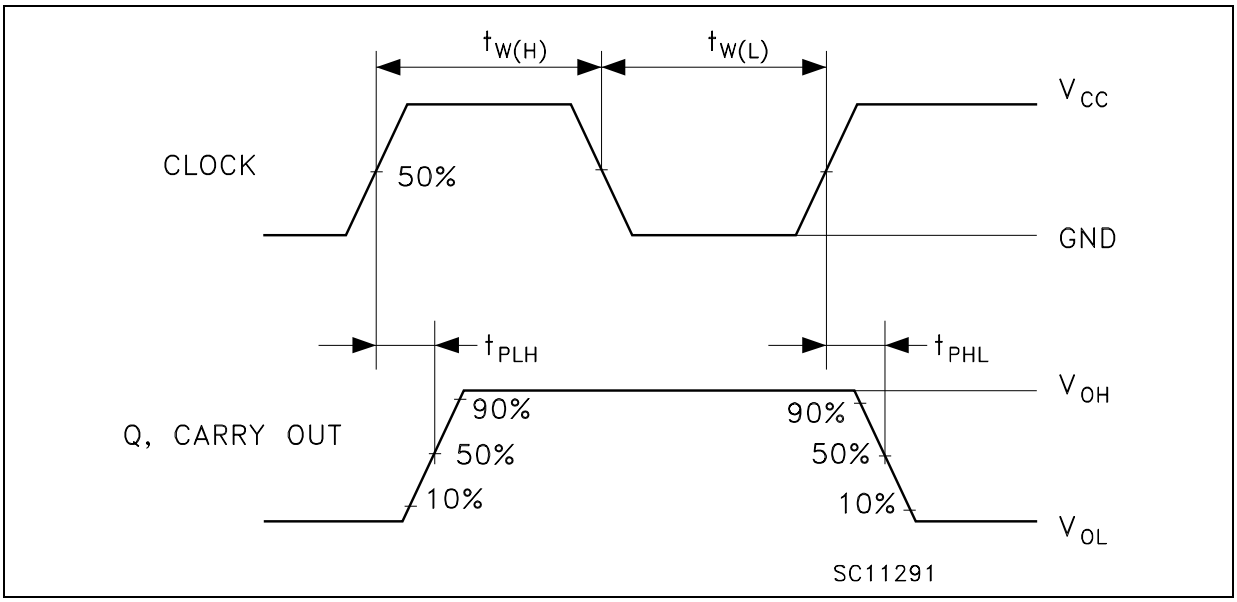
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)

TEST CIRCUIT

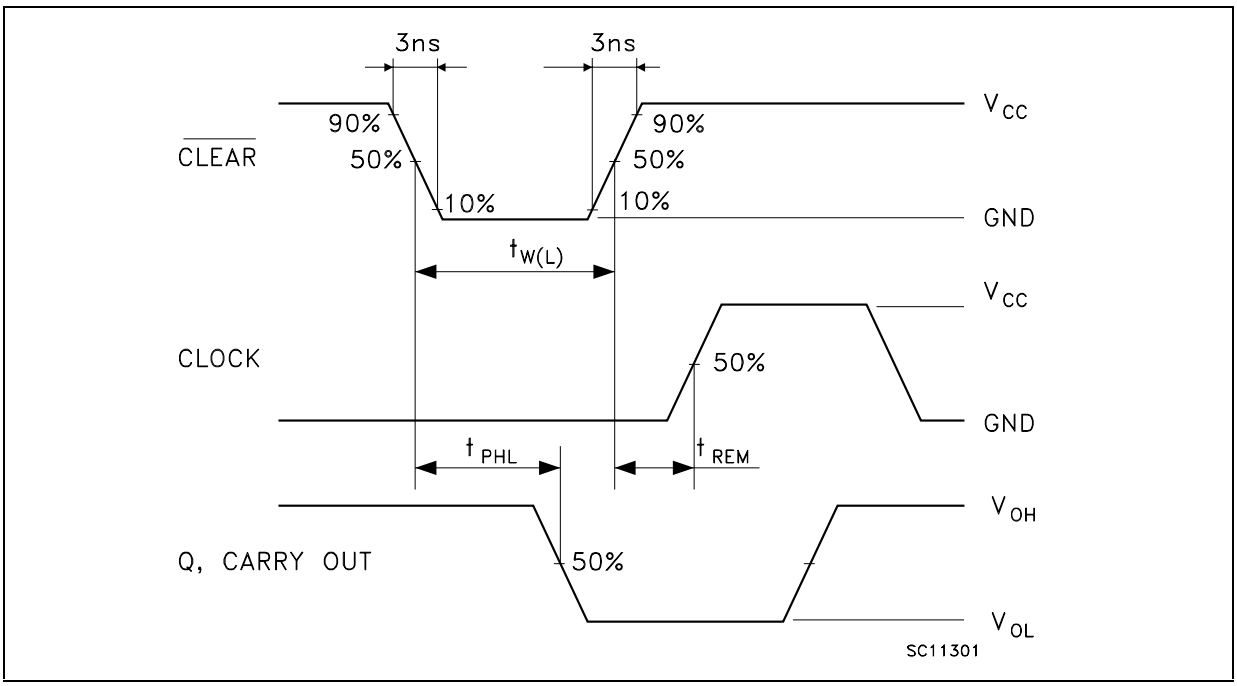


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

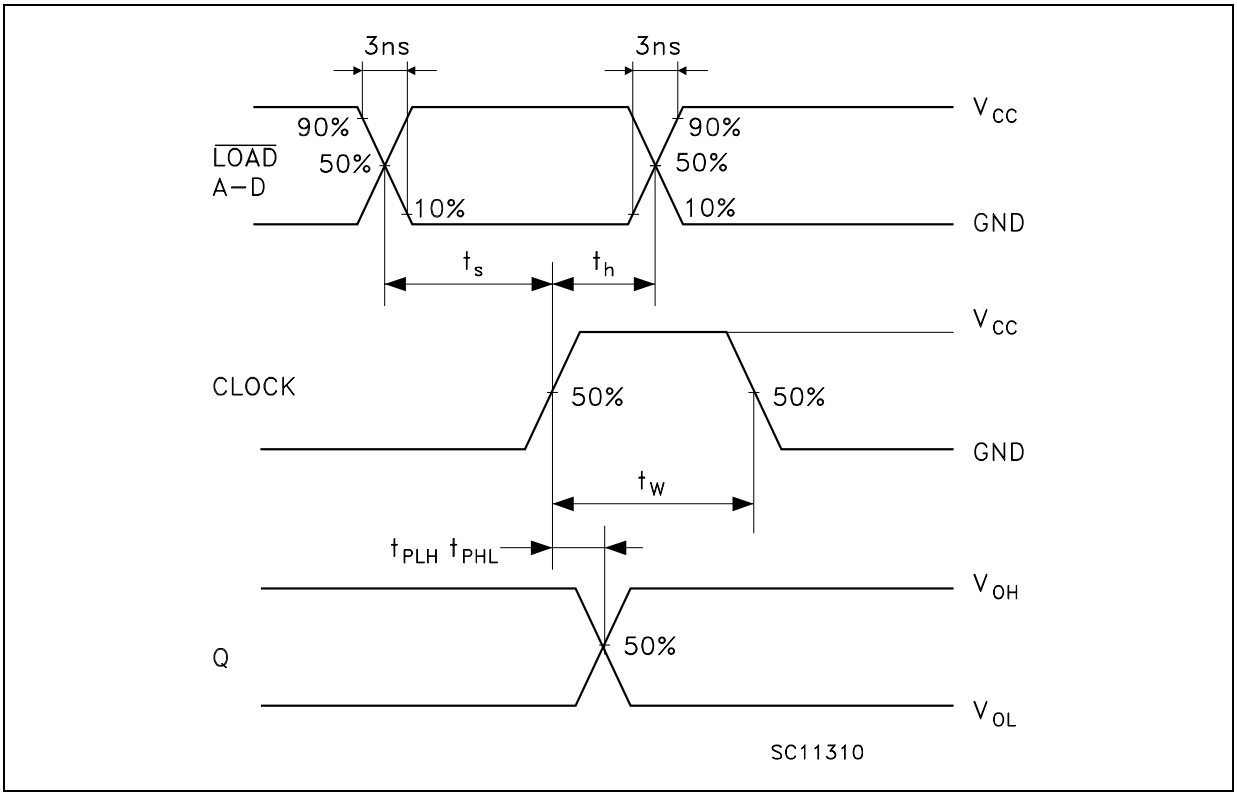
WAVEFORM 1 : PROPAGATION DELAYS , COUNT MODE (f=1MHz; 50% duty cycle)



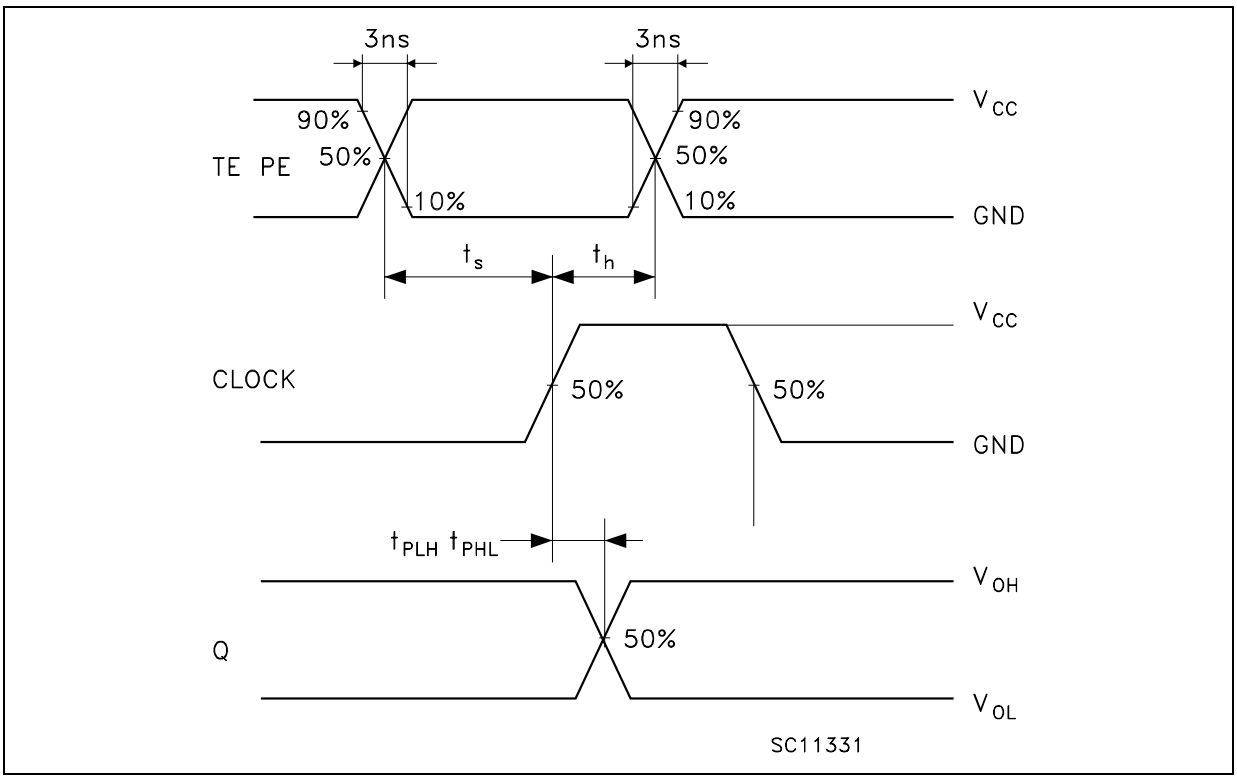
WAVEFORM 2: PROPAGATION DELAYS CLEAR MODE (f=1MHz; 50% duty cycle)



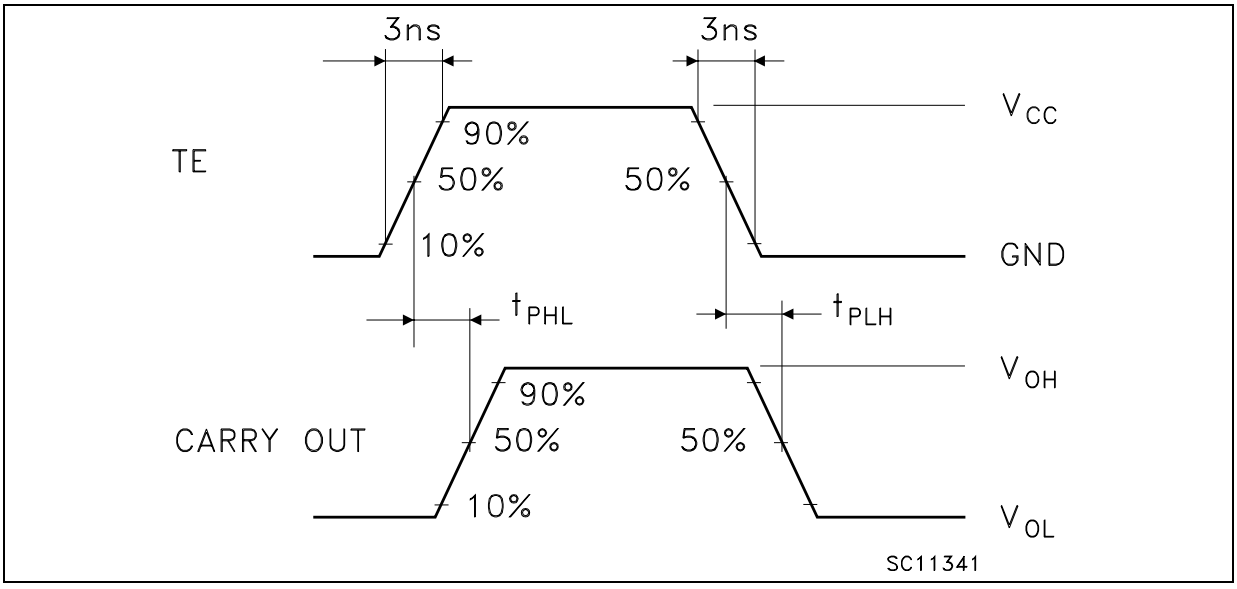
WAVEFORM 3: PROPAGATION DELAYS PRESET MODE (f=1MHz; 50% duty cycle)



WAVEFORM 4: PROPAGATION DELAYS COUNTABLE MODE (f=1MHz; 50% duty cycle)

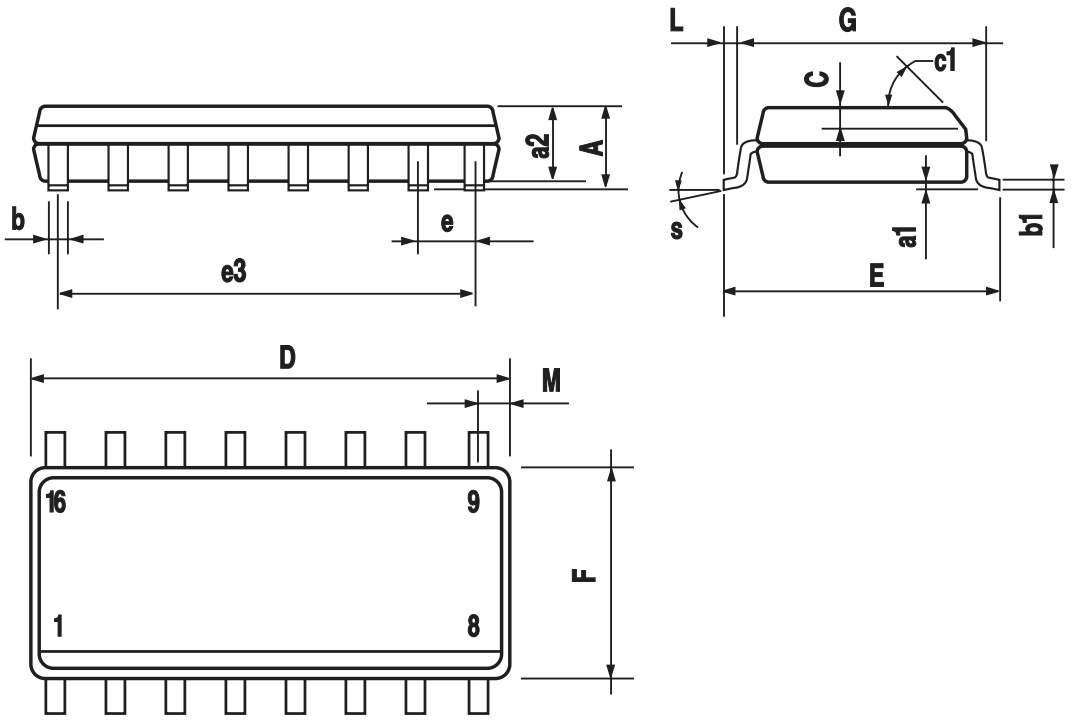


WAVEFORM 5: PROPAGATION DELAYS CASCADE MODE (f=1MHz; 50% duty cycle)



SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030