

# DATA SHEET

**74LV139**

Dual 2-to-4 line decoder/demultiplexer

Product data  
Supersedes data of 1998 Apr 28

2003 Mar 13

## Dual 2-to-4 line decoder/demultiplexer

## 74LV139

## FEATURES

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard
- $I_{CC}$  category: MSI

## APPLICATIONS

- Memory decoding or data-routing
- Code conversion

## DESCRIPTION

The 74LV139 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT139.

The 74LV139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs ( $nA_0$  and  $nA_1$ ) and providing four mutually exclusive active LOW outputs ( $n\bar{Y}_0$  to  $n\bar{Y}_3$ ). Each decoder has an active LOW enable input ( $n\bar{E}$ ).

When  $n\bar{E}$  is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay $nA_n$ to $n\bar{Y}_n$ , $n\bar{E}$ to $n\bar{Y}_n$	$C_L = 15$ pF; $V_{CC} = 3.3$ V	11 10	ns
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per multiplexer	$V_{CC} = 3.3$ V $V_I = \text{GND to } V_{CC}^1$	42	pF

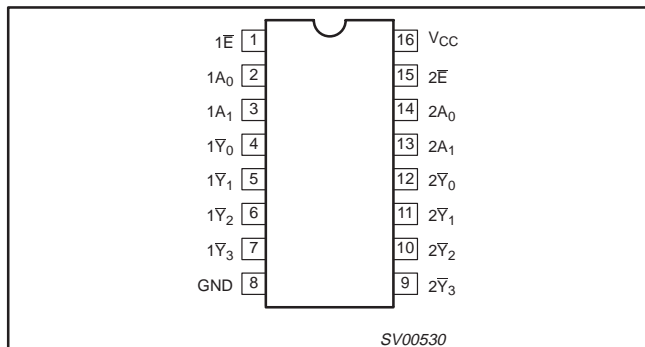
## NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W)  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 $N$  = number of outputs switching;  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	PKG. DWG. #
16-Pin Plastic DIL	-40 °C to +125 °C	74LV139N	SOT38-4
16-Pin Plastic SO	-40 °C to +125 °C	74LV139D	SOT109-1
16-Pin Plastic SSOP Type II	-40 °C to +125 °C	74LV139DB	SOT338-1
16-Pin Plastic TSSOP Type I	-40 °C to +125 °C	74LV139PW	SOT403-1

## PIN CONFIGURATION



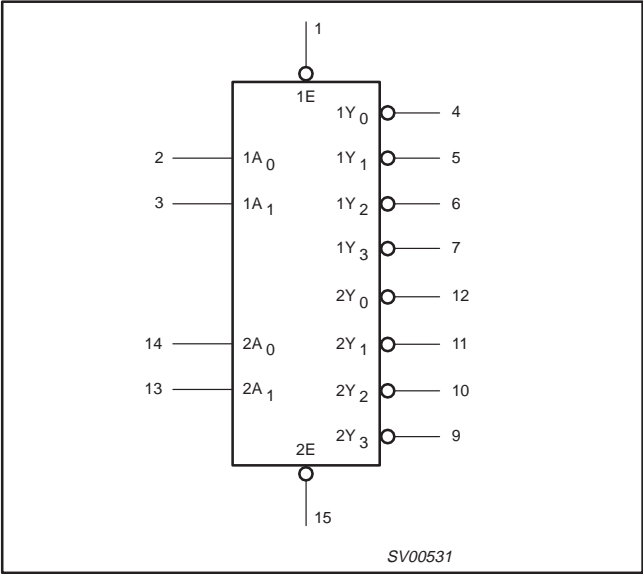
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	$1\bar{E}$ , $2\bar{E}$	Enable inputs (active LOW)
2, 3	$1A_0$ , $1A_1$	Address inputs
4, 5, 6, 7	$1\bar{Y}_0$ to $1\bar{Y}_3$	Outputs (active LOW)
8	GND	Ground (0 V)
12, 11, 10, 9	$2\bar{Y}_0$ to $2\bar{Y}_3$	Outputs (active LOW)
14, 13	$2A_0$ , $2A_1$	Address inputs
16	$V_{CC}$	Positive supply voltage

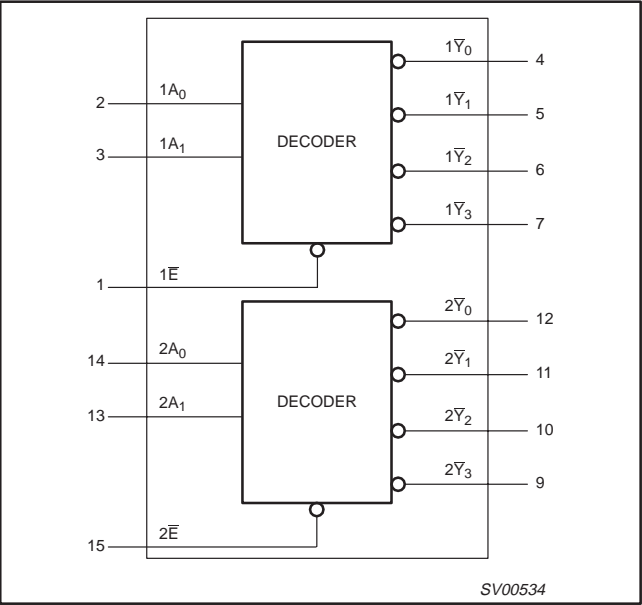
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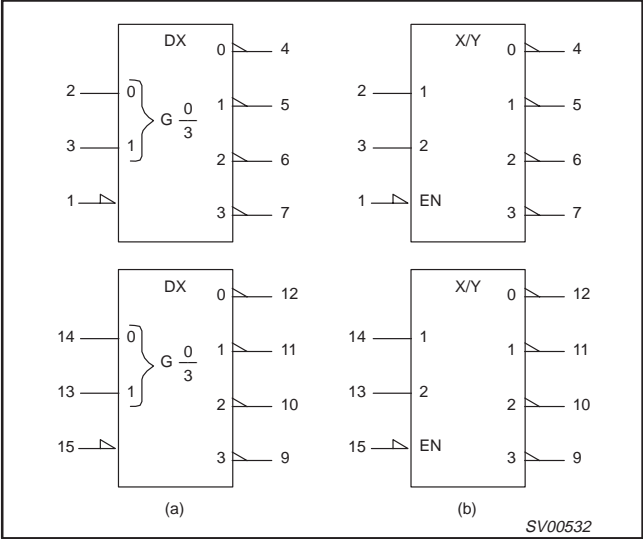
LOGIC DIAGRAM



FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS			OUTPUTS			
nE	nA <sub>0</sub>	nA <sub>1</sub>	nY <sub>0</sub>	nY <sub>1</sub>	nY <sub>2</sub>	nY <sub>3</sub>
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

NOTES:  
H = HIGH voltage level  
L = LOW voltage level  
X = don't care

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note 1	1.0	3.3	5.5	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$	–	–	500	ns/V
		$V_{CC} = 2.0V$ to $2.7V$	–	–	200	ns/V
		$V_{CC} = 2.7V$ to $3.6V$	–	–	100	ns/V
		$V_{CC} = 3.6V$ to $5.5V$	–	–	50	ns/V

## NOTE:

1. The LV is guaranteed to function down to  $V_{CC} = 1.0$  V (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2$  V to  $V_{CC} = 5.5$  V.

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	50	mA
$\pm I_O$	DC output source or sink current (standard outputs)	$-0.5$ V $< V_O < V_{CC} + 0.5$ V	25	mA
$\pm I_{GND}, \pm I_{CC}$	DC $V_{CC}$ or GND current for types with standard outputs		50	mA
$T_{stg}$	Storage temperature range		–65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 °C to +125 °C above +70 °C derate linearly with 12 mW/K above +70 °C derate linearly with 8 mW/K above +60 °C derate linearly with 5.5 mW/K	750 500 400	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			−40 °C to +85 °C			−40 °C to +125 °C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2 V	0.9			0.9		V
		V <sub>CC</sub> = 2.0 V	1.4			1.4		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0			2.0		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7*V <sub>CC</sub>			0.7*V <sub>CC</sub>		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2 V			0.3		0.3	V
		V <sub>CC</sub> = 2.0 V			0.6		0.6	
		V <sub>CC</sub> = 2.7 V to 3.6 V			0.8		0.8	
		V <sub>CC</sub> = 4.5 V to 5.5			0.3*V <sub>CC</sub>		0.3*V <sub>CC</sub>	
V <sub>OH</sub>	HIGH level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; −I <sub>O</sub> = 100 μA		1.2				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; −I <sub>O</sub> = 100 μA	1.8	2.0		1.8		
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; −I <sub>O</sub> = 100 μA	2.5	2.7		2.5		
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; −I <sub>O</sub> = 100 μA	2.8	3.0		2.8		
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; −I <sub>O</sub> = 100 μA	4.3	4.5		4.3		
V <sub>OH</sub>	HIGH level output voltage; STANDARD outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; −I <sub>O</sub> = 6 mA	2.40	2.82		2.20		V
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; −I <sub>O</sub> = 12 mA	3.60	4.20		3.50		
V <sub>OL</sub>	LOW level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0	0.2		0.2	
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0	0.2		0.2	
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0	0.2		0.2	
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0	0.2		0.2	
V <sub>OL</sub>	LOW level output voltage; STANDARD outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6 mA		0.25	0.40		0.50	V
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12 mA		0.35	0.55		0.65	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND			1.0		1.0	μA
I <sub>CC</sub>	Quiescent supply current; MSI	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0			20.0		160	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> − 0.6 V			500		850	μA

**NOTE:**1. All typical values are measured at  $T_{amb} = 25\text{ }^\circ\text{C}$ .

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AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 1$  k $\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 °C to +85 °C			−40 °C to +125 °C		
			V <sub>CC</sub> (V)	MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nA <sub>n</sub> to $\bar{Y}_n$	Figures 1, 2	1.2		70				ns
			2.0		24	31		39	
			2.7		18	23		29	
			3.0 to 3.6		13 <sup>2</sup>	18		23	
			4.5 to 5.5			15		19	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay n $\bar{E}$ to $\bar{Y}_n$	Figures 1, 2	1.2		60				ns
			2.0		20	27		34	
			2.7		15	20		25	
			3.0 to 3.6		11 <sup>2</sup>	16		20	
			4.5 to 5.5			13		16	

- NOTES:
1. Unless otherwise stated, all typical values are measured at  $T_{amb} = 25$  °C.
  2. Typical values are measured at  $V_{CC} = 3.3$  V.

AC WAVEFORMS

$V_M = 1.5$  V at  $V_{CC} \geq 2.7$  V and  $\leq 3.6$  V;  
 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7$  V and  $\geq 4.5$  V.  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

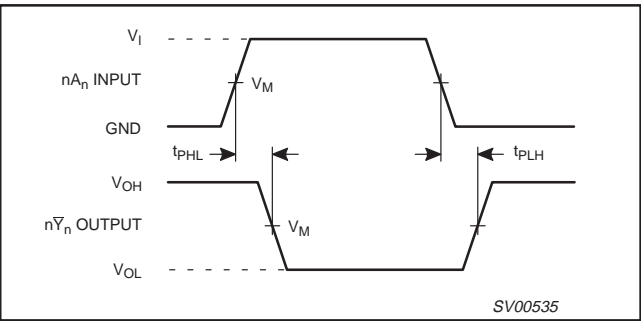


Figure 1. Address input ( $nA_n$ ) to output ( $n\bar{Y}_n$ ) propagation delays.

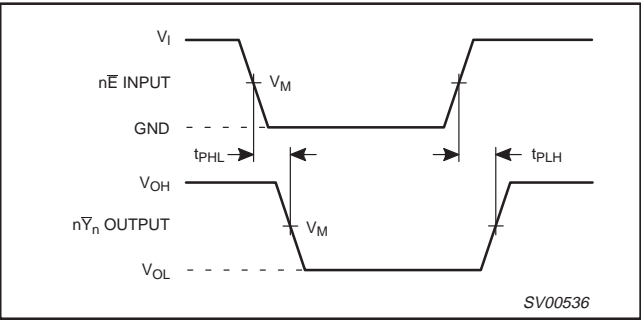


Figure 2. Enable input ( $n\bar{E}$ ) to output ( $n\bar{Y}_n$ ) propagation delays.

TEST CIRCUIT

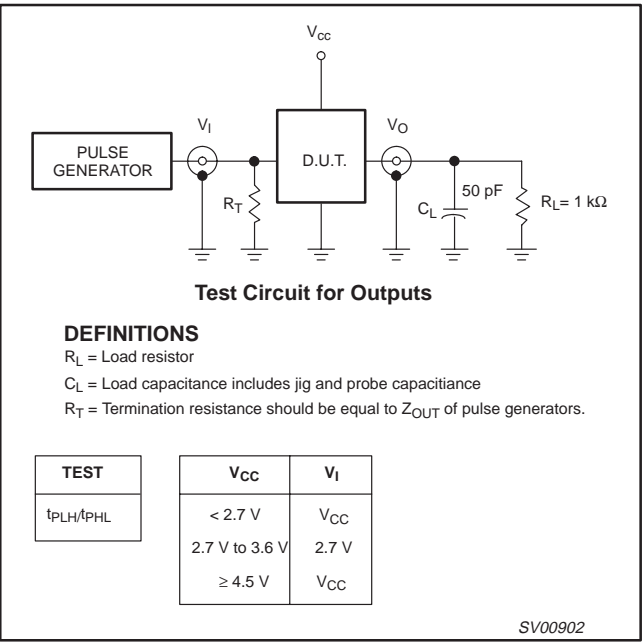


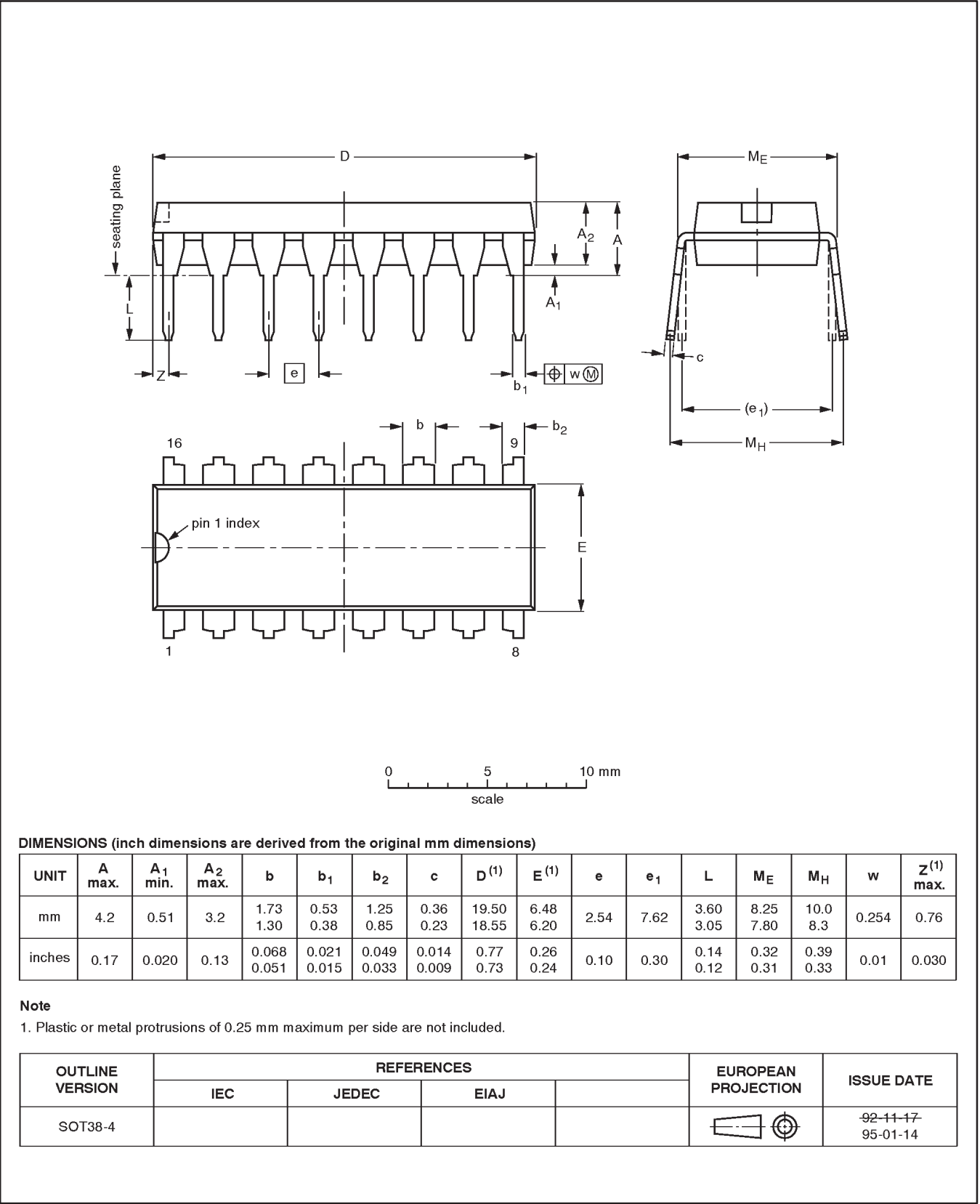
Figure 3. Load circuitry for switching times.

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

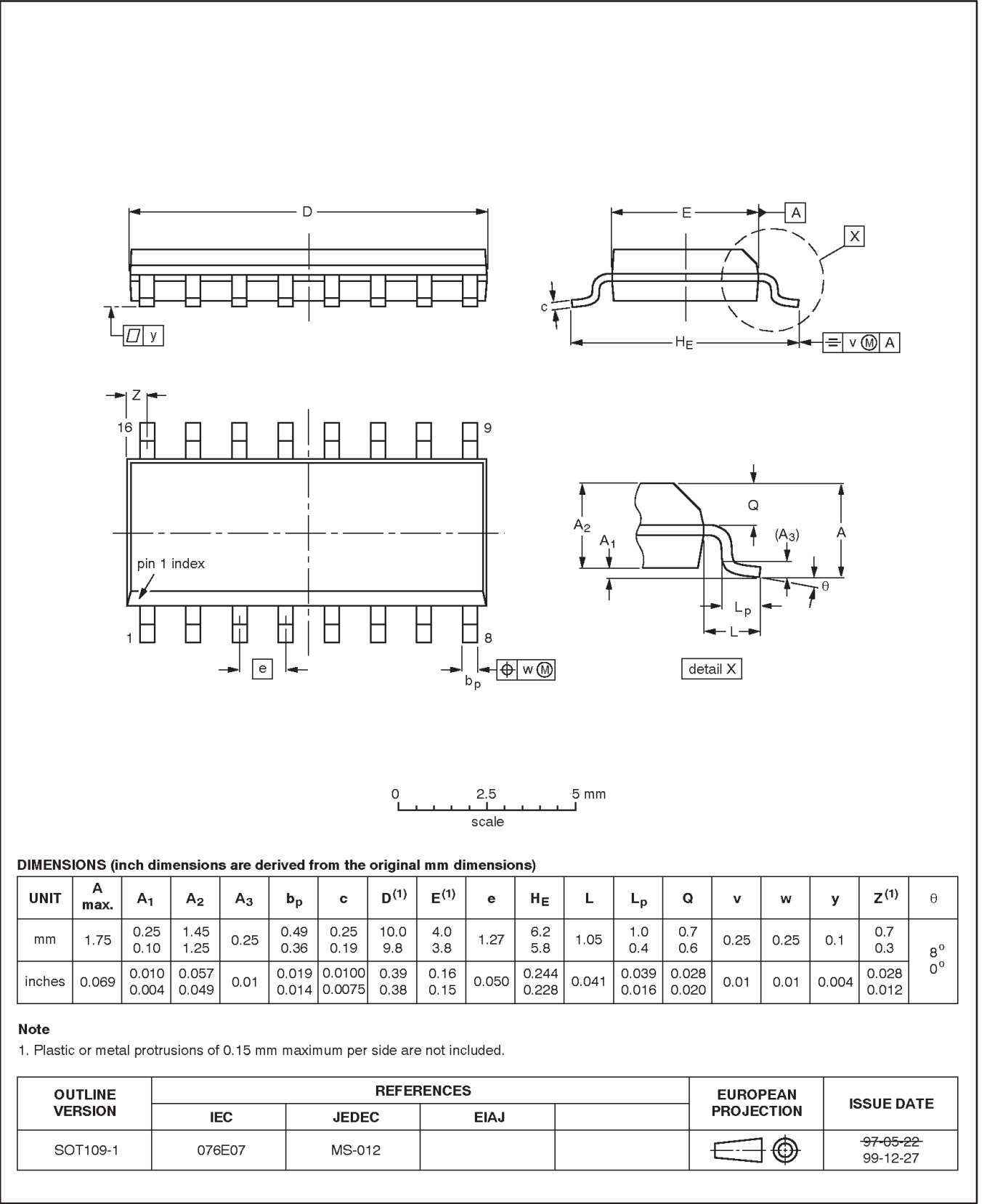


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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

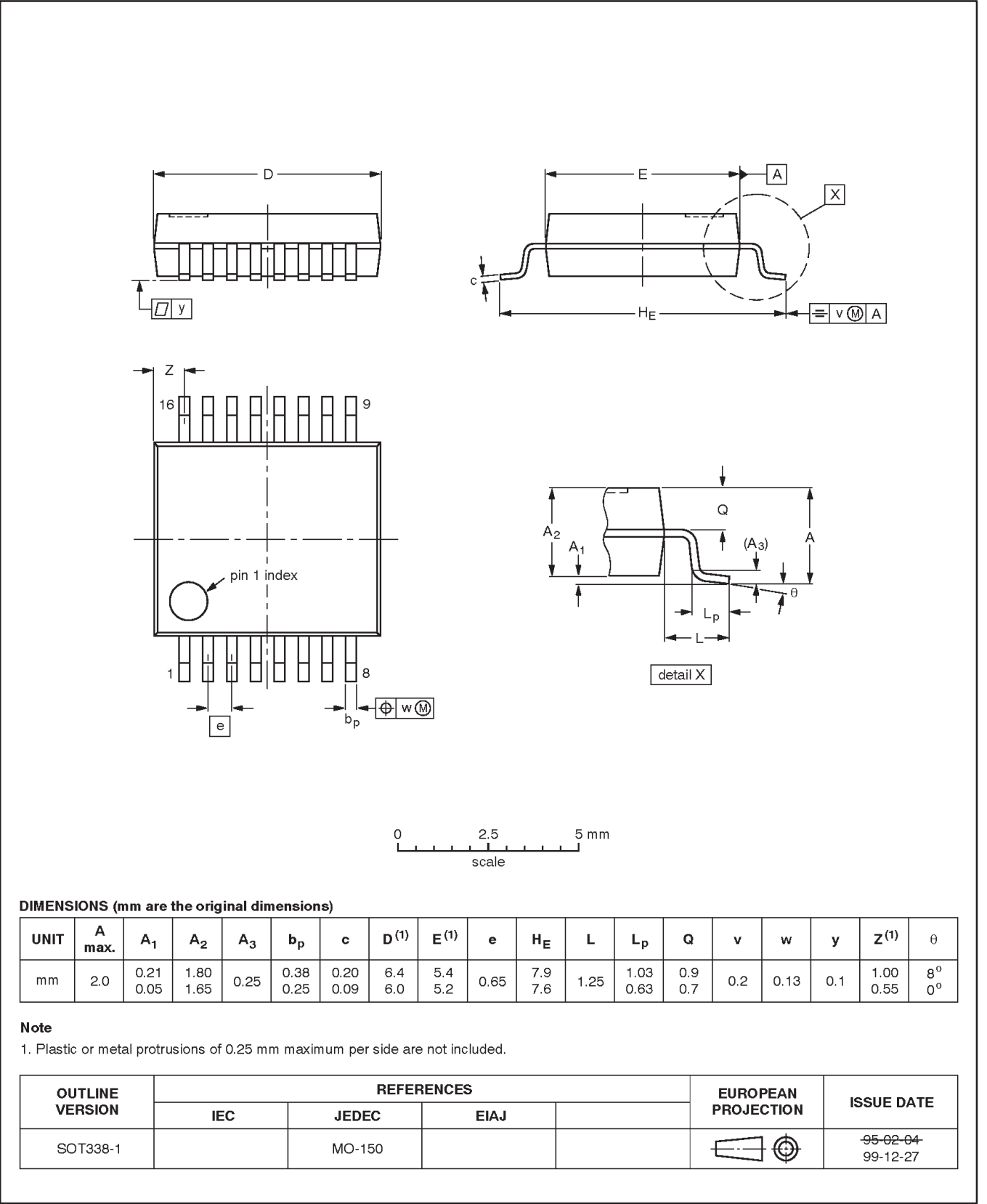


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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

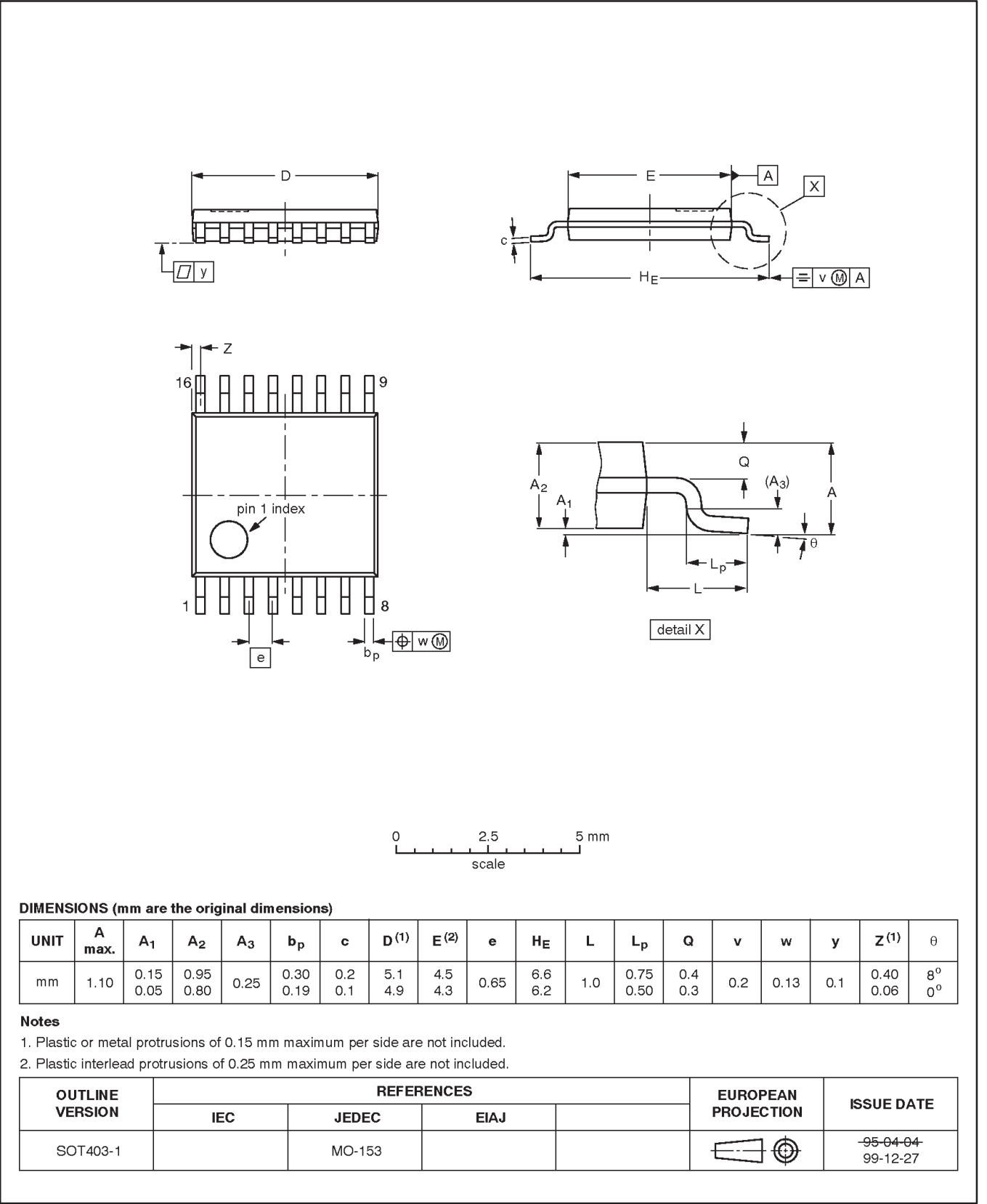


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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



## Dual 2-to-4 line decoder/demultiplexer

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## REVISION HISTORY

Rev	Date	Description
_3	20030313	<b>Product data (9397 750 11245). ECN 853-1922 29492 of 07 February 2003.</b> <b>Supersedes Product specification of 1998 Apr 20 (9397 750 04424).</b>  Modifications: <ul style="list-style-type: none"><li>• Quick Reference Data: Correct power dissipation formula in Note 1.</li><li>• Ordering information: delete "North America"column; rename column from "Outside North America" to "Order Code".</li><li>• Pin configuration diagram: correct pin number labels .</li></ul>
_2	19980428	<b>Product specification (9397 750 04424). ECN 853-1922 19290 of 28 April 1998.</b> <b>Supersedes data of 1997 Feb 12.</b>

## Dual 2-to-4 line decoder/demultiplexer

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## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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