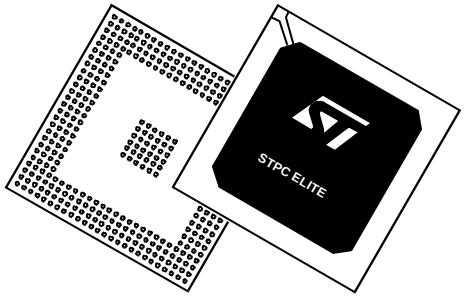
STPC® ELITE

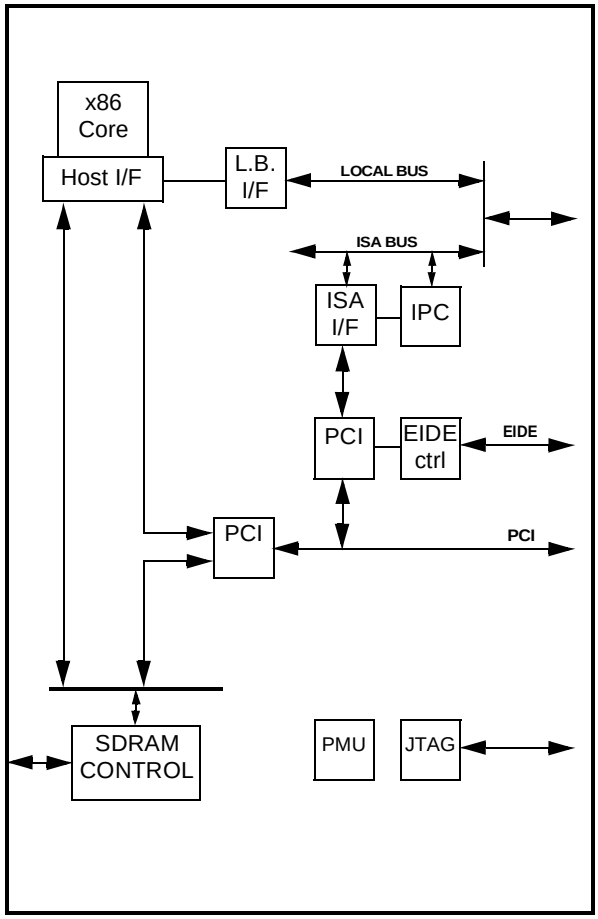
X86 Core General Purpose PC Compatible System - on - Chip

- POWERFUL X86 PROCESSOR
- 64-BIT SDRAM CONTROLLER
- PCI MASTER / SLAVE CONTROLLER
- ISA MASTER/SLAVE
- 16-BIT LOCAL BUS INTERFACE
- EIDE CONTROLLER
- INTEGRATED PERIPHERAL CONTROLLER
  - DMA CONTROLLER
  - INTERRUPT CONTROLLER
  - TIMER / COUNTERS
- POWER MANAGEMENT UNIT
- I²C INTERFACE
- 16 GENERAL PURPOSE I/O.
- JTAG IEEE1149.1
- PROGRAMMABLE OUTPUT CLOCK



PBGA388

Logic Diagram



DESCRIPTION

The STPC Elite integrates a fully static x86 processor, fully compatible with standard x86 processors, and combines it with powerful chipset to provide a general purpose PC compatible subsystem on a single device. The device is packaged in a 388 Ball Grid Array (PBGA).

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8KByte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Clock core speeds up to of 100 MHz in x1 clock mode and 133MHz in x2 mode.
- Fully static design for dynamic clock control.
- Low power and system management modes.

- **SDRAM Controller**
- 64-bit data bus.
- Up to 100MHz SDRAM clock speed.
- Supports 8MB up to 128 MB system memory.
- Supports 16-, 64- and 128-Mbit memories.
- Supports up to 4 memory banks.
- Supports buffered, non buffered, registered DIMMs
- 4-line write buffers for CPU to DRAM and PCI to DRAM cycles.
- 4-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for DRAM parameters.
- Supports -8, -10, -12, -13, -15 memory parts
- Supports memory hole between 1MB and 8MB for PCI/ISA busses.

- **PCI Controller**
- Compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External logic allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- 0.25X, 0.33X and 0.5X Host clock PCI clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus. NSP compliant.
- 16-bit I/O decoding.

- **Local Bus interface**
- Multiplexed with ISA/DMA/Timer functions.
- High speed, low latency bus.
- Supports 32-bit Flash burst.
- 16-bit data bus with word steering capability.
- Separate memory and I/O address spaces.
- Programmable timing (Host clock granularity)
- Supports 2 cashable banks of 16MB flash devices with boot block shadowed to 0x000F0000.
- 2 Programmable Flash/EPROM Chip Select.
- 4 Programmable I/O Chip Select.
- 2-level hardware key protection for Flash boot block protection.
- 22 bit address bus.

- **EIDE Controller**
- Compatible with EIDE (ATA-2).
- Backward compatibility with IDE (ATA-1).
- Supports up to 4 IDE devices
- Supports PIO and Bus Master IDE
- Concurrent channel operation (PIO & DMA modes) - 4 x 32-Bit Buffer FIFO per channel
- Support for 11.1/16.6 MB/s, I/O Channel Ready PIO data transfers.
- Bus Master with scatter/gather capability.
- Multi-word DMA support for fast IDE drives.
- Individual drive timing for all four IDE devices.
- Supports both legacy & native IDE modes.
- Supports hard drives larger than 528MB.
- Support for CD-ROM and tape peripherals.

- **Integrated Peripheral Controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.
- Supports external RTC.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports SMM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel ports.
- Supports RTC, interrupts and DMAs wake-up

- **GPIOs**
- 16 General Purpose IO.

- **JTAG Function**

- **Programmable GP-Clock**
- This clock is programmable to frequencies up to 135 MHz.