3.3 VOLT TIME SLOT INTERCHANGE DIGITAL SWITCH 8,192 x 8,192

PRELIMINARY
IDT72V71650

FEATURES:

- 8K x 8K non-blocking switching at 16.384Mb/s
- 32 serial input and output streams
- Accepts data streams at 2.048Mb/s, 4.096Mb/s, 8.192Mb/s or 16.384Mb/s
- Per-channel Variable Delay Mode for low-latency applications
- Per-channel Constant Delay Mode for frame integrity applications
- Automatic identification of ST-BUS® and GCI bus interfaces
- Automatic frame offset delay measurement
- Per-stream frame delay offset programming
- Per-channel high-impedance output control
- Direct microprocessor access to all internal memories
- Memory block programming for quick setup
- IEEE-1149.1 (JTAG) Test Port
- 3.3V Power Supply
- Available in 144-pin (13mm x 13mm) Plastic Ball Grid Array (PBGA) and 144-pin (20mm x 20mm) Thin Quad Flatpack (TQFP) packages
- Operating Temperature Range -40°C to +85°C

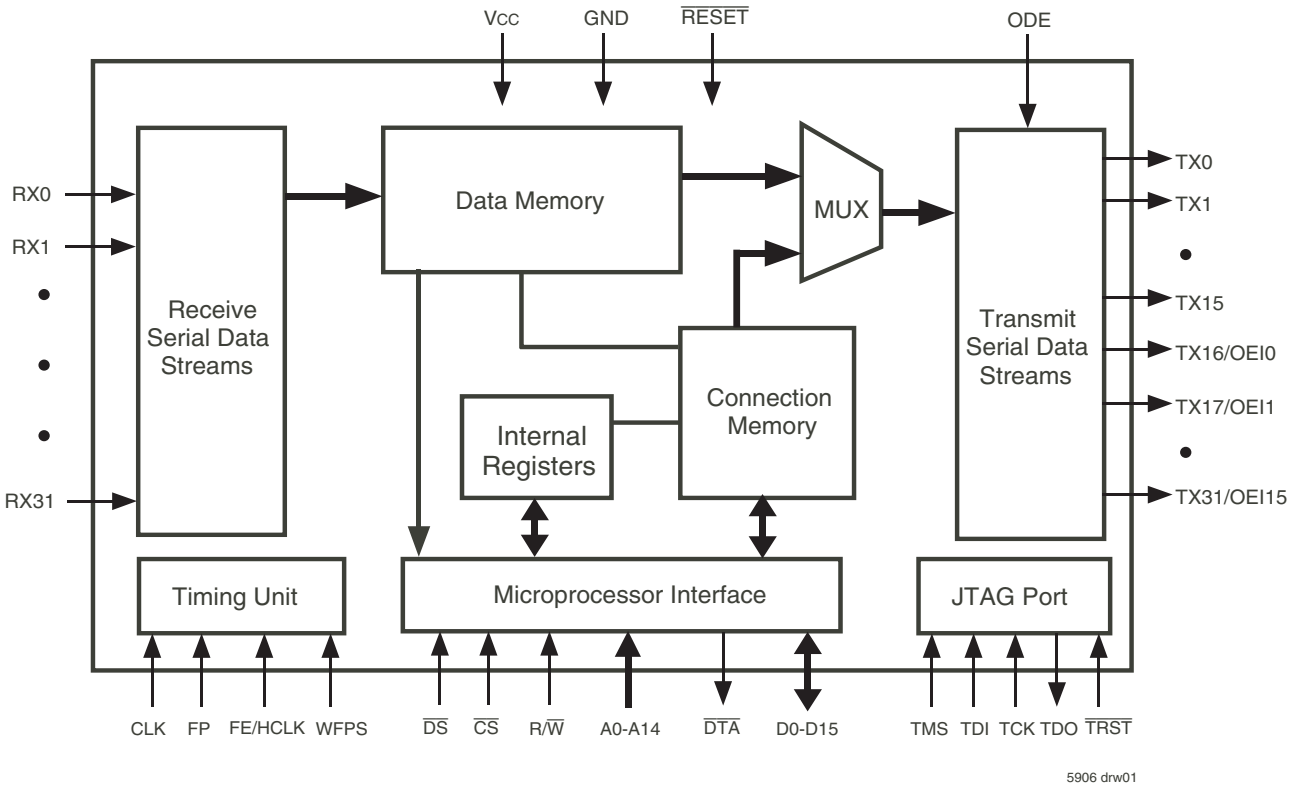
DESCRIPTION:

The IDT72V71650 has a non-blocking switch capacity of 1,024 x 1,024 channels at 2.048Mb/s, 2,048 x 2,048 channels at 4.096Mb/s, and 4,096 x 4,096 channels at 8.192Mb/s and 8,192 x 8,192 channels at 16.384Mb/s. With 32 inputs and 32 outputs, programmable per stream control, and a variety of operating modes the IDT72V71650 is designed for the TDM time slot interchange function in either voice or data applications.

Some of the main features of the IDT72V71650 are low power 3.3 Volt operation, automatic ST-BUS® /GCI sensing, memory block programming, simple microprocessor interface, one cycle direct internal memory accesses, JTAG Test Access Port (TAP) and per stream programmable input offset delay, variable or constant throughput modes, output enable and processor mode.

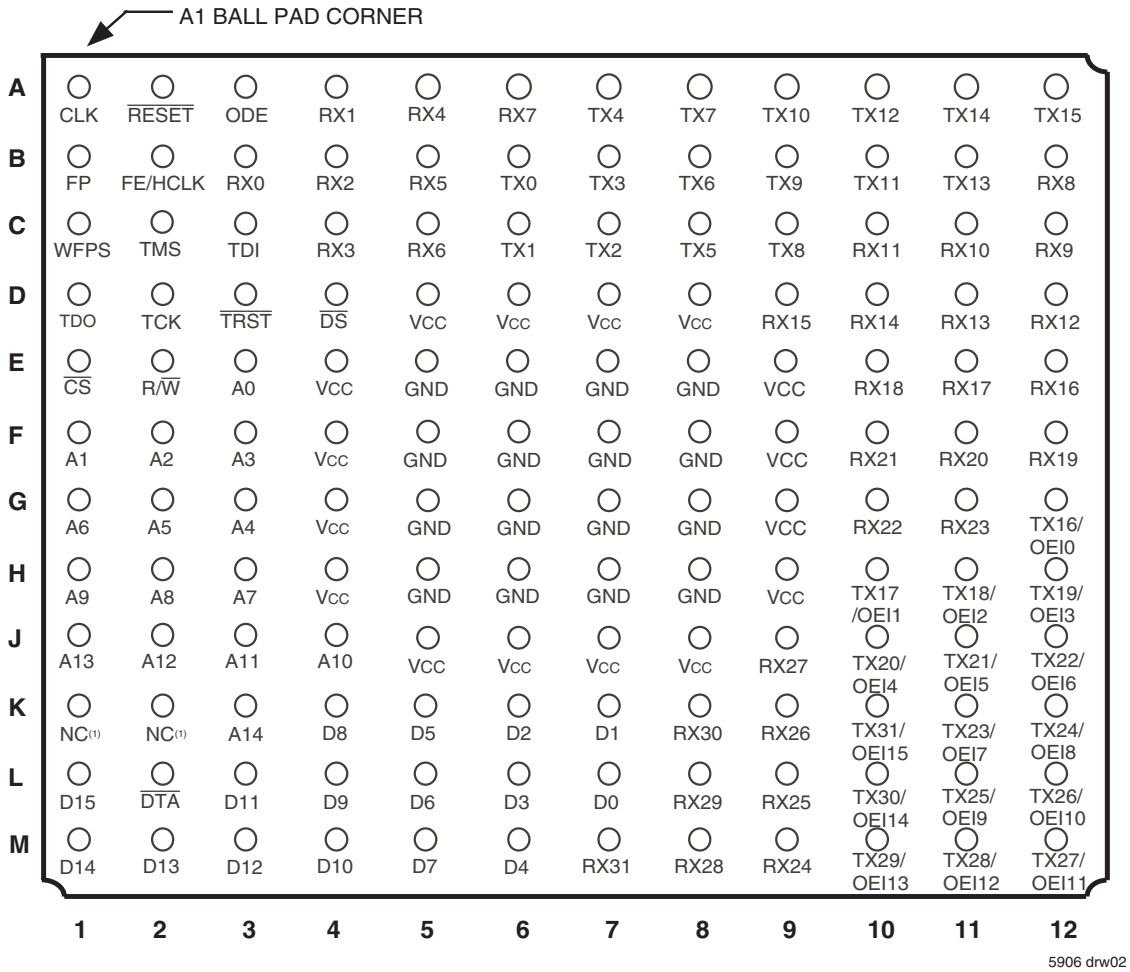
The IDT72V71650 is capable of switching up to 8,192 x 8,192 channels without blocking. Designed to switch 64 Kbit/s PCM or N x 64 Kbit/s data, the device maintains frame integrity in data applications and minimizes throughput delay for voice applications on a per-channel basis.

FUNCTIONAL BLOCK DIAGRAM



5906 drw01

PIN CONFIGURATIONS

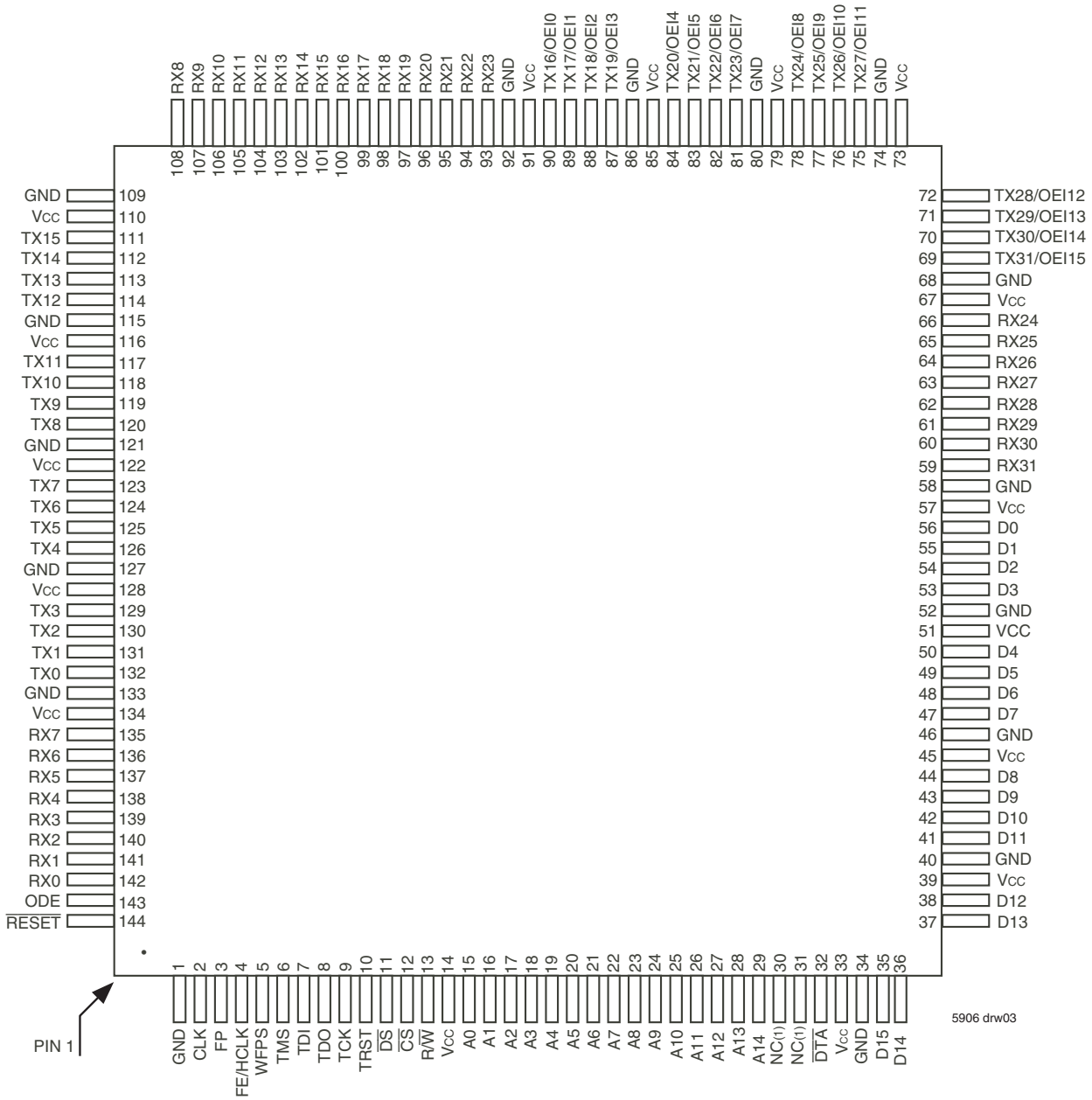


5906 drw02

PBGA: 1mm pitch, 13mm x 13mm (BB144-1, order code: BB)
TOP VIEW

NOTE:
1. NC = No Connect

PIN CONFIGURATIONS (CONTINUED)



TQFP: 0.50mm pitch, 20mm x 20mm (DA144-1, order code: DA)
TOP VIEW

NOTE:
1. NC = No Connect

PIN DESCRIPTION

SYMBOL	NAME	I/O	DESCRIPTION
A0-14	Address 0 to 14	I	These address lines access all internal memories.
CLK	Clock	I	Serial clock for shifting data in/out on the serial data streams. Depending upon the value programmed, this input accepts a 4.096, 8.192 or 16.384 MHz clock. See the Control Register bits on Table 5 for the values.
$\overline{CS}$	Chip Select	I	This active LOW input is used by a microprocessor to activate the microprocessor port of IDT72V71650.
D0-15	Data Bus 0-15	I/O	These pins are the data bits of the microprocessor port.
$\overline{DS}$	Data Strobe	I	This active LOW input works in conjunction with $\overline{CS}$ to enable the read and write operations and enables the data bus lines (D0-D15).
$\overline{DTA}$	Data Transfer Acknowledgment	O	Indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then goes high-impedance, allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is in high-impedance.
FE/HCLK	Frame Evaluation/ HCLK Clock	I	When the WFPS pin is LOW, this pin is the frame measurement input. When the WFPS pin is HIGH, the HCLK (4.096 MHz clock) is required for frame alignment in the wide frame pulse mode (WFPS).
FP	Frame Pulse	I	When the WFPS pin is LOW, this input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS® and GCI specifications. When pin WFPS is HIGH, this pin accepts a negative frame pulse, which conforms to the WFPS format.
GND	Ground		Ground Rail.
ODE	Output Drive Enable	I	This is the output enable control for the TX serial outputs. When the ODE input is LOW and the Output Stand By bit of the Control Register is LOW, all TX outputs are in a high-impedance state. If this input is HIGH, the TX output drivers are enabled. However, each channel may still be put into a high-impedance state by using the per-channel control bit in the Connection Memory.
$\overline{RESET}$	Device Reset	I	This input puts the IDT72V71650 into a reset state that clears the device internal counters, registers and brings TX0-31 and D0-D15 into a high-impedance state. The $\overline{RESET}$ pin must be held LOW for a minimum of 20ns to properly reset the device.
R/$\overline{W}$	Read/Write	I	This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
RX0-31	Data Stream	I	Serial data input stream. These streams may have a data rate of 2.048Mb/s, 4.096Mb/s, 8.192Mb/s, or 16.384Mb/s, depending upon the value programmed in the Control Register.
TCK	Test Clock	I	Provides the clock to the JTAG test logic.
TDI	Test Serial Data In	I	JTAG serial test instructions and data are shifted in on this pin. This pin is pulled HIGH by an internal pull-up when not driven.
TDO	Test Serial Data Out	O	JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high-impedance state when JTAG scan is not enabled.
TMS	Test Mode Select	I	JTAG signal that controls the state transitions of the TAP controller. This pin is pulled HIGH by an internal pull-up when not driven.
$\overline{TRST}$	Test Reset	I	Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin is pulled by an internal pull-up when not driven. This pin should be pulsed LOW on power-up, or held LOW, to ensure that the IDT72V71650 is in the normal functional mode.
TX0-15	TX Output 0 to 15 (Three-state Outputs)	O	Serial data output stream. These streams may have a data rate of 2.048Mb/s, 4.096Mb/s, 8.192Mb/s, or 16.384Mb/s, depending upon the value programmed in the Control Register.
TX16-31/ OEI0-15	TX Output 16 to 31/ Output Enable Indication 0 to 15 (Three-State Outputs)	O	When all 32 outputs streams are selected via Control Register, these pins are the output streams TX16 to TX31 and may operate at a data rate of 2.048Mb/s, 4.096Mb/s, 8.192Mb/s, or 16.384Mb/s. When output enable function is selected, these pins reflect the active or high-impedance status for the corresponding output stream OEI0-31.
Vcc	Vcc		+3.3 Volt Power Supply.
WFPS	Wide Frame Pulse Select	I	When 1, enables the wide frame pulse (WFPS) Frame Alignment interface. When 0, the device operates in ST-BUS®/GCI mode.

DESCRIPTION (CONTINUED)

The 32 serial input streams (RX) of the IDT72V71650 can run up to 16.384Mb/s allowing 256 channels per 125µs frame. The data rates on the output streams (TX) are identical to those on the input streams (RX).

With two main operating modes, Processor Mode and Connection Mode, the IDT72V71650 can easily switch data from incoming serial streams (Data Memory) or from the controlling microprocessor via Connection Memory. As control and status information is critical in data transmission, the Processor Mode is especially useful when there are multiple devices sharing the input and output streams.

With data coming from multiple sources and through different paths, data entering the device is often delayed. To handle this problem, the IDT72V71650 has a Frame Evaluation feature to allow individual streams to be offset from the frame pulse in half clock-cycle intervals up to +7.5 clock cycles.

The IDT72V71650 also provides a JTAG test access port, memory block programming, a simple microprocessor interface and automatic ST-BUS®/GCI sensing to shorten setup time, aid in debugging and ease use of the device without sacrificing capabilities.

FUNCTIONAL DESCRIPTION

DATA AND CONNECTION MEMORY

All data that comes in through the RX inputs go through a serial-to-parallel conversion before being stored into internal Data Memory. The 8 KHz frame pulse (FP) is used to mark the 125µs frame boundaries and to sequentially address the input channels in Data Memory.

Data output on the TX streams may come from either the serial input streams (Data Memory) or from the microprocessor (Connection Memory). In the case that RX input data is to be output, the addresses in Connection Memory are used to specify a stream and channel of the input. The Connection Memory is setup in such a way that each location corresponds to an output channel for each particular stream. In that way, more than one channel can output the same data. In Processor Mode, the microprocessor writes data to the Connection Memory locations corresponding to the stream and channel that is to be output. The lower half (8 least significant bits) of the Connection Memory is output every frame until the microprocessor changes the data or mode of the channel. By using this Processor Mode capability, the microprocessor can access input and output time-slots on a per-channel basis.

The two most significant bits of the Connection Memory are used to control the per-channel mode of the out put streams. Specifically, the MOD1-0 bits are used to select Processor Mode, Constant or Variable delay Mode, and the high-impedance state of output drivers. If the MOD1-0 bits are set to 1-1 accordingly, only that particular output channel (8 bits) will be in the high-impedance state. If however, the ODE input pin is LOW and the Output Standby Bit in the Control Register is LOW, all of the outputs will be in a high-impedance state even if a particular channel in Connection Memory has enabled the output for that channel. In other words, the ODE pin and Output Stand By control bit are master output enables for the device (See Table 3).

SERIAL DATA INTERFACE TIMING

When a 16.384Mb/s serial data rate is required, the master clock frequency will be running at 16.384 MHz resulting in a single-bit per clock. For all other cases, 2.048Mb/s, 4.096Mb/s, and 8.192Mb/s, the master clock frequency will be twice the data rate on the serial streams, resulting in two clocks per bit. Use Table 5 to determine clock speed and the DR1-0 bits in the Control Register to setup the device. The IDT72V71650 provides two different interface timing modes, ST-BUS® or GCI. The IDT72V71650 automatically detects the presence of an input frame pulse and identifies it as either ST-BUS® or GCI.

In ST-BUS®, when running at 16.384 MHz, data is clocked out on the falling edge and is clocked in on the subsequent rising-edge. At all other data rates, there are two clock cycles per bit and every second falling edge of the master clock marks a bit boundary and the data is clocked in on the rising edge of CLK, three quarters of the way into the bit cell. See Figure 13 for timing.

In GCI format, when running at 16.384 MHz, data is clocked out on the rising edge and is clocked in on the subsequent falling edge. At all other data rates, there are two clock cycles per bit and every second rising edge of the master clock marks the bit boundary and data is clocked in on the falling edge of CLK at three quarters of the way into the bit cell. See Figure 14 for timing.

INPUT FRAME OFFSET SELECTION

Input frame offset selection allows the channel alignment of individual input streams to be offset with respect to the output stream channel alignment. Although all input data comes in at the same speed, delays can be caused by variable path serial backplanes and variable path lengths which may be implemented in large centralized and distributed switching systems. Because data is often delayed, this feature is useful in compensating for the skew between input streams.

Each input stream can have its own delay offset value by programming the frame input offset registers (FOR, Table 8). The maximum allowable skew is +7.5 master clock (CLK) periods forward with a resolution of ½ clock period, see Table 9. The output frame cannot be adjusted.

SERIAL INPUT FRAME ALIGNMENT EVALUATION

The IDT72V71650 provides the Frame Evaluation input to determine different data input delays with respect to the frame pulse FP. A measurement cycle is started by setting the Start Frame Evaluation bit of the Control Register LOW for at least one frame. When the Start Frame Evaluation bit in the Control Register is changed from LOW to HIGH, the evaluation starts. Two frames later, the Complete Frame Evaluation bit of the Frame Alignment Register changes from LOW to HIGH to signal that a valid offset measurement is ready to be read from bits 0 to 11 of the Frame Alignment Register. The Start Frame Evaluation bit must be set to zero before a new measurement cycle is started.

In ST-BUS® mode, the falling edge of the frame measurement signal (Frame Evaluation) is evaluated against the falling edge of the ST-BUS® frame pulse. In GCI mode, the rising edge of Frame Evaluation is evaluated against the rising edge of the GCI frame pulse. See Table 7 and Figure 1 for the description of the Frame Alignment Register.

MEMORY BLOCK PROGRAMMING

The IDT72V71650 provides users with the capability of initializing the entire Connection Memory block in two frames. To set bits 14 and 15 of every Connection Memory location, first program the desired pattern in the Block Programming Data Bits (BPD 1-0), located in bits 7 and 8 of the Control Register.

The block programming mode is enabled by setting the Memory Block Program bit of the Control Register HIGH. When the Block Programming Enable bit of the Control Register is set to HIGH, the Block Programming Data will be loaded into the bits 14 and 15 of every Connection Memory location. The other Connection Memory bits (bit 0 to bit 13) are loaded with zeros. When the memory block programming is complete, the device resets the Block Programming Enable, Block Programming Data 1-0 and Memory Block Program bits to zero.

DELAY THROUGH THE IDT72V71650

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time-slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, variable throughput delay is best as it ensures minimum delay between input and output data. In wideband data applications, constant throughput delay is best as the frame integrity of the information is maintained through the switch.

The delay through the device varies according to the type of throughput delay selected in the MOD bits of the Connection Memory.

VARIABLE DELAY MODE (MOD1-0 = 0-0)

In this mode, the delay is dependent only on the combination of source and destination channels and is independent of input and output streams. The minimum delay achievable in the IDT72V71650 is three time-slots. If the input channel data is switched to the same output channel (channel n, frame p), it will be output in the following frame (channel n, frame p+1). The same is true if the input channel n is switched to output channel n+1 or n+2. If the input channel n is switched to output channel n+3, n+4,..., the new output data will appear in the same frame. Table 2 shows the possible delays for the IDT72V71650 in Variable Delay mode.

CONSTANT DELAY MODE (MOD1-0 = 0-1)

In this mode, frame integrity is maintained in all switching configurations by making use of a multiple data memory buffer. Input channel data is written into the data memory buffers during frame n will be read out during frame n+2. In the IDT72V71650, the minimum throughput delay achievable in Constant Delay mode will be one frame plus one channel. See Table 1.

MICROPROCESSOR INTERFACE

The IDT72V71650's microprocessor interface looks like a standard RAM interface to improve integration into a system. With a 15-bit address bus and a 16-bit data bus, reads and writes are mapped directly into Data and Connection Memories and require only one clock cycle to access. By allowing the internal memories to be randomly accessed in one cycle, the controlling microprocessor has more time to manage other peripheral devices and can more easily and quickly gather information and setup the switch paths. Table 4 shows the mapping of the addresses into internal memory blocks.

MEMORY MAPPING

The address bus on the microprocessor interface selects the internal registers and memories of the IDT72V71650.

The two most significant bits of the address select between the registers, Data Memory, and Connection Memory. If A14 and A13 are HIGH, A12-A0 are used to address the Data Memory. If A14 is HIGH and A13 is LOW, A12-A0 are used to address Connection Memory. If A14 is LOW and A13 is HIGH A12-A0 are used to select the Control Register, Frame Alignment Register, and Frame Offset Registers. See Table 4 for mappings.

As explained in the Serial Data Interface Timing and Switching Configurations sections, after system power-up, the Control Register should be programmed immediately to establish the desired switching configuration.

The data in the Control Register consists of the Memory Block Programming bit, the Block Programming Data bits, the Begin Block Programming Enable, the Output Stand By, Start Frame Evaluation, Output Enable Indication, and Data Rate Select bits. As explained in the Memory Block Programming section, the Block Programming Enable begins the programming if the Memory Block Program bit is enabled. This allows the entire Connection Memory block to be programmed with the Block Programming Data bits. If the ODE pin is LOW, the Output Stand By bit enables (if HIGH) or disables (if LOW) all TX output drivers. If the ODE pin is HIGH, the Output Stand By bit is ignored and all TX output drivers are enabled.

SOFTWARE RESET

The Software Reset serves the same function as the hardware reset. As with the hard reset, the Software Reset must also be set HIGH for 20ns before bringing the Software Reset LOW again for normal operation. Once the Software Reset is LOW, internal registers and other memories may be read or written. During Software Reset, the microprocessor port is still able to read from all internal memories. The only write operation allowed during a Software Reset is to the Software Reset bit in the Control Register to complete the Software Reset.

CONNECTION MEMORY CONTROL

If the ODE pin and the Output Stand By bit are LOW, all output channels will be in three-state. See Table 3 for detail.

If MOD1-0 of the Connection Memory is 1-0 accordingly, the output channel will be in Processor Mode. In this case the lower eight bits of the Connection Memory are output each frame until the MOD1-0 bits are changed. If MOD 1-0 of the Connection Memory are 0-1 accordingly, the channel will be in Constant Delay Mode and bits 12-0 are used to address a location in Data Memory. If MOD1-0 of the Connection Memory are 0-0, the channel will be in Variable Delay Mode and bits 12-0 are used to address a location in Data Memory. If MOD 1-0 of the Connection Memory are 1-1, the channel will be in High-Impedance mode and that channel will be in three-state.

OUTPUT ENABLE INDICATION

The IDT72V71650 has the capability to indicate the state of the outputs (active) or three-state) by enabling the Output Enable Indication in the Control Register. In the Output Enable Indication mode however, only half of the output streams are available. If this same capability is desired with all 32 streams, this can be accomplished by using two IDT72V71650 or one IDT72V71660 devices. In one device, the All Output Enable bit is set to a one while in the other the All Output Enable is set to zero. In this way, one device acts as the switch and the other as a three-state control device, see Figure 4. It is important to note if the TSI device is programmed for All Output Enable and the Output Enable Indication is also set, the device will be in the All Output Enable mode not Output Enable Indication.

INITIALIZATION OF THE IDT72V71650

After power up, the state of the Connection Memory is unknown. As such, the outputs should be put in high-impedance by holding the ODE pin LOW. While the ODE is LOW, the microprocessor can initialize the device by using the Block Programming feature and program the active paths via the microprocessor bus. Once the device is configured, the ODE pin (or Output Stand By bit depending on initialization) can be switched to enable the TSI switch.

TABLE 1 — CONSTANT THROUGHPUT DELAY VALUE

Input Rate	Delay for Constant Throughput Delay Mode (m – output channel number) (n – input channel number)
2.048Mb/s	32 + (32 – n) +m time-slots
4.096Mb/s	64 + (64 – n) +m time-slots
8.192Mb/s	128 + (128 – n) +m time-slots
16.384Mb/s	256 + (256 – n) +m time-slots

TABLE 2 — VARIABLE THROUGHPUT DELAY VALUE

Input Rate	Delay for Variable Throughput Delay Mode (m – output channel number; n – input channel number)	
	m ≤ n+2	m > n+2
2.048Mb/s	32 – (n-m) time-slots	(m-n) time-slots
4.096Mb/s	64 – (n-m) time-slots	(m-n) time-slots
8.192Mb/s	128 – (n-m) time-slots	(m-n) time-slots
16.384Mb/s	256 – (n-m) time-slots	(m-n) time-slots

TABLE 3 — OUTPUT HIGH-IMPEDANCE CONTROL

Bits MOD1-0 Values in Connection Memory	ODE pin	OSB bit in Control Register	Output Status
1 and 1	Don't Care	Don't Care	Per-channel High-Impedance
Any, other than 1 and 1	0	0	High-Impedance
Any, other than 1 and 1	0	1	Enable
Any, other than 1 and 1	1	0	Enable
Any, other than 1 and 1	1	1	Enable

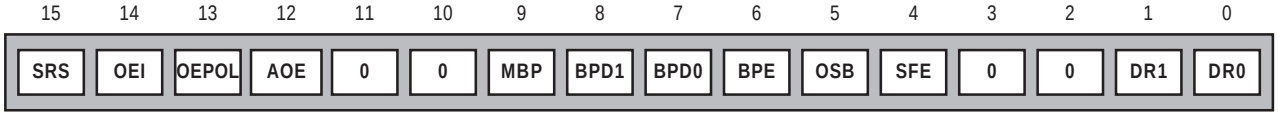
TABLE 4 — INTERNAL REGISTER AND ADDRESS MEMORY MAPPING

A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	Location
1	1	STA4	STA3	STA2	STA1	STA0	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	R	Data Memory
1	0	STA4	STA3	STA2	STA1	STA0	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	R/W	Connection Memory
0	1	0	0	0	0	x	x	x	x	x	x	x	x	x	R/W	Control Register
0	1	0	0	0	1	x	x	x	x	x	x	x	x	x	R	Frame Align Register
0	1	1	0	0	0	x	x	x	x	x	x	x	x	x	R/W	Frame Offset Register 0
0	1	1	0	0	1	x	x	x	x	x	x	x	x	x	R/W	Frame Offset Register 1
0	1	1	0	1	0	x	x	x	x	x	x	x	x	x	R/W	Frame Offset Register 2
0	1	1	0	1	1	x	x	x	x	x	x	x	x	x	R/W	Frame Offset Register 3
0	1	1	1	0	0	x	x	x	x	x	x	x	x	x	R/W	Frame Offset Register 4
0	1	1	1	0	1	x	x	x	x	x	x	x	x	x	R/W	Frame Offset Register 5
0	1	1	1	1	0	x	x	x	x	x	x	x	x	x	R/W	Frame Offset Register 6
0	1	1	1	1	1	x	x	x	x	x	x	x	x	x	R/W	Frame Offset Register 7

NOTE: Unused STA and CH bits should be set to zero.

TABLE 5 — CONTROL REGISTER (CR) BITS

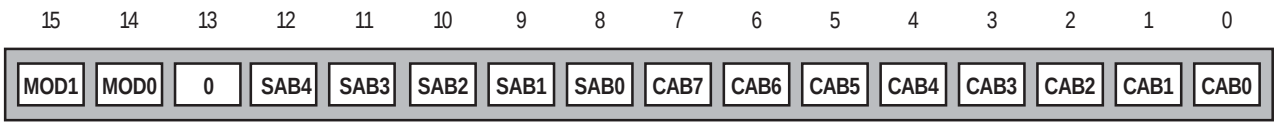
Reset Value: 0000_H.



BIT	NAME	DESCRIPTION
15	SRS (Software Reset)	A one will reset the device and have the same effect as the RESET pin. Must be zero for normal operation.
14	OEI (Output Enable Indication)	When 1, the TX16-31/OEI0-15 pins will be OEI0-15 and reflect the active or high-impedance state of their corresponding output data streams. When 0, this feature is disabled and these pins are used as output data streams TX16-31.
13	OEPOL (Output Enable Polarity)	When 1, a one on an Output Enable Indication pin denotes an active state on the output data stream; zero on an Output Enable Indication pin denotes high-impedance state. When 0, a one on an Output Enable Indication pin denotes high-impedance and a zero denotes an active state.
12	AOE (All Output Enables)	When 1, TX0-31 will behave as OEI0-31 accordingly. These outputs will reflect the active or high-impedance state of the corresponding output data streams (TX0-31) in another IDT72V71650 if programmed identically. When 0, the TSI operates in the normal switch mode.
11-10	Unused	Must be zero for normal operation.
9	MBP (Memory Block Program)	When 1, the Connection Memory block programming feature is ready for the programming of Connection Memory HIGH bits, bit 14 to bit 15. When 0, this feature is disabled.
8-7	BPD1-0 (Block Programming Data)	These bits carry the value to be loaded into the Connection Memory block whenever the memory block programming feature is activated. After the Memory Block Program bit in the Control Register is set to 1 and the Block Programming Enable is set to 1, the contents of the bits Block Programming Data1-0 are loaded into bit 15 and 14 of the Connection Memory. Bit 13 to bit 0 of the Connection Memory are set to 0.
6	BPE (Begin Block Programming Enable)	A zero to one transition of this bit enables the memory block programming function. The Block Programming Enable and Block Programming Data1-0 bits in the Control Register have to be defined in the same write operation. Once the Block Programming Enable bit is set HIGH, the device requires two frames to complete the block programming. After the programming function has finished, the Block Programming Enable, Memory Block Program and Block Programming Data 1-0 bits will be reset to zero by the device to indicate the operation is complete.
5	OSB (Output Stand By)	When ODE = 0 and Output Stand By = 0, the output drivers of the transmit serial streams are in high-impedance mode. When either ODE = 1 or Output Stand By =1 the output serial streams drivers function normally.
4	SFE (Start Frame Evaluation)	A zero to one transition in this bit starts the Frame Evaluation procedure. When the Complete Frame Evaluation bit in the Frame Alignment Register changes from zero to one, the evaluation procedure stops. To start another Frame Evaluation cycle, set this bit to zero for at least one frame.
3-2	Unused	Must be zero for normal operation.
1-0	DR1-0	

DR1	DR0	Data Rate	Master Clock
0	0	2.048Mb/s	4.096 MHz
0	1	4.096Mb/s	8.192 MHz
1	0	8.192Mb/s	16.384 MHz
1	1	16.384Mb/s	16.384 MHz

TABLE 6 — CONNECTION MEMORY BITS



Bit	Name	Description
15, 14	MOD1-0 (Switching Mode Selection)	MOD1 MOD0 MODE 0 0 Variable Delay mode 0 1 Constant Delay mode 1 0 Processor mode 1 1 Output High-impedance
13	Unused	Must be zero for normal operation.
12-8	SAB4-0 (Source Stream Address Bits)	The binary value is the number of the data stream for the source of the connection.
7-0	CAB7-0 (Source Channel Address Bits)	The binary value is the number of the channel for the source of the connection.

NOTE:
1. Unused SAB and CAB bits should be set to zero.

TABLE 7 — FRAME ALIGNMENT REGISTER (FAR) BITS

Reset Value: 0000H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	CFE	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Bit	Name	Description
15-13	Unused	Must be zero for normal operation.
12	CFE (Complete Frame Evaluation)	When Complete Frame Evaluation = 1, the Frame Evaluation is completed and bits FD11 to FD0 bits contains a valid frame alignment offset. This bit is reset to zero, when Start Frame Evaluation bit in the Control Register is changed from 1 to 0.
11	FD11 (Frame Delay Bit 11)	The falling edge of Frame Evaluation (or rising edge for GCI mode) is sampled during the CLK-HIGH phase (FD11 = 1) or during the CLK-LOW phase (FD11 = 0). This bit allows the measurement resolution to ½ CLK cycle. This bit is reset to zero when the Start Frame Evaluation bit of the Control Register changes from 1 to 0.
10-0	FD10-0 (Frame Delay Bits)	The binary value expressed in these bits refers to the measured input offset value. These bits are reset to zero when the Start Frame Evaluation bit of the Control Register changes from 1 to 0. (FD10 – MSB, FD0 – LSB)

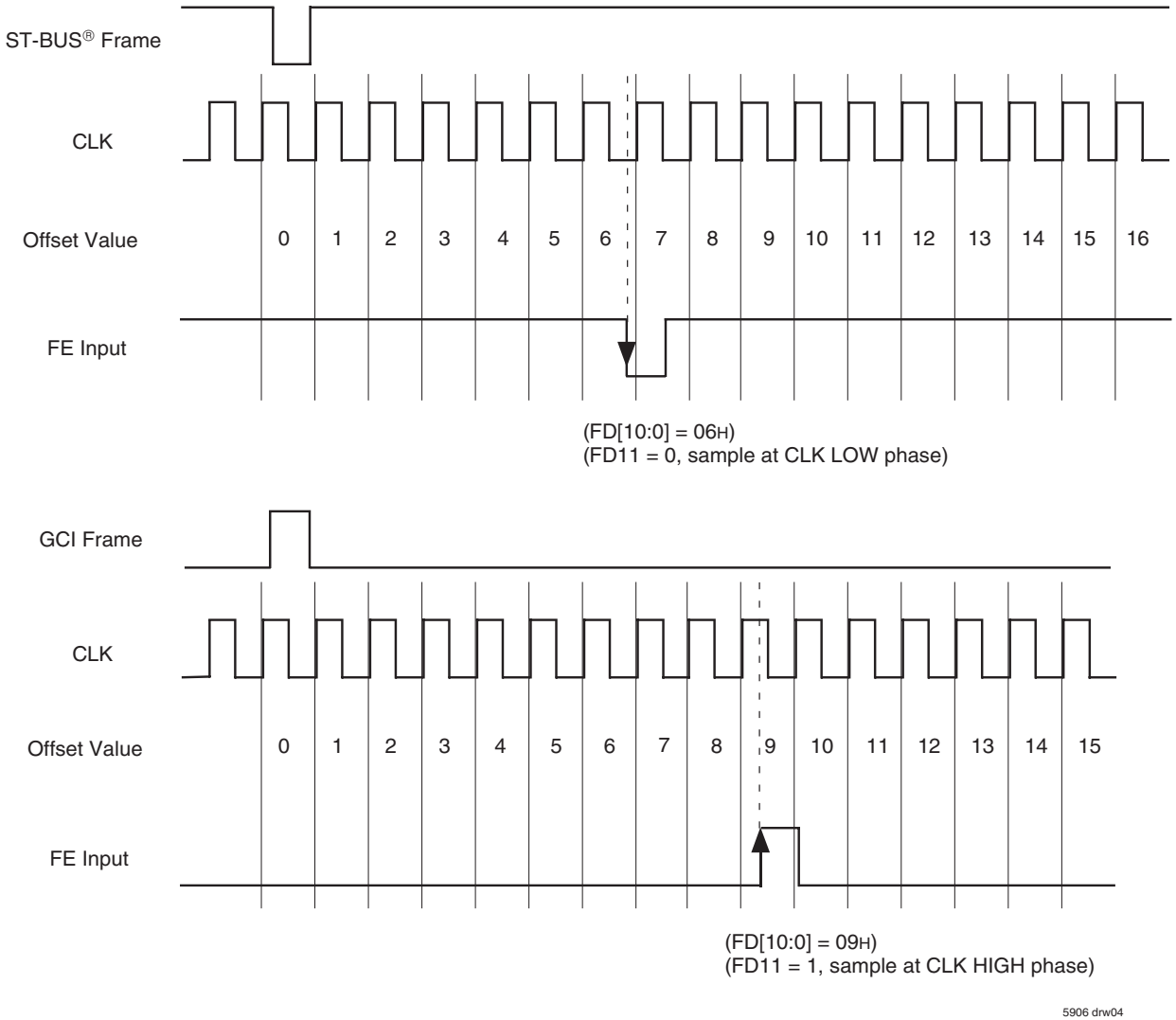


Figure 1. Example for Frame Alignment Measurement

TABLE 8 — FRAME INPUT OFFSET REGISTER (FOR) BITS

Reset Value: 0000_H for all FOR registers.

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOR0 Register	OF32	OF31	OF30	DLE3	OF22	OF21	OF20	DLE2	OF12	OF11	OF10	DLE1	OF02	OF01	OF00	DLE0
FOR1 Register	OF72	OF71	OF70	DLE7	OF62	OF61	OF60	DLE6	OF52	OF51	OF50	DLE5	OF42	OF41	OF40	DLE4
FOR2 Register	OF112	OF111	OF110	DLE11	OF102	OF101	OF100	DLE10	OF92	OF91	OF90	DLE9	OF82	OF81	OF80	DLE8
FOR3 Register	OF152	OF151	OF150	DLE15	OF142	OF141	OF140	DLE14	OF132	OF131	OF130	DLE13	OF122	OF121	OF120	DLE12
FOR4 Register	OF192	OF191	OF190	DLE19	OF182	OF181	OF180	DLE18	OF172	OF171	OF170	DLE17	OD162	OD161	OF160	DLE16
FOR5 Register	OF232	OF231	OF230	DLE23	OF222	OF221	OF220	DLE22	OF212	OF211	OF210	DLE21	OF202	OF201	OF200	DLE20
FOR6 Register	OF272	OF271	OF270	DLE27	OF262	OF261	OF260	DLE26	OF252	OF251	OF250	DLE25	OF242	OF241	OF240	DLE24
FOR7 Register	OF312	OF311	OF310	DLE31	OF302	OF301	OF300	DLE30	OF292	OF291	OF290	DLE29	OF280	OF281	OF280	DLE28

Name[1]	Description
OFn2, OFn1, OFn0 (Offset Bits 2, 1 & 0)	These three bits define how long the serial interface receiver takes to recognize and store bit 0 from the RX input pin: i.e., to start a new frame. The input frame offset can be selected to +7.5 clock periods from the point where the external frame pulse input signal is applied to the FP input of the device. See Figure 2.
DLEn	ST-BUS® and GCI mode: DLEn = 0, offset is on the clock boundary DLEn = 1, offset is a half clock cycle off of the clock boundary.

NOTE:
1. n denotes an input stream number from 0 to 31.

TABLE 9 — OFFSET BITS (OFn2, OFn1, OFn0, DLEn) & FRAME DELAY BITS (FD11, FD2-0)

Input Stream Offset	Measurement Result from Frame Delay Bits				Corresponding Offset Bits			
	FD11	FD2	FD1	FD0	OFn2	OFn1	OFn0	DLEn
No clock period shift (Default)	1	0	0	0	0	0	0	0
+ 0.5 clock period shift	0	0	0	0	0	0	0	1
+ 1.0 clock period shift	1	0	0	1	0	0	1	0
+ 1.5 clock period shift	0	0	0	1	0	0	1	1
+ 2.0 clock period shift	1	0	1	0	0	1	0	0
+ 2.5 clock period shift	0	0	1	0	0	1	0	1
+ 3.0 clock period shift	1	0	1	1	0	1	1	0
+ 3.5 clock period shift	0	0	1	1	0	1	1	1
+ 4.0 clock period shift	1	1	0	0	1	0	0	0
+ 4.5 clock period shift	0	1	0	0	1	0	0	1
+5.0 clock period shift	1	1	0	1	1	0	1	0
+5.5 clock period shift	0	1	0	1	1	0	1	1
+6.0 clock period shift	1	1	1	0	1	1	0	0
+6.5 clock period shift	0	1	1	0	1	1	0	1
+7.0 clock period shift	1	1	1	1	1	1	1	0
+7.5 clock period shift	0	1	1	1	1	1	1	1

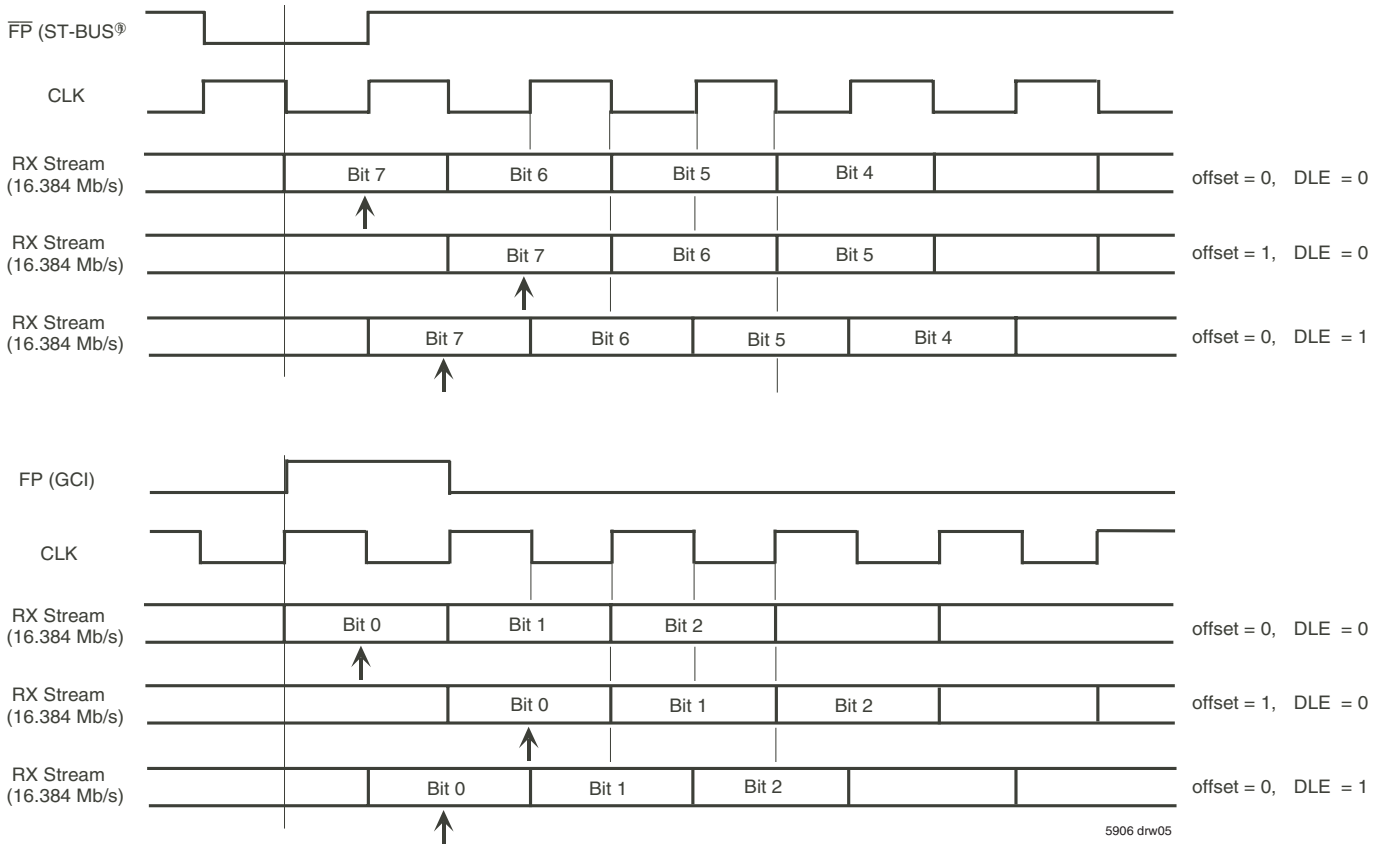


Figure 2. Examples for Input Offset Delay Timing in 16.384Mb/s mode

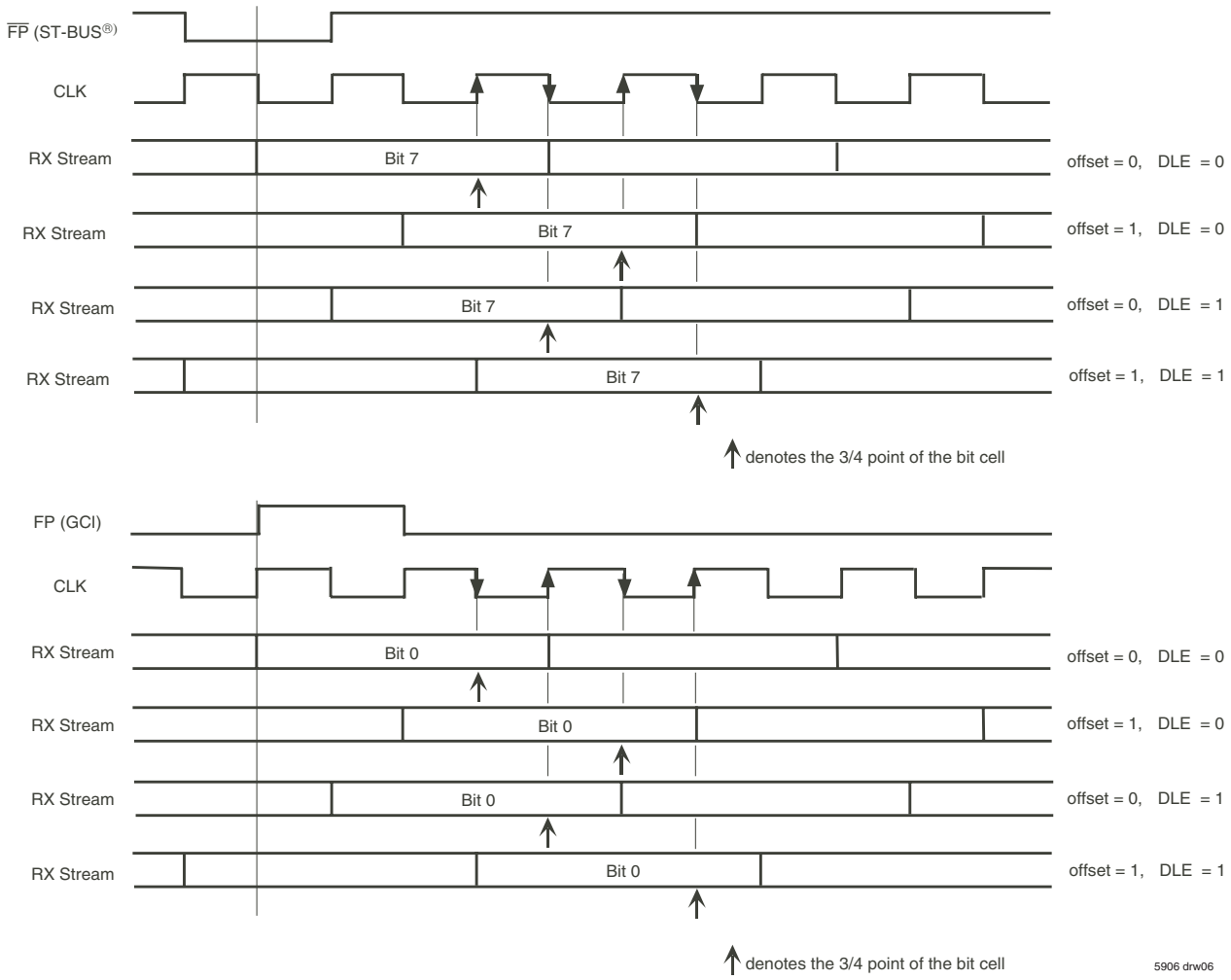


Figure 2. Examples for Input Offset Delay Timing in 8.192Mb/s, 4.096Mb/s and 2.048Mb/s mode (Continued)

JTAG SUPPORT

The IDT72V71650 JTAG interface conforms to the Boundary-Scan standard IEEE-1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the boundary-scan circuitry is controlled by an external test access port (TAP) Controller.

TEST ACCESS PORT (TAP)

The Test Access Port (TAP) provides access to the test functions of the IDT72V71650. It consists of three input pins and one output pin.

•Test Clock Input (TCK)

TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.

•Test Mode Select Input (TMS)

The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to VCC when it is not driven from an external source.

•Test Data Input (TDI)

Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to VCC when it is not driven from an external source.

•Test Data Output (TDO)

Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out through the TDO pin on the falling edge of each TCK pulse. When no data is shifted through the boundary scan cells, the TDO driver is set to a high-impedance state.

•Test Reset (TRST)

Reset the JTAG scan structure. This pin is internally pulled to VCC when it is not driven from an external source.

INSTRUCTION REGISTER

In accordance with the IEEE-1149.1 standard, the IDT72V71650 uses public instructions. The IDT72V71650 JTAG interface contains a four-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shift-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning. See Table 12 below for Instruction decoding.

TEST DATA REGISTER

As specified in IEEE-1149.1, the IDT72V71650 JTAG Interface contains two test data registers:

•The Boundary-Scan register

The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the IDT72V71650 core logic.

•The Bypass Register

The Bypass register is a single stage shift register that provides a one-bit path from TDI to TDO. The IDT72V71650 boundary scan register bits are shown in Table 14. Bit 0 is the first bit clocked out. All three-state enable bits are active HIGH.

ID CODE REGISTER

As specified in IEEE-1149.1, this instruction loads the IDR with the Revision Number, Device ID, and ID Register Indicator Bit. See Table 10.

TABLE 10—IDENTIFICATION REGISTER DEFINITIONS

INSTRUCTION FIELD	VALUE	DESCRIPTION
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x435	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

TABLE 11 — SCAN REGISTER SIZES

REGISTER NAME	BIT SIZE
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note(1)

NOTES:

1. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

TABLE 12— SYSTEM INTERFACE PARAMETERS

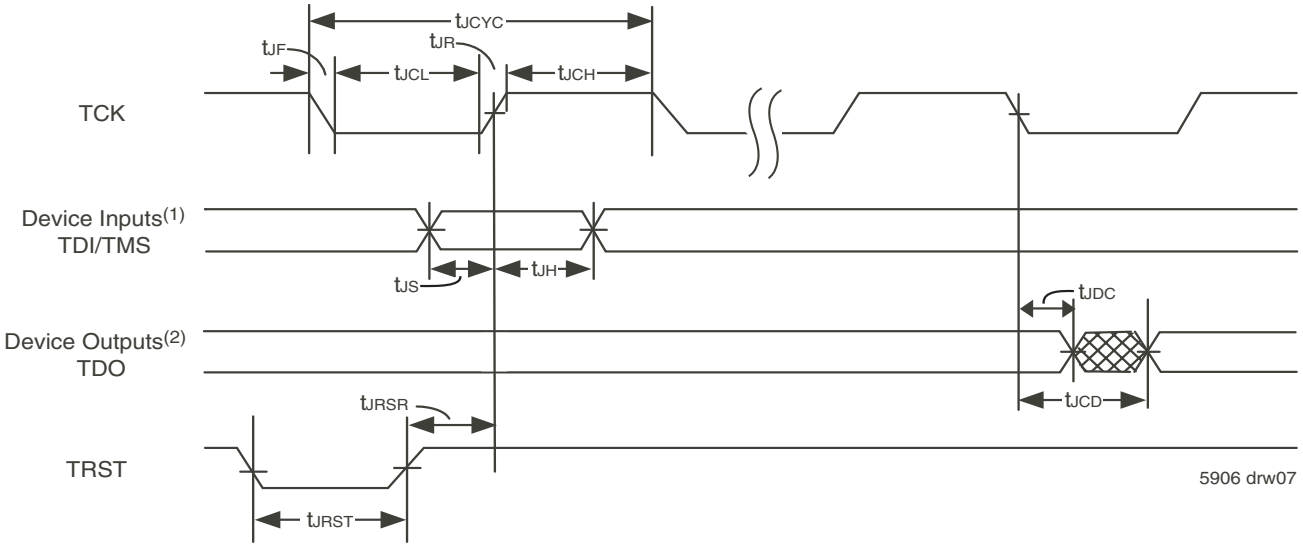
INSTRUCTION	CODE	DESCRIPTION
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs[1]. Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGH-Z	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
CLAMP	0011	Places the bypass register (BYR) between TDI and TDO. Forces contents of the boundary scan cells onto the device outputs.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs[2] and outputs[1] to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use other codes than those identified above.

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS and $\overline{TRST}$.

TABLE 13 — JTAG AC ELECTRICAL CHARACTERISTICS (1,2,3,4)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock High	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	3[1]	ns
t_{JF}	JTAG Clock Fall Time	—	3[1]	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	25	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	15	—	ns
t_{JH}	JTAG Hold	15	—	ns

NOTES:
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.



NOTES:
1. Device inputs = All device inputs except TDI, TMS and $\overline{TRST}$.
2. Device outputs = All device outputs except TDO.

Figure 3. JTAG Timing Specifications

TABLE 14 — BOUNDARY SCAN REGISTER BITS

Device Pin	Boundary Scan Bit 0 to bit 168		
	Input Scan Cell	Output Scan Cell	Three-State Control
ODE	0		
$\overline{\text{RESET}}$	1		
CLK	2		
FP	3		
FE(HCLK)	4		
WFPS	5		
$\overline{\text{DS}}$	6		
$\overline{\text{CS}}$	7		
R/$\overline{\text{W}}$	8		
A0	9		
A1	10		
A2	11		
A3	12		
A4	13		
A5	14		
A6	15		
A7	16		
A8	17		
A9	18		
A10	19		
A11	20		
A12	21		
A13	22		
A14	23		
$\overline{\text{DTA}}$		24	
D15	25	26	27
D14	28	29	30
D13	31	32	33
D12	34	35	36
D11	37	38	39
D10	40	41	42
D9	43	44	45
D8	46	47	48
D7	49	50	51
D6	52	53	54
D5	55	56	57
D4	58	59	60
D3	61	62	63
D2	64	65	66
D1	67	68	69
D0	70	71	72
RX31	73		
RX30	74		
RX29	75		
RX28	76		
RX27	77		
RX26	78		
RX25	79		
RX24	80		
TX31/OEI15		81	82
TX30/OEI14		83	84
TX29/OEI13		85	86

Device Pin	Boundary Scan Bit 0 to bit 168		
	Input Scan Cell	Output Scan Cell	Three-State Control
TX28/OEI12		87	88
TX27/OEI11		89	90
TX26/OEI10		91	92
TX25/OEI9		93	94
TX24/OEI8		95	96
TX23/OEI7		97	98
TX22/OEI6		99	100
TX21/OEI5		101	102
TX20/OEI4		103	104
TX19/OEI3		105	106
TX18/OEI2		107	108
TX17/OEI1		109	110
TX16/OEI0		111	112
RX23	113		
RX22	114		
RX21	115		
RX20	116		
RX19	117		
RX18	118		
RX17	119		
RX16	120		
RX15	121		
RX14	122		
RX13	123		
RX12	124		
RX11	125		
RX10	126		
RX9	127		
RX8	128		
TX15		129	130
TX14		131	132
TX13		133	134
TX12		135	136
TX11		137	138
TX10		139	140
TX9		141	142
TX8		143	144
TX7		145	146
TX6		147	148
TX5		149	150
TX4		151	152
TX3		153	154
TX2		155	156
TX1		157	158
TX0		159	160
RX7	161		
RX6	162		
RX5	163		
RX4	164		
RX3	165		
RX2	166		
RX1	167		
RX0	168		

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	+4.0	V
Vi	Voltage on Digital Inputs	GND -0.3	V_{CC} +0.3	V
Io	Current at Digital Outputs	-50	50	mA
Ts	Storage Temperature	-55	+125	° C
P_D	Package Power Dissapation	—	2	W

NOTE:
1. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Positive Supply	3.0	3.3	3.6	V
V_{IH}	Input HIGH Voltage	2.0	—	V_{CC}	V
V_{IL}	Input LOW Voltage	-0.3	—	0.8	V
T_{OP}	Operating Temperature Industrial	-40	25	+85	°C

NOTE:
1. Voltages are with respect to Ground unless otherwise stated.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Units
I_{CC} (2)	Supply Current	@ 2.048Mb/s	-	-	60	mA
		@ 4.096Mb/s	-	-	80	mA
		@ 8.192Mb/s	-	-	90	mA
		@ 16.384Mb/s	-	-	95	mA
I_{IL}(3,4)	Input Leakage (input pins)		-	-	60	µA
I_{OZ}(3,4)	High-impedance Leakage		-	-	60	µA
V_{OH}(5)	Output HIGH Voltage		2.4	-	-	V
V_{OL}(6)	Output LOW Voltage		-	-	0.4	V

NOTES:
1. Voltages are with respect to ground (GND) unless otherwise stated.
2. Outputs unloaded.
3. $0 \leq V \leq V_{CC}$.
4. Maximum leakage on pins (output or I/O pins in high-impedance state) is over an applied voltage (V).
5. IOH = 10 mA.
6. IOL = 10 mA.

AC ELECTRICAL CHARACTERISTICS - TIMING PARAMETER MEASUREMENT VOLTAGE LEVELS

Symbol	Rating	Level	Unit
V_{TT}	TTL Threshold	1.5	V
V_{HM}	TTL Rise/Fall Threshold Voltage HIGH	2.0	V
V_{LM}	TTL Rise/Fall Threshold Voltage LOW	0.8	V
	Input Pulse Levels		V
t_R, t_F	Input Rise/Fall Times	1	ns
	Input Timing Reference Levels		V
	Output Reference Levels		V
C_L[1]	Output Load	150	pF
Cin[2]	Input Capacitance	8	pF

NOTES:
1. JTAG C_L is 30 pF.
2. For 144 TQFP

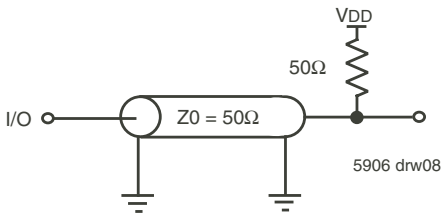


Figure 4. Output Load

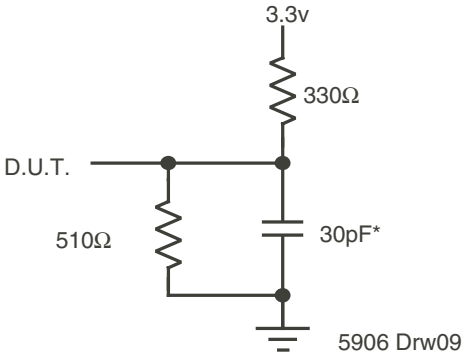


Figure 5. Output Load

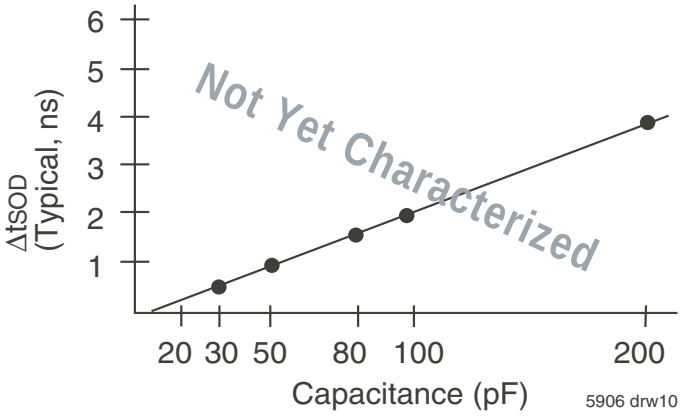
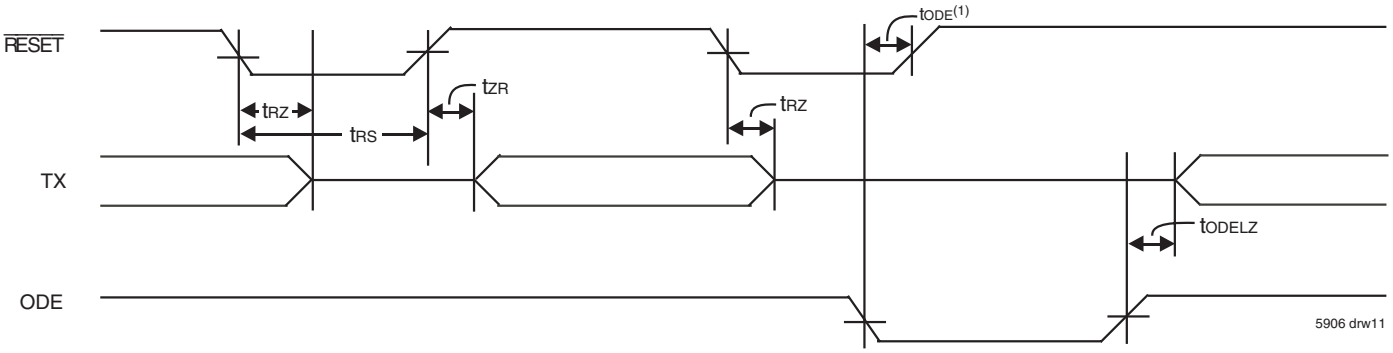


Figure 6. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS - FRAME PULSE AND CLOCK

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{FPW}	Frame Pulse Width (ST-BUS®, GCI)				
	Bit rate = 2.048Mb/s	26	—	295	ns
	Bit rate = 4.096Mb/s	26	—	145	ns
	Bit rate = 8.192Mb/s or 16.384Mb/s	26	—	65	ns
t_{FPS}	Frame Pulse Setup time before CLK falling (ST-BUS® or GCI)	5	—	—	ns
t_{FPH}	Frame Pulse Hold Time from CLK falling (ST-BUS® or GCI)	10	—	—	ns
t_{CP}	CLK Period				
	Bit rate = 2.048Mb/s	190	244	300	ns
	Bit rate = 4.096Mb/s	110	122	150	ns
	Bit rate = 8.192Mb/s or 16.384Mb/s	55	61	70	ns
t_{CH}	CLK Pulse Width HIGH				
	Bit rate = 2.048Mb/s	85	122	150	ns
	Bit rate = 4.096Mb/s	50	61	75	ns
	Bit rate = 8.192Mb/s or 16.384Mb/s	20	30	40	ns
t_{CL}	CLK Pulse Width LOW				
	Bit rate = 2.048Mb/s	85	122	150	ns
	Bit rate = 4.096Mb/s	50	61	75	ns
	Bit rate = 8.192Mb/s or 16.384Mb/s	20	30	40	ns
t_{HFPW}	Wide Frame Pulse Width				
	HCLK = 4.096Mb/s		244		ns
t_{HFPS}	Frame Pulse Setup Time before HCLK @ 4.096 MHz falling	50	—	150	ns
t_{HFPH}	Frame Pulse Hold Time from HCLK @ 4.096 MHz falling	50	—	150	ns
t_{HCP}	HCLK Period				
	@ 4.096 MHz	190	244	300	ns
t_{HCH}	HCLK Pulse Width HIGH				
	@ 4.096Mb/s	110	122	150	ns
t_{HCL}	HCLK Pulse Width LOW				
	@ 4.096Mb/s	110	122	150	ns
t_{Hr}, t_{Hf}	HCLK Rise/Fall Time	—	—	10	ns
t_{DIF}	Delay between falling edge of HCLK and falling edge of CLK	-10	—	10	ns



NOTE:
1. To guarantee TX outputs remain in high-impedance.

Figure 7. RESET and ODE Timing

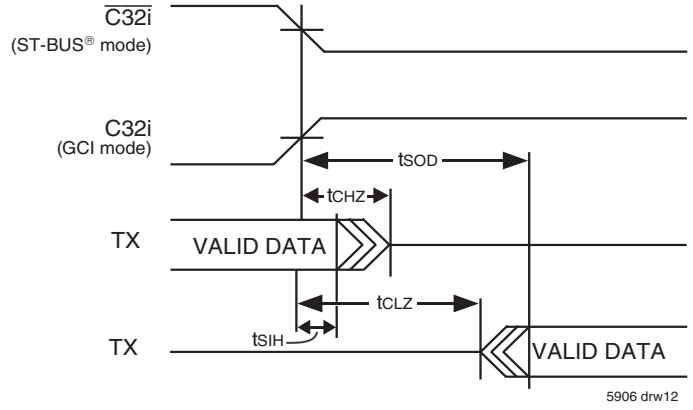


Figure 8. Serial Output and External Control

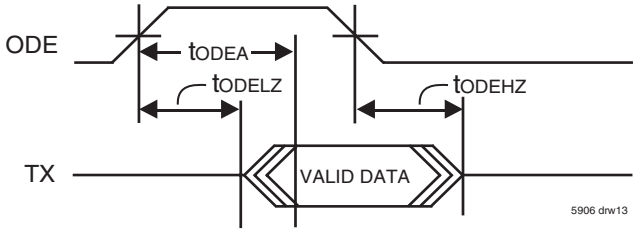
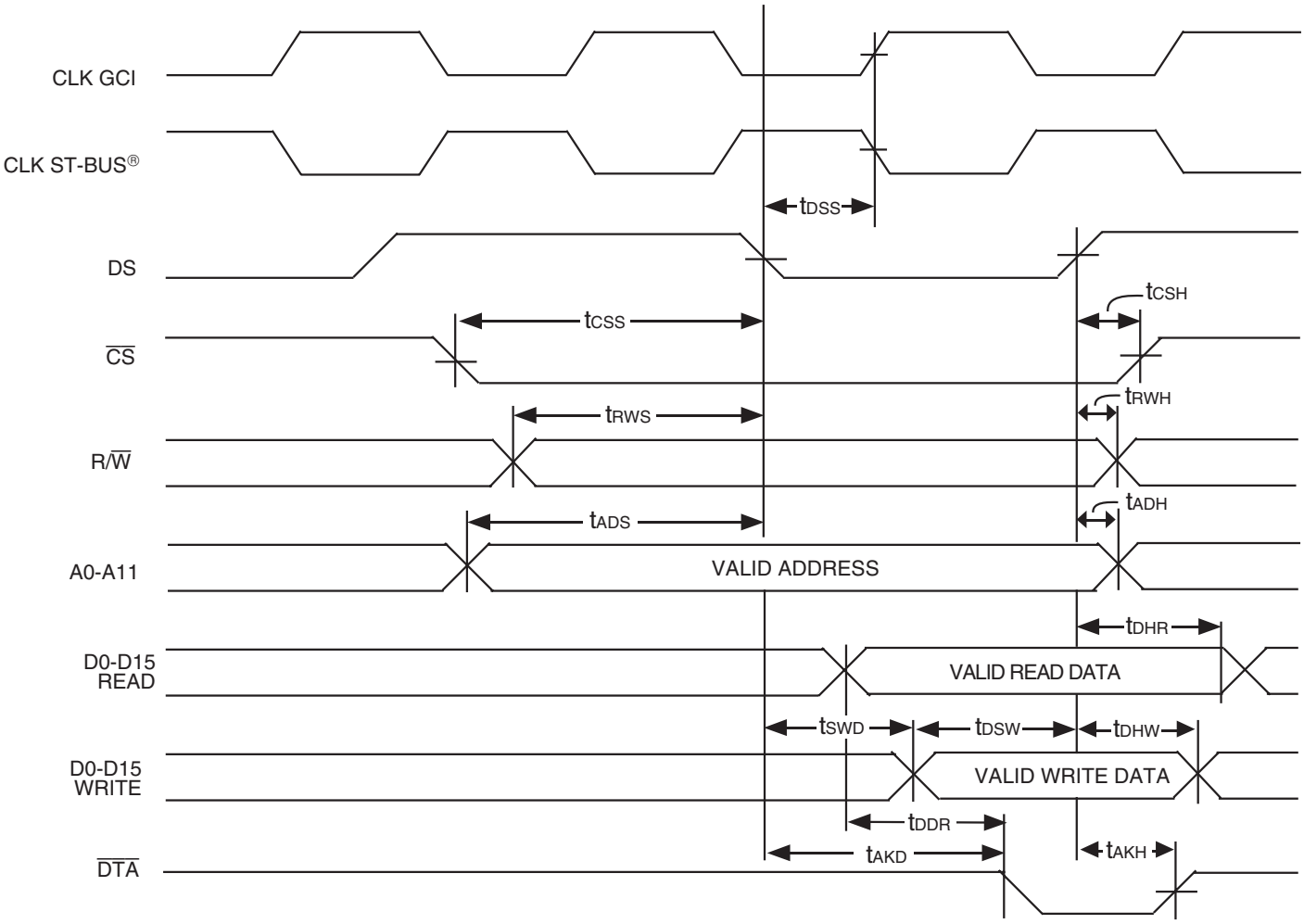


Figure 9. Output Driver Enable (ODE)

AC ELECTRICAL CHARACTERISTICS - MICROPROCESSOR INTERFACE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CSS}	CS Setup from DS falling	0	—	—	ns
t_{RWS}	R/W Setup from DS falling	3	—	—	ns
t_{ADS}	Address Setup from DS falling	2	—	—	ns
t_{CSH}	CS Hold after DS rising	0	—	—	ns
t_{RWH}	R/W Hold after DS Rising	3	—	—	ns
t_{ADH}	Address Hold after DS Rising	2	—	—	ns
t_{DDR}	Data Setup from $\overline{DTA}$ LOW on Read	1	—	—	ns
t_{DHR}	Data Hold on Read	10	15	25	ns
t_{DSW}	Data Setup on Write (Register Write)	10	—	—	ns
t_{SWD}	Valid Data Delay on Write (Connection Memory Write)	—	—	0	ns
t_{DHW}	Data Hold on Write	5	—	—	ns
t_{AKD}	Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory @ 2.048Mb/s @ 4.096Mb/s @ 8.192Mb/s or 16.384Mb/s			 32 345 200 120	 ns ns ns ns
t_{AKH}	Acknowledgment Hold Time	—	—	20	ns
t_{DSS}	Data Strobe Setup Time	6	—	—	ns



NOTE:
1. For quick microprocessor access t_{DSS} must be met. In this case $t_{AKD} = t_{AKD}$ (max) - CLK (period) t_{DSS}.

Figure 10. Motorola Non-Multiplexed Bus Timing

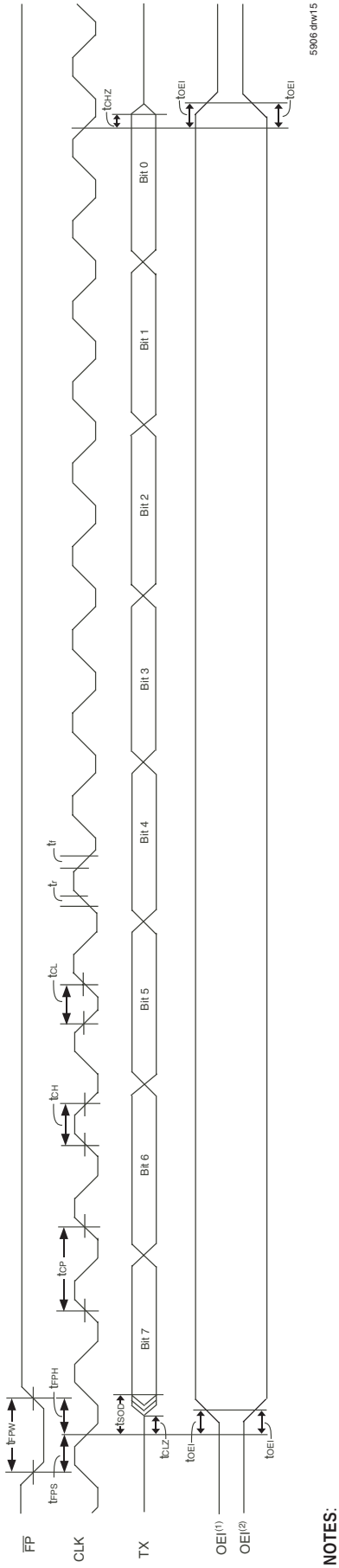


Figure 11. Output Enable Indicator Timing (8 Mb/s ST-BUS®)

NOTES:
1. When Output Enable Polarity = 1, Output Enable Indication is HIGH when TX is active and LOW when TX is in three-state.
2. When Output Enable Polarity = 0, Output Enable Indication is LOW when TX is active and HIGH when TX is in three-state.

AC ELECTRICAL CHARACTERISTICS — SERIAL STREAM (ST-BUS® and GCI)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{SIS}	RX Setup Time	4	—	—	ns
t_{SIH}	RX Hold Time	8	—	—	ns
t_{SOD}	Clock to Valid Data	8	—	20	ns
t_{CHZ}	Clock to High-Z	—	—	9	ns
t_{CLZ}	Clock to Low-Z	3	—	—	ns
t_{ODE}	Output Driver Enable to Reset High	5	—	—	ns
t_{ODEHZ}	Output Driver Enable (ODE) Delay	—	—	9	ns
t_{ODELZ}	Output Driver Enable (ODE) to Low-Z	5	—	—	ns
t_{OEI}	Output Enable Indicator	8	—	20	ns
t_{RZ}	Active to High-Z on Master Reset	—	—	12	ns
t_{ZR}	High-Z to Active on Master Reset	—	—	12	ns
t_{RS}	Reset pulse width	20	—	—	ns
t_{ODEA}	Output Drive Enable to Active	6	—	16	ns

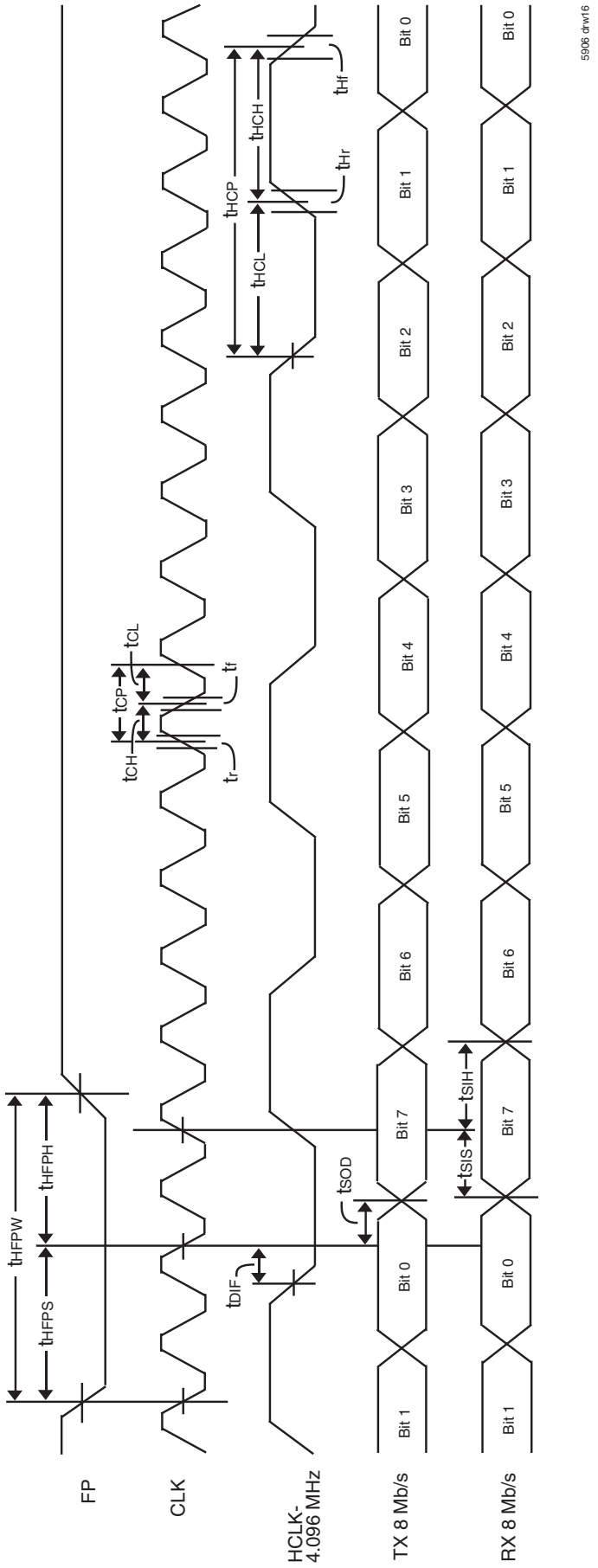


Figure 12. WFPS Timing

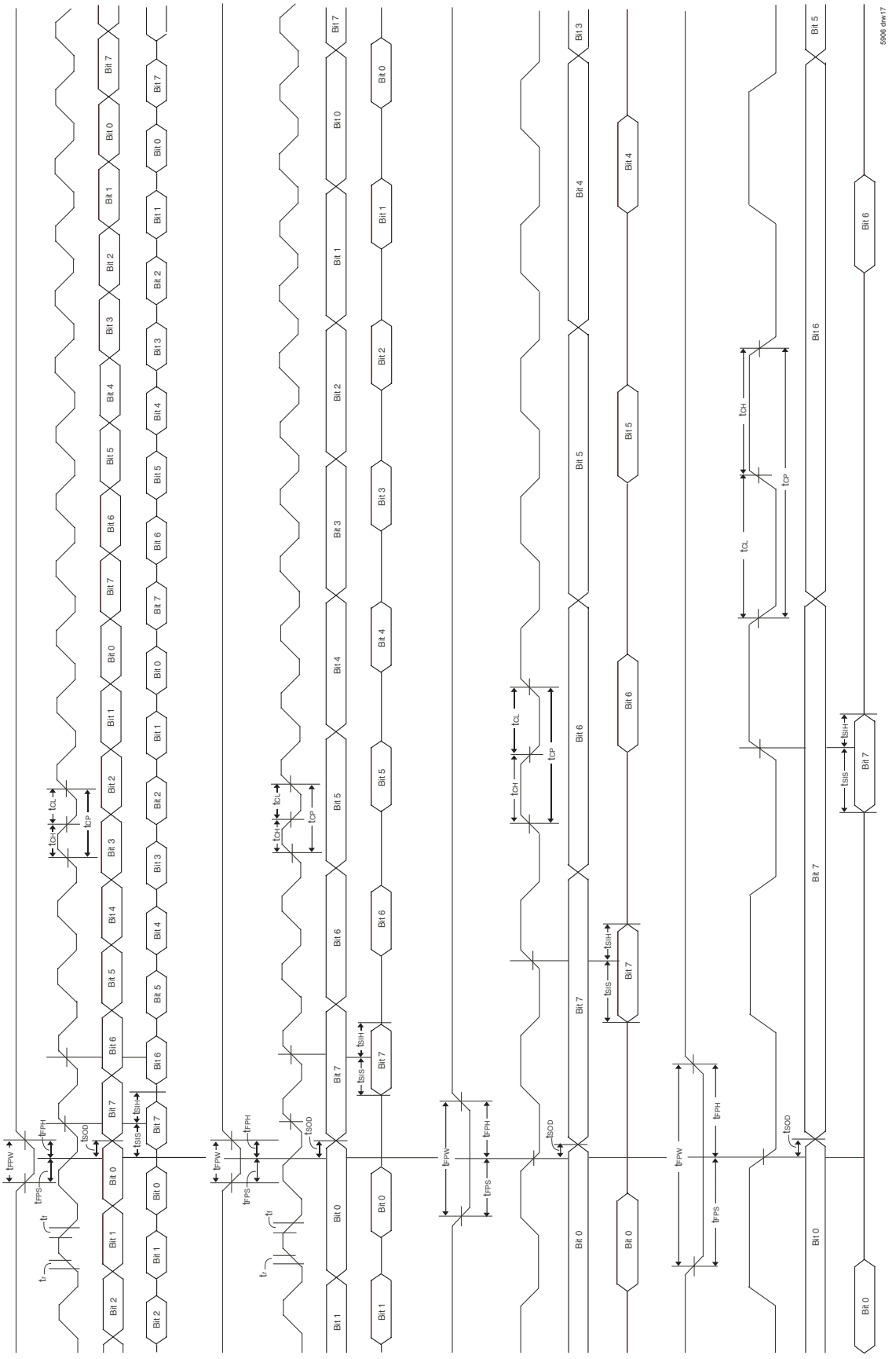
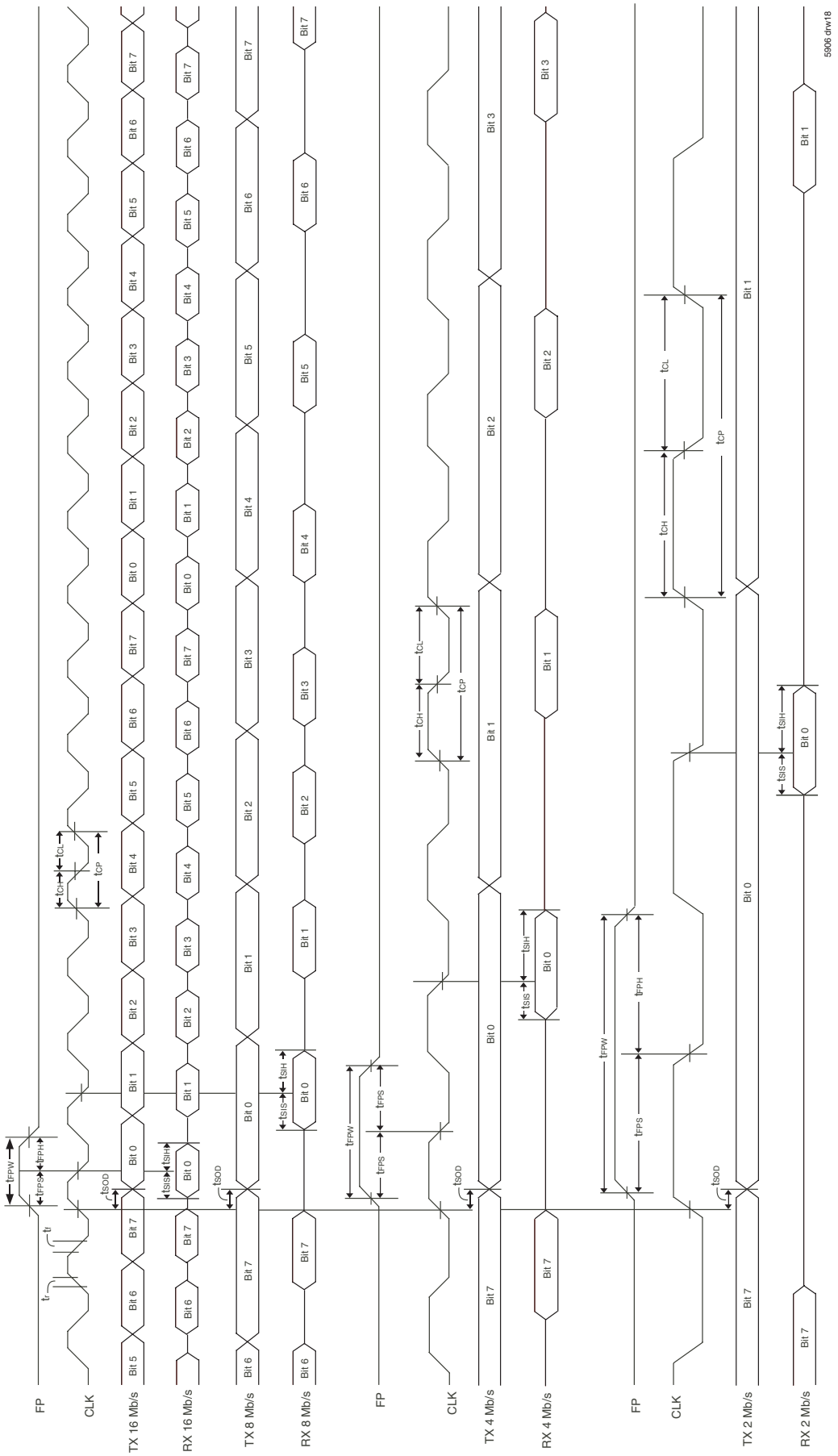


Figure 13. Serial Interface Timing (ST-BUS® Style)

NOTE:

1. @ 2.048Mb/s mode, last channel = ch 31,
   @ 4.096Mb/s mode, last channel = ch 63,
   @ 8.192Mb/s mode, last channel = ch 127.
   @ 16.384Mb/s mode, last channel = ch 255.

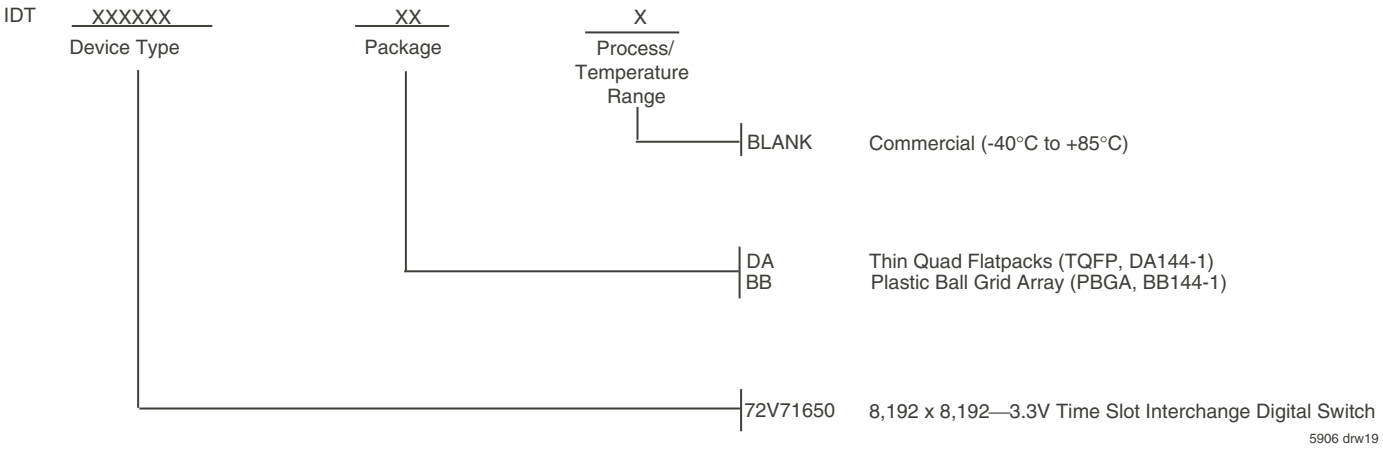


NOTE:

1. @ 2.048Mb/s mode, last channel = ch 31,
   @ 4.096Mb/s mode, last channel = ch 63,
   @ 8.192Mb/s mode, last channel = ch 127,
   @ 16.384Mb/s mode, last channel = ch 255.

Figure 14 Serial Interface Timing (GCI Style)

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

08/14/2001	pgs. 3, 18, 19, 21, 22, 24 and 25.
09/24/2001	pgs. 2, 3, 11, 19, 21, 24 and 25.
12/19/2001	pgs. 1-6, 8, 10-19, 20-21 and 23-27.
12/21/2001	pgs. 1, 5, 6, 14-19 and 24.
03/26/2002	pgs. 17 and 18.
08/02/2002	pg. 8
05/24/2003	pg. 18.

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