6812

DABiC-IV, 20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

A6812xA

Dwg. PP-029-7

The A6812– devices combine a 20-bit CMOS shift register, accompanying data latches and control circuitry with bipolar sourcing outputs and pnp active pull downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The A6812– features an increased data input rate (compared with the older UCN/UCQ5812-F) and a controlled output slew rate.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 3.3 V or 5 V logic supply, typical serial-data input rates are up to 33 MHz.

A CMOS serial data output permits cascade connections in applications requiring additional drive lines. Similar devices are available as the A6809– and A6810– (10 bits), A6811– (12 bits), and A6818– (32 bits).

The A6812– output source drivers are npn Darlingtons, capable of sourcing up to 40 mA. The controlled output slew rate reduces electro-magnetic noise, which is an important consideration in systems that include telecommunications and/or microprocessors and to meet government emissions regulations. For inter-digit blanking, all output drivers can be disabled and all sink drivers turned on with a BLANK-ING input high. The pnp active pull-downs will sink at least 2.5 mA.

Three temperature ranges are available for optimum performance in commercial (suffix S-), industrial (suffix E-), or automotive (suffix K-) applications. Package styles are provided for through-hole DIP (suffix -A), surface-mount SOIC (suffix -LW), or minimum-area surface-mount PLCC (suffix -EP). Copper lead frames, low logic-power dissipation, and low output-saturation voltages allow these drivers to source 25 mA from all outputs continuously to more than +43°C (suffix -LW), +61°C (suffix -EP), or +77°C (suffix -A).

ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

Logic Supply Voltage, V_{DD} .... **7.0 V**

Driver Supply Voltage, V_{BB} .... **60 V**

Continuous Output Current Range,
I_{OUT} .... **-40 mA to +15 mA**

Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**

Package Power Dissipation,
P_D .... **See Graph**

Operating Temperature Range, T_A
(Suffix 'E–') .... **-40°C to +85°C**
(Suffix 'K–') .... **-40°C to +125°C**
(Suffix 'S–') .... **-20°C to +85°C**

Storage Temperature Range,
T_S .... **-55°C to +125°C**

Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.

FEATURES

- Controlled Output Slew Rate
- High-Speed Data Storage
- 60 V Minimum Output Breakdown
- High Data Input Rate
- PNP Active Pull-Downs
- Low Output-Saturation Voltages
- Low-Power CMOS Logic and Latches
- Improved Replacements for TL5812–, UCN5812–, and UCQ5812–

Complete part number includes a suffix to identify operating temperature range (E-, K-, or S-) and package type (-A, -EP, or -LW). Always order by complete part number, e.g., A6812SLW .
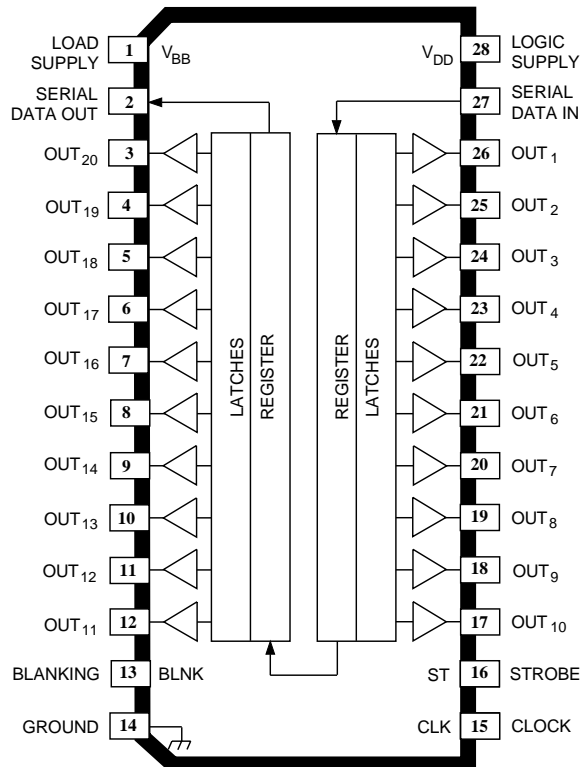
Allegro®
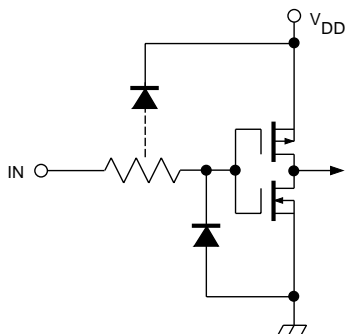MicroSystems, Inc.
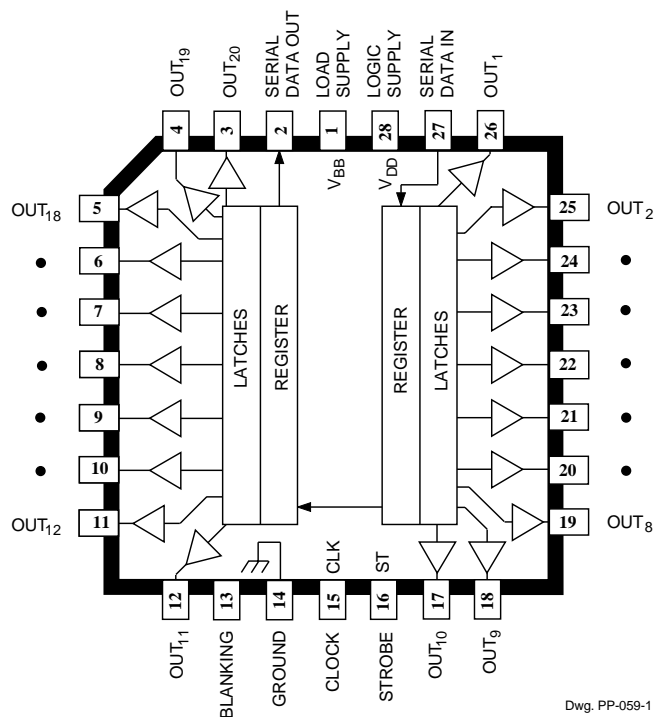
A6812xEP

Dwg. PP-059-1

A6812xLW

Dwg. PP-029-8

TYPICAL INPUT CIRCUIT

Dwg. EP-010-5

TYPICAL OUTPUT DRIVER

Dwg. EP-021-19

ALLOWABLE PACKAGE POWER DISSIPATION IN WATTS

AMBIENT TEMPERATURE IN °C

SUFFIX 'A', $R_{\theta JA}$ = 45°C/W

SUFFIX 'EP', $R_{\theta JA}$ = 55°C/W

SUFFIX 'LW', $R_{\theta JA}$ = 66°C/W

Dwg. GP-024-2

FUNCTIONAL BLOCK DIAGRAM

Dwg. FP-013-1
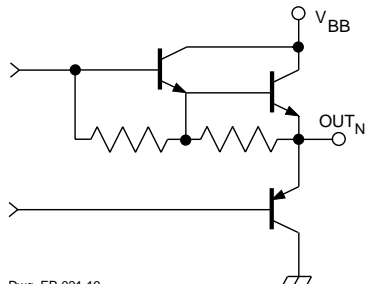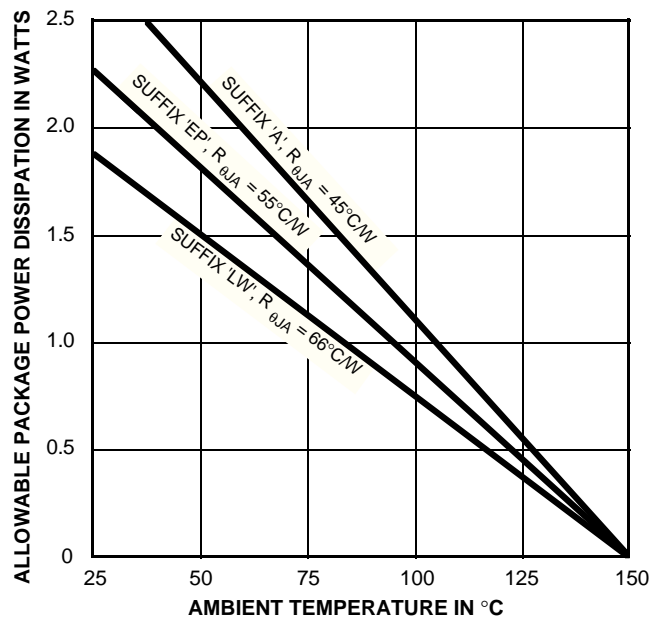
TRUTH TABLE

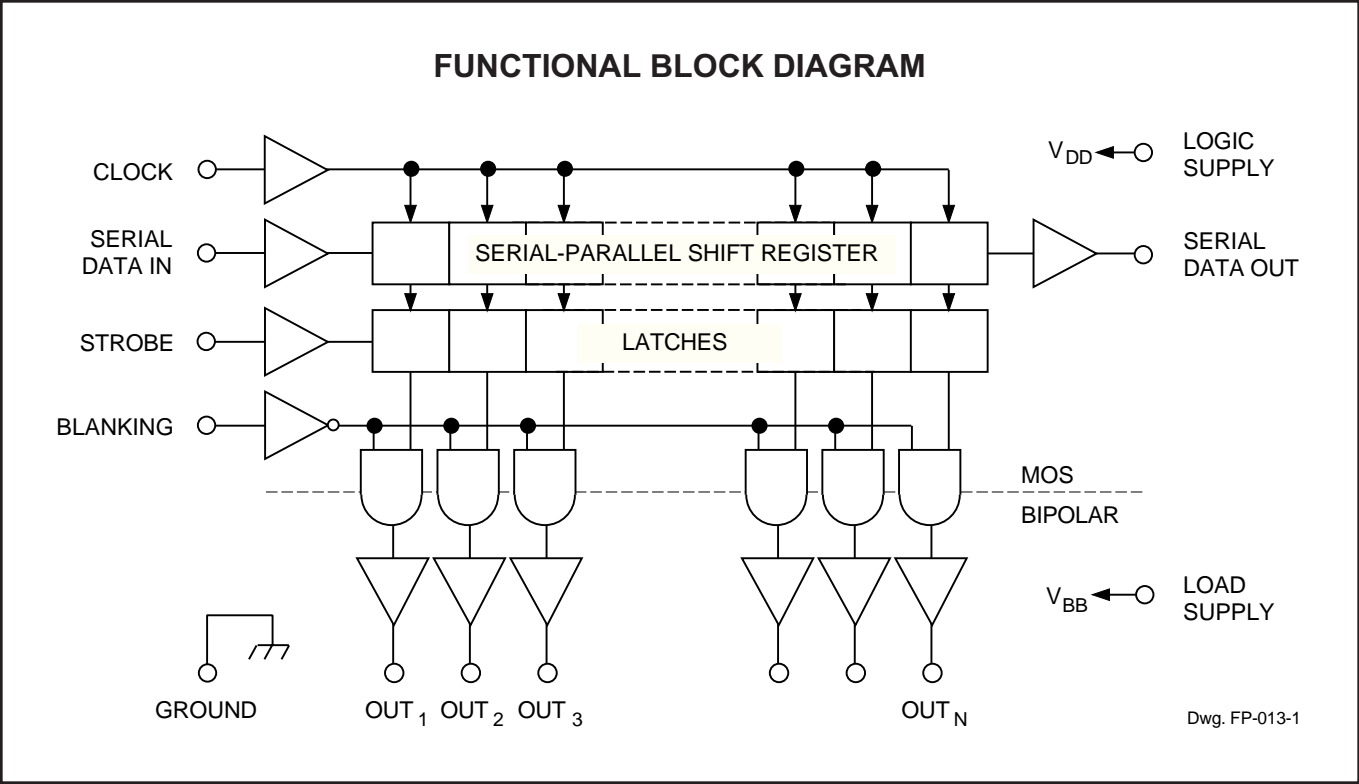| Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Blanking	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	I_N
H	⎍	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	⎍	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	⎍	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State

ELECTRICAL CHARACTERISTICS at T$_A$ = +25°C (A6812S-) or over operating temperature range (A6812E- and A6812K-), V$_{BB}$ = 60 V unless otherwise noted.

| Characteristic	Symbol	Test Conditions	Limits @ V$_{DD}$ = 3.3 V			Limits @ V$_{DD}$ = 5 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I$_{CEX}$	V$_{OUT}$ = 0 V	—	<-0.1	-15	—	<-0.1	-15	µA
Output Voltage	V$_{OUT(1)}$	I$_{OUT}$ = -25 mA	57.5	58.3	—	57.5	58.3	—	V
	V$_{OUT(0)}$	I$_{OUT}$ = 1 mA	—	1.0	1.5	—	1.0	1.5	V
Output Pull-Down Current	I$_{OUT(0)}$	V$_{OUT}$ = 5 V to V$_{BB}$	2.5	5.0	—	2.5	5.0	—	mA
Input Voltage	V$_{IN(1)}$		2.2	—	—	3.3	—	—	V
	V$_{IN(0)}$		—	—	1.1	—	—	1.7	V
Input Current	I$_{IN(1)}$	V$_{IN}$ = V$_{DD}$	—	<0.01	1.0	—	<0.01	1.0	µA
	I$_{IN(0)}$	V$_{IN}$ = 0 V	—	<-0.01	-1.0	—	<-0.01	-1.0	µA
Input Clamp Voltage	V$_{IK}$	I$_{IN}$ = -200 µA	—	-0.8	-1.5	—	-0.8	-1.5	V
Serial Data Output Voltage	V$_{OUT(1)}$	I$_{OUT}$ = -200 µA	2.8	3.05	—	4.5	4.75	—	V
	V$_{OUT(0)}$	I$_{OUT}$ = 200 µA	—	0.15	0.3	—	0.15	0.3	V
Maximum Clock Frequency	f$_c$		10	33	—	10	33	—	MHz
Logic Supply Current	I$_{DD(1)}$	All Outputs High	—	0.25	0.75	—	0.3	1.0	mA
	I$_{DD(0)}$	All Outputs Low	—	0.25	0.75	—	0.3	1.0	mA
Load Supply Current	I$_{BB(1)}$	All Outputs High, No Load	—	3.0	6.0	—	3.0	6.0	mA
	I$_{BB(0)}$	All Outputs Low	—	0.2	20	—	0.2	20	µA
Blanking-to-Output Delay	t$_{dis(BQ)}$	C$_L$ = 30 pF, 50% to 50%	—	0.7	2.0	—	0.7	2.0	µs
	t$_{en(BQ)}$	C$_L$ = 30 pF, 50% to 50%	—	1.8	3.0	—	1.8	3.0	µs
Strobe-to-Output Delay	t$_{p(STH-QL)}$	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	—	0.7	2.0	—	0.7	2.0	µs
	t$_{p(STH-QH)}$	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	—	1.8	3.0	—	1.8	3.0	µs
Output Fall Time	t$_f$	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	2.4	—	12	2.4	—	12	µs
Output Rise Time	t$_r$	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	2.4	—	12	2.4	—	12	µs
Output Slew Rate	dV/dt	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	4.0	—	20	4.0	—	20	V/µs
Clock-to-Serial Data Out Delay	t$_{p(CH-SQX)}$	I$_{OUT}$ = ±200 µA	—	50	—	—	50	—	ns

Negative current is defined as coming out of (sourcing) the specified device terminal.

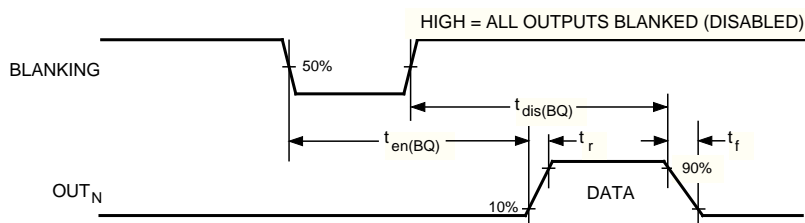Typical data is is for design information only and is at T$_A$ = +25°C.

TIMING REQUIREMENTS and SPECIFICATIONS
(Logic Levels are V_{DD} and Ground)
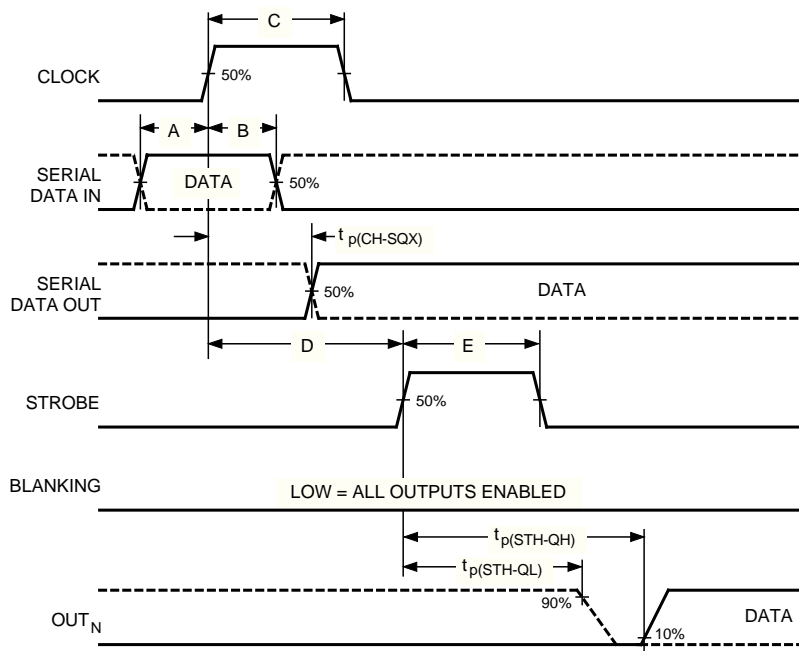
Dwg. WP-029

Dwg. WP-030

A. Data Active Time Before Clock Pulse
(Data Set-Up Time), $t_{su(D)}$ .... **25 ns**
B. Data Active Time After Clock Pulse
(Data Hold Time), $t_{h(D)}$ .... **25 ns**
C. Clock Pulse Width, $t_{w(CH)}$ .... **50 ns**
D. Time Between Clock Activation and Strobe, $t_{su(C)}$ .... **100 ns**
E. Strobe Pulse Width, $t_{w(STH)}$ .... **50 ns**

NOTE – Timing is representative of a 10 MHz clock. Significantly higher speeds are attainable.

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.
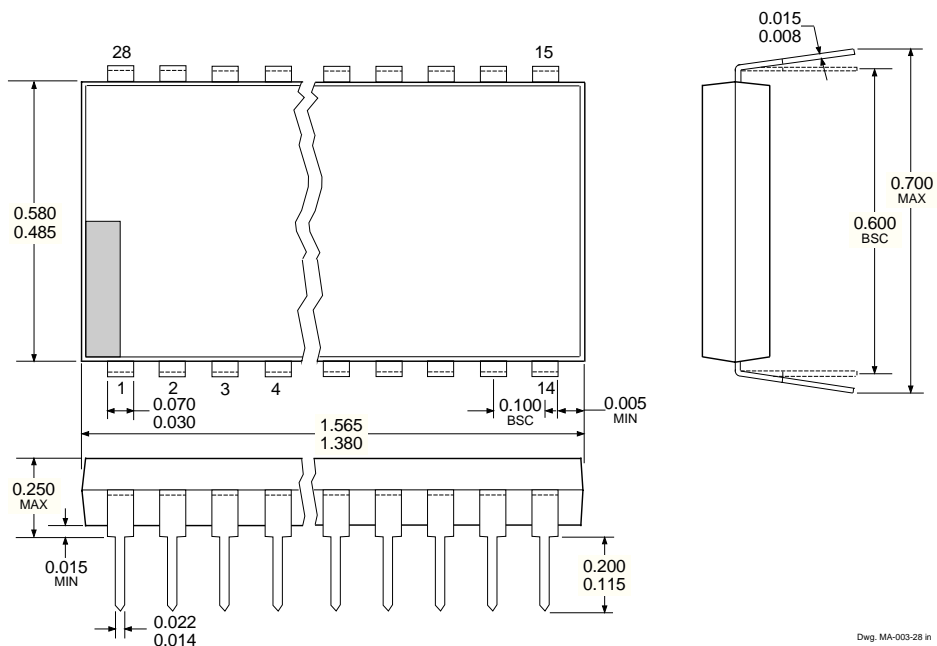
When the BLANKING input is high, the output source drivers are disabled (OFF); the pnp active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.
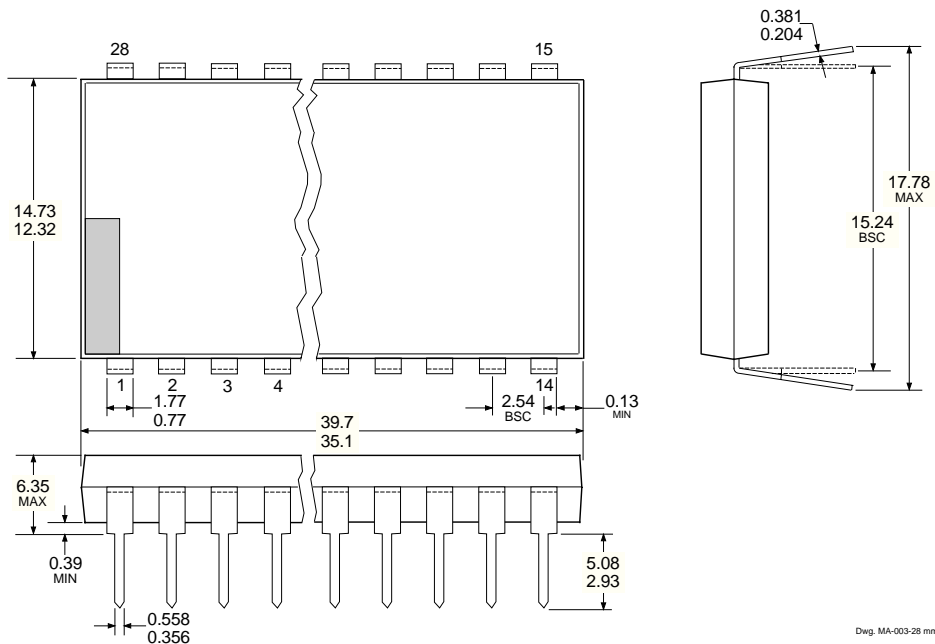
A6812EA, A6812KA, & A6812SA

Dimensions in Inches
(controlling dimensions)

28   15

0.580
0.485

1   2   3   4   14
0.070   0.100   0.005
0.030   BSC   MIN

1.565
1.380

0.250
MAX

0.015
MIN

0.200
0.115

0.022
0.014

0.015
0.008

0.700
MAX

0.600
BSC

Dwg. MA-003-28 in

Dimensions in Millimeters
(for reference only)

28   15

14.73
12.32

1   2   3   4   14
1.77   2.54   0.13
0.77   BSC   MIN

39.7
35.1

6.35
MAX

0.39
MIN

5.08
2.93

0.558
0.356

0.381
0.204

17.78
MAX

15.24
BSC

Dwg. MA-003-28 mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
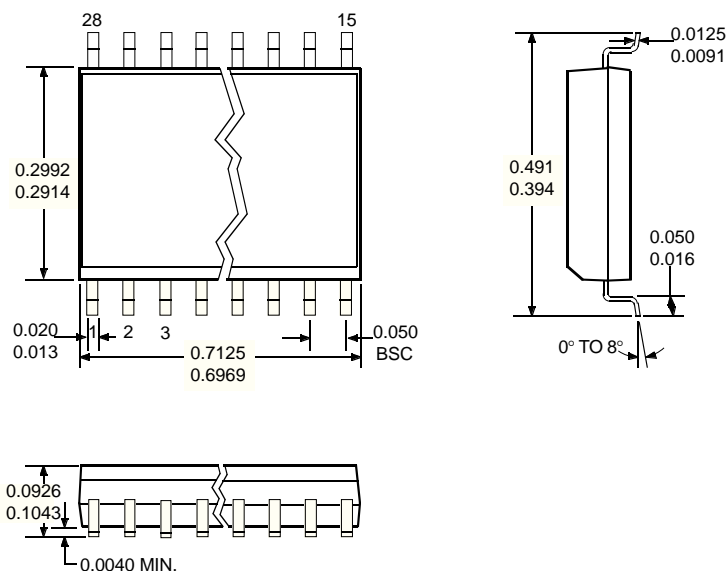3. Lead thickness is measured at seating plane or below.

A6812EEP, A6812KEP, & A6812SEP

Dimensions in Inches
(controlling dimensions)

0.013
0.021

0.219
0.191

0.050
BSC

0.219
0.191

0.456
0.450

0.495
0.485

0.026
0.032

INDEX AREA

18   12

19   11

25   5

26   28   1   4

0.020
MIN

0.165
0.180

0.456
0.450

0.495
0.485

Dwg. MA-005-28A in

Dimensions in Millimeters
(for reference only))

0.331
0.533

5.56
4.85

1.27
BSC

5.56
4.85

11.58
11.43

12.57
12.32

0.812
0.661

INDEX AREA

18   12

19   11

25   5

26   28   1   4

0.51
MIN

4.57
4.20

11.582
11.430

12.57
12.32

Dwg. MA-005-28A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
          2. Lead spacing tolerance is non-cumulative.

A6812ELW, A6812KLW, & A6812SLW

Dimensions in Inches
(for reference only)

28   15

0.2992
0.2914

0.020
0.013

1 2 3

0.7125
0.6969

0.050
BSC

0.0125
0.0091

0.491
0.394

0.050
0.016

0° TO 8°

0.0926
0.1043

0.0040 MIN.

Dwg. MA-008-28 in

Dimensions in Millimeters
(controlling dimensions)
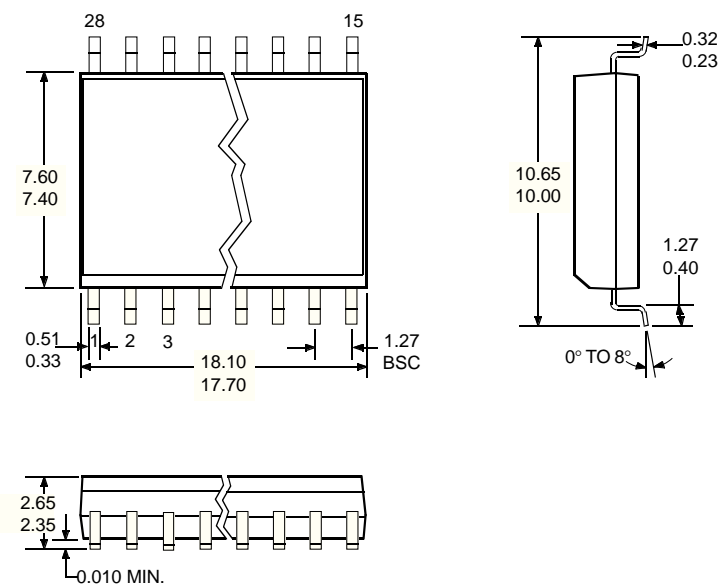
28   15

7.60
7.40

0.51
0.33

1 2 3

18.10
17.70

1.27
BSC

0.32
0.23

10.65
10.00

1.27
0.40

0° TO 8°

2.65
2.35

0.010 MIN.

Dwg. MA-008-28 mm

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NOTES: 1. Exact body and lead configuration at vendor's option within
            limits shown.
        2. Lead spacing tolerance is non-cumulative.