

HN62454N Series

262144-word $\times$ 16-bit / 524288-word $\times$ 8-bit CMOS Mask
Programmable ROM

HITACHI

ADE-203-404A (Z)

Rev. 1.0

May. 21, 1996

Description

The HN62454N is a 4-Mbit CMOS mask-Programmable ROM organized either as 262144 words by 16 bits or 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 100 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

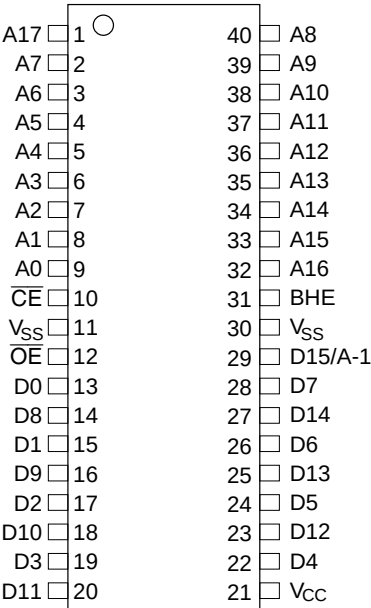
- Single 5 V supply
- High speed
 - Normal access time: 100 ns (max)
 - Page access time: 40 ns (max)
- Low power
 - Active: 550 mW (max)
 - Standby: 165 μ W (max)
- Byte-wide or word-wide data organization (Switched by BHE terminal)
- 4 word page access on word-wide mode
- 8 byte page access on byte-wide mode
- Three-state data output for or-tying
- Directly TTL compatible
 - All inputs and outputs
- Pin compatible with 4 Mbit EPROM (HN27C4000G/FP)

Ordering Information

Type No.	Access time	Package
HN62454NP-10	100 ns	600 mil 40-pin plastic DIP (DP-40)
HN62454NFA-10	100 ns	525 mil 40-pin plastic SOP (FP-40D)
HN62454NTT-10	100 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

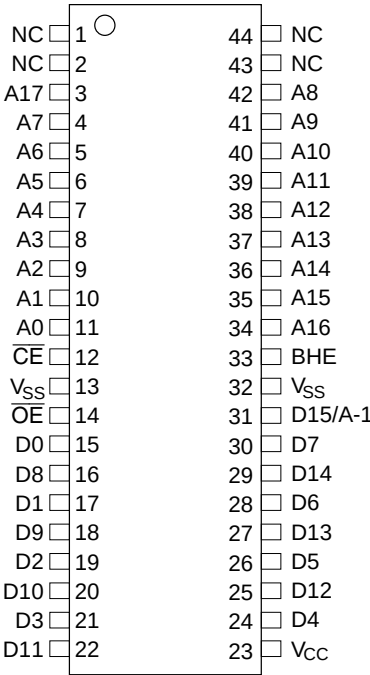
Pin Arrangement

HN62454NP Series



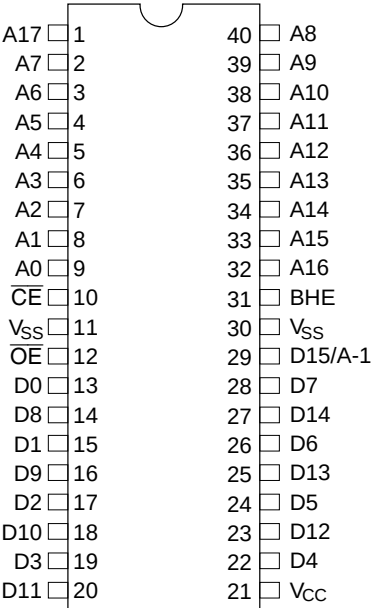
(Top view)

HN62454NTT Series



(Top view)

HN62454NFA Series

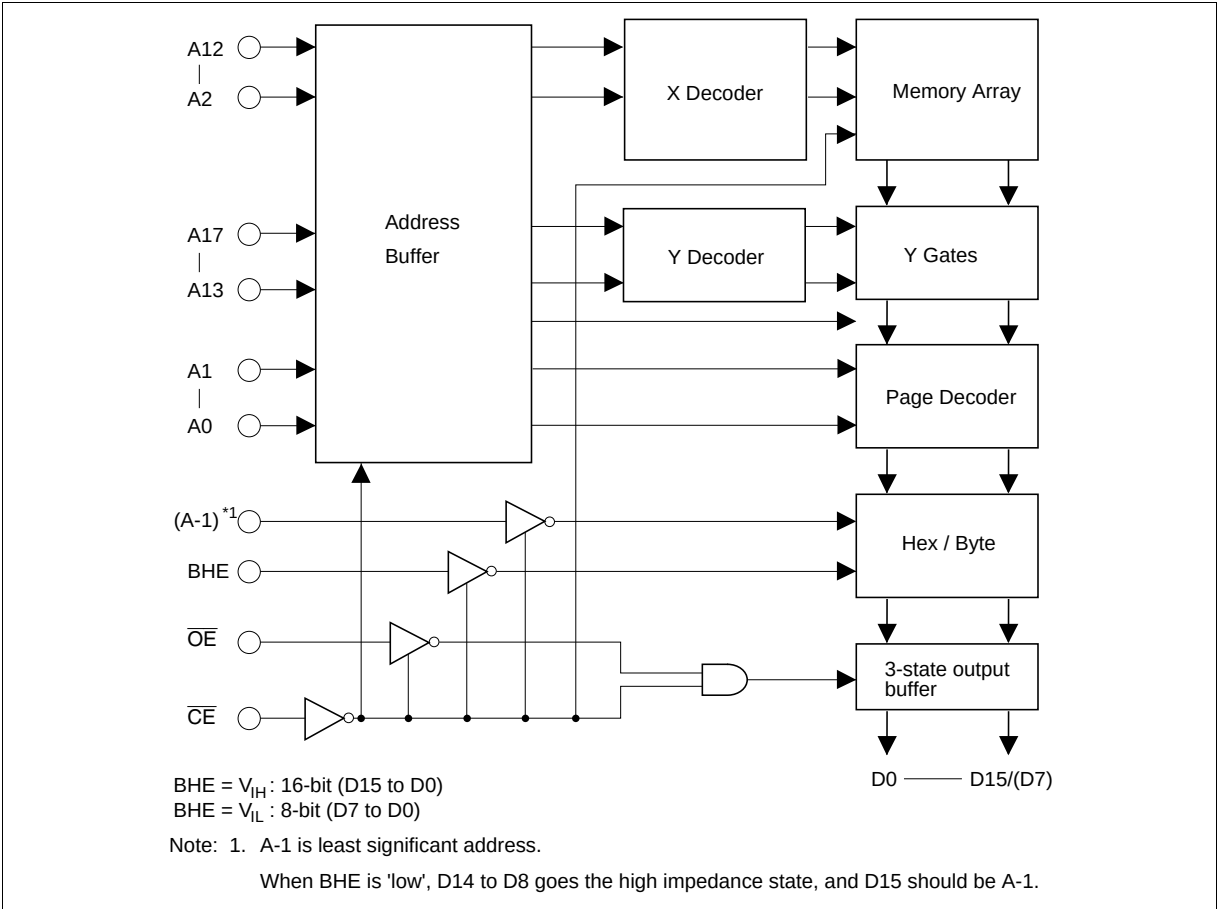


(Top view)

Pin Description

Pin name	Function
A2 to A17	Address inputs
A-1, A0, A1	Page address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	Pin				Data output		Address input	
	$\overline{\text{CE}}$	$\overline{\text{OE}}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	$\times^{*1}$	$\times$	$\times$	High-Z ^{*2}	High-Z	—	—
Output disable	L	H	$\times$	$\times$	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

Notes: 1. $\times$: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ^{*1}	V_{CC}	−0.3 to + 7.0	V
All input and output voltage ^{*1}	$V_{\text{in}}, V_{\text{out}}$	−0.3 to $V_{\text{CC}} + 0.3$	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C
Temperature under bias	T_{bias}	−20 to +85	°C

Note: 1. With respect to V_{SS} .

Recommended DC Operating Conditions ($T_{\text{a}} = 0 \text{ to } + 70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	$V_{\text{CC}} + 0.3$	V
	V_{IL}	−0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I _{CC}	—	100	mA	V _{CC} = 5.5 V, I _{DOUT} = 0 mA, t _{RC} = 100 ns
	Standby	I _{SB1}	—	30	μA	V _{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$
	Standby	I _{SB2}	—	3	mA	V _{CC} = 5.5 V, $\overline{CE} \geq 2.2\text{ V}$
Input leakage current		I _{IL}	—	10	μA	V _{in} = 0 to V _{CC}
Output leakage current		I _{OL}	—	10	μA	$\overline{CE} = 2.2\text{ V}$, V _{out} = 0 to V _{CC}
Output voltage		V _{OH}	2.4	—	V	I _{OH} = −205 μA
		V _{OL}	—	0.4	V	I _{OL} = 1.6 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, V_{in} = 0 V, f = 1MHz)

Parameter		Symbol	Min	Max	Unit
Input capacitance ^{*1}		Cin	—	10	pF
Output capacitance ^{*1}		Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

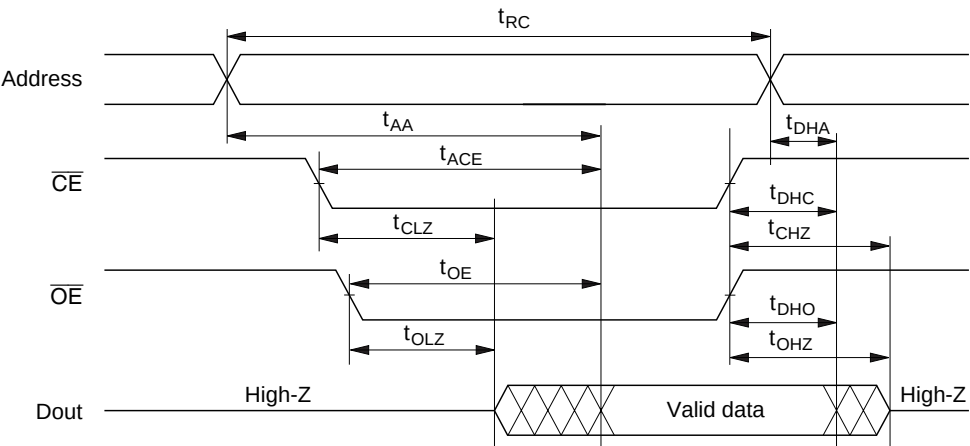
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall time: 5 ns

Parameter	Symbol	HN62454N-10		Unit	Note
		Min	Max		
Read cycle time	t _{RC}	100	—	ns	
Page read cycle time	t _{PC}	40	—	ns	
Address access	t _{AA}	—	100	ns	
Page address access time	t _{PA}	—	40	ns	
$\overline{\text{CE}}$ access time	t _{ACE}	—	100	ns	
$\overline{\text{OE}}$ access time	t _{OE}	—	40	ns	
BHE access time	t _{BHE}	—	100	ns	
Output hold time from address change	t _{DHA}	0	—	ns	
Output hold time from $\overline{\text{CE}}$	t _{DHC}	0	—	ns	
Output hold time from $\overline{\text{OE}}$	t _{DHO}	0	—	ns	
Output hold time from BHE	t _{DHB}	0	—	ns	
$\overline{\text{CE}}$ to output in high-Z	t _{CHZ}	—	30	ns	1
$\overline{\text{OE}}$ to output in high-Z	t _{OHZ}	—	30	ns	1
BHE to output in high-Z	t _{BHZ}	—	30	ns	1
$\overline{\text{CE}}$ to output in low-Z	t _{CLZ}	5	—	ns	
$\overline{\text{OE}}$ to output in low-Z	t _{OLZ}	5	—	ns	
BHE to output in low-Z	t _{BLZ}	5	—	ns	

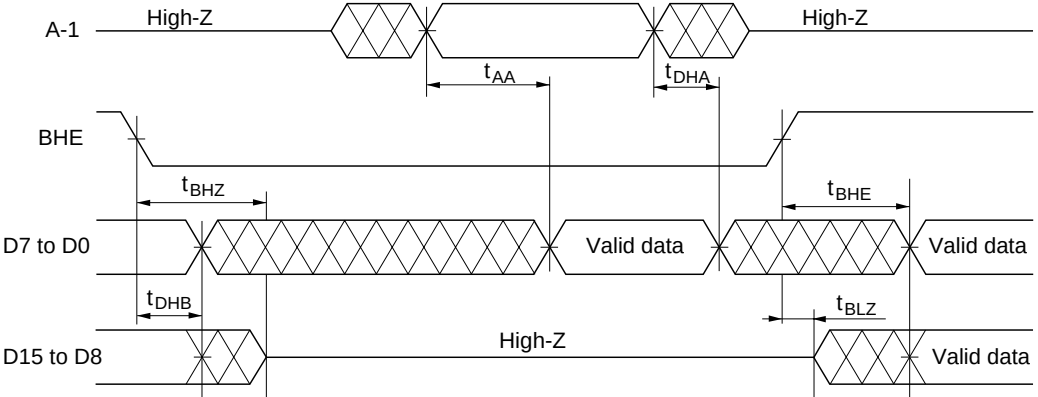
Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

Timing Waveforms

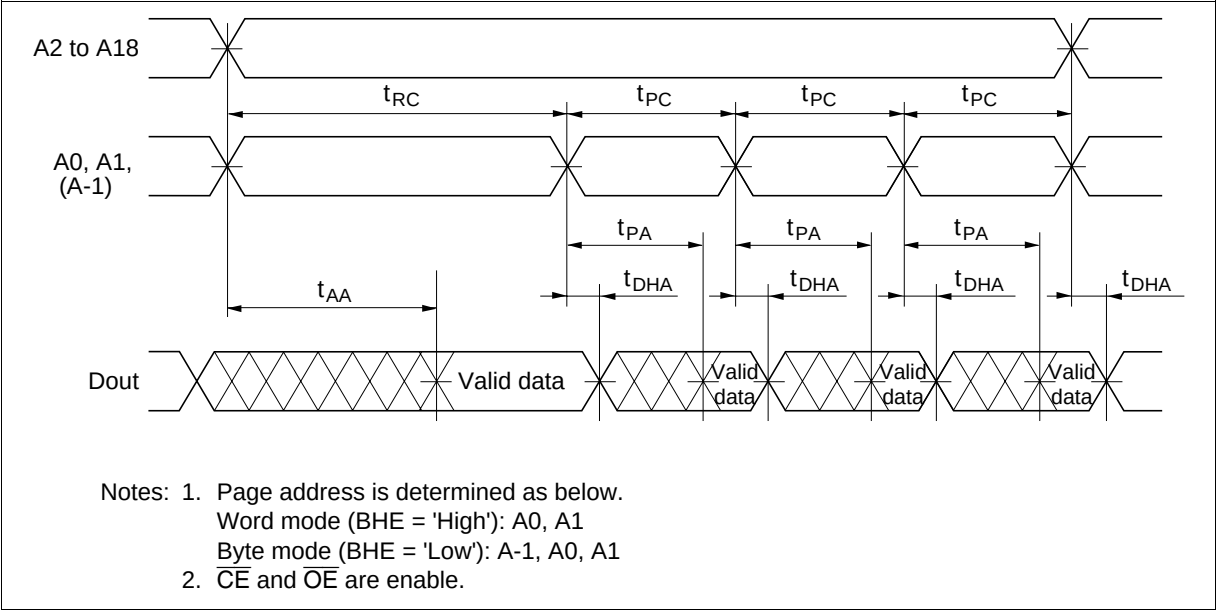
Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



Word Mode, Byte Mode Switch



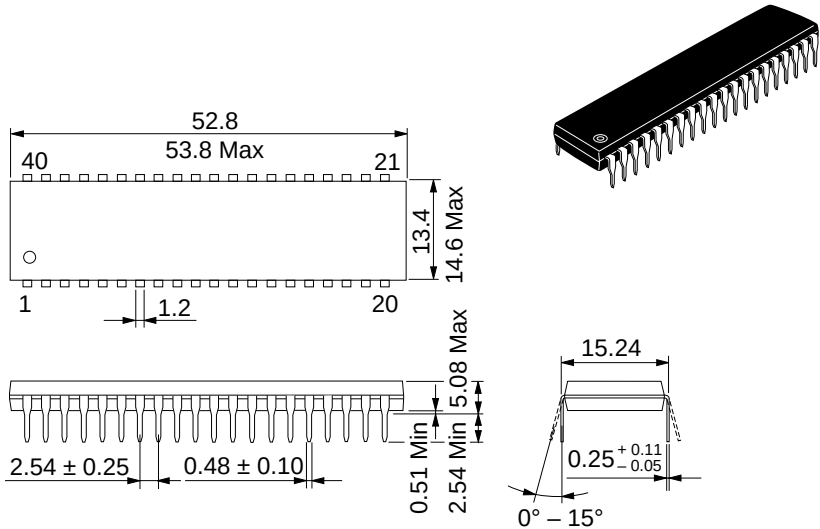
Page Mode



Package Dimensions

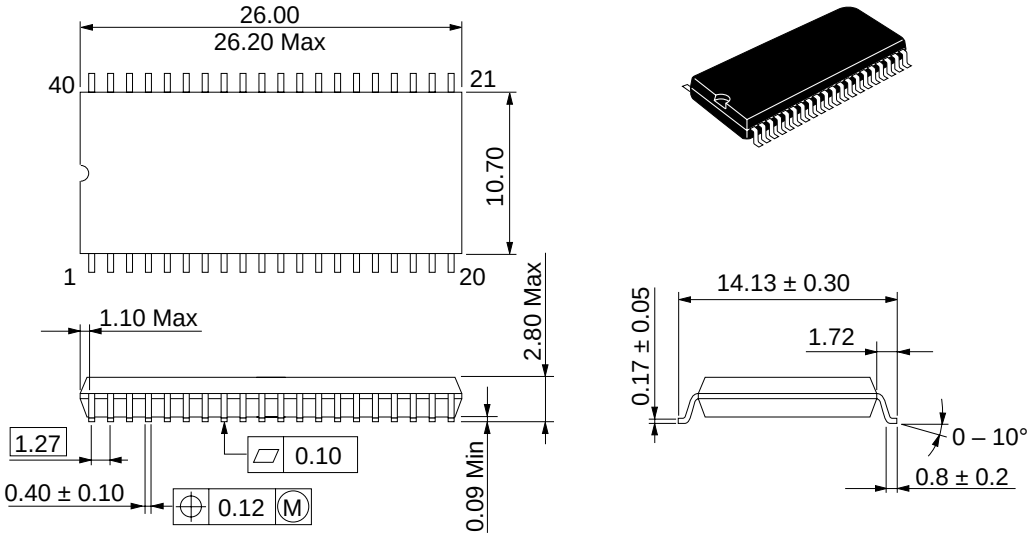
HN62454NP Series (DP-40)

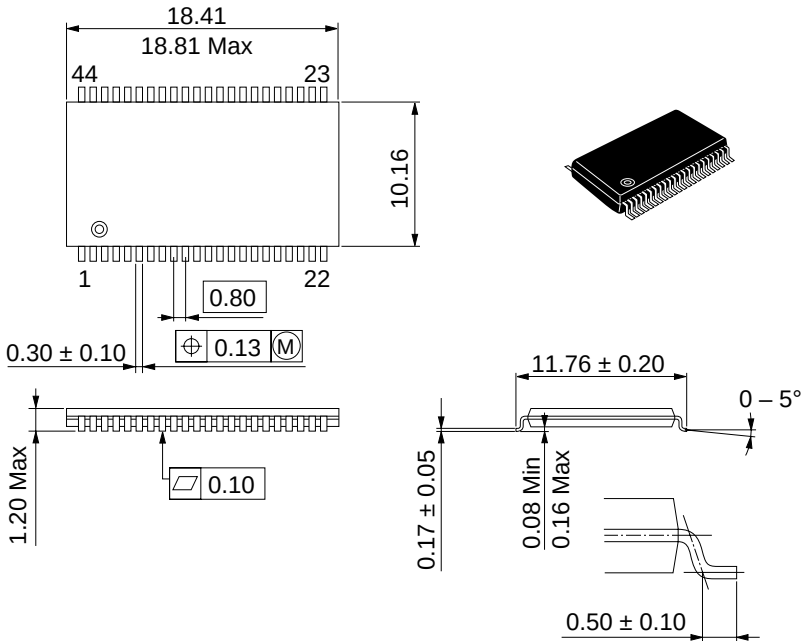
Unit: mm



HN62454NFA Series (FP-40D)

Unit: mm





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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jun. 20, 1995	Initial issue	M. Shirai	T. Wada
0.1	Jul. 19, 1995	Change of Type No. HN62454NP-8 to HN62454NP-85 HN62454NFP-8 to HN62454NFP-85 HN62454NTT-8 to HN62454NTT-85 DC Characteristics I _{CC} Test condition: t _{RC} = 80/100 ns to t _{RC} = 85/100 ns AC Characteristics t _{RC} (min): 80/100 ns to 85/100 ns t _{AA} (max): 80/100 ns to 85/100 ns t _{ACE} (max): 80/100 ns to 85/100 ns t _{BHE} (max): 80/100 ns to 85/100 ns	M. Shirai	T. Wada
1.0	May. 21, 1996	Change of Format Deretion of HN62454N-85 Series DC Characteristics I _{CC} (max): 120/100 ns to 100 ns I _{CC} Test condition: t _{RC} = 85/100 ns to t _{RC} = 100 ns		