VP2612

Video Multiplexer

Supersedes version in June 1995 Digital Video & DSP IC Handbook, HB3923-2 DS3511 - 3.0 June 1996

FEATURES

- Fully integrated H261 video multiplexer
- Inputs data direct from VP2611 source coder
- Output to X21 line buffers
- Line rates from 64kbits/s up to 2Mbits/s
- 100 Pin Quad Flatpack

ASSOCIATED PRODUCTS

- VP2611 H.261 Encoder
- VP2615 H.261 Decoder
- VP2614 Video Demultiplexer
- VP520S CIF/QCIF Converter
- VP510 Colour Space Converter

The VP2612 Video Multiplexer forms part of the Mitel Semiconductor chip-set for video conferencing, video telephony, and multimedia applications. This chip set implements the H261 standard for video compression for line rates of between 64K and 2M bits per second. With a 27MHz clock rate full CIF resolution images can be coded at a frame rate of up to 30Hz.

The device contains all the elements necessary to convert the run length coded data from the VP2611 source coder into an H261 compatible bit stream. It also calculates the differential motion vectors and macroblock addresses from the absolute values received from the VP2611. These values are variable length coded, and bit packed for temporary storage in the transmission buffer. The size of this buffer can be either 256Kbits or 512Kbits. Data from the transmission buffer is output through an X21 compatible serial interface, and consists of frames containing framing bits, data, and the BCH (511,493) forward error correction code.

The system processor interface is used to write data for PTYPE, PSPARE, GSPARE, and to select the source of temporal reference. The interface can also be used to monitor the pointers into the transmission buffer, so that the buffer fullness can be controlled using proprietary software algorithms. In addition to the bus interface, flags are supplied which indicate the start of each macroblock, each FEC stuffed frame, the number of bits per picture is reaching the allowable maximum, and impending buffer overflow.

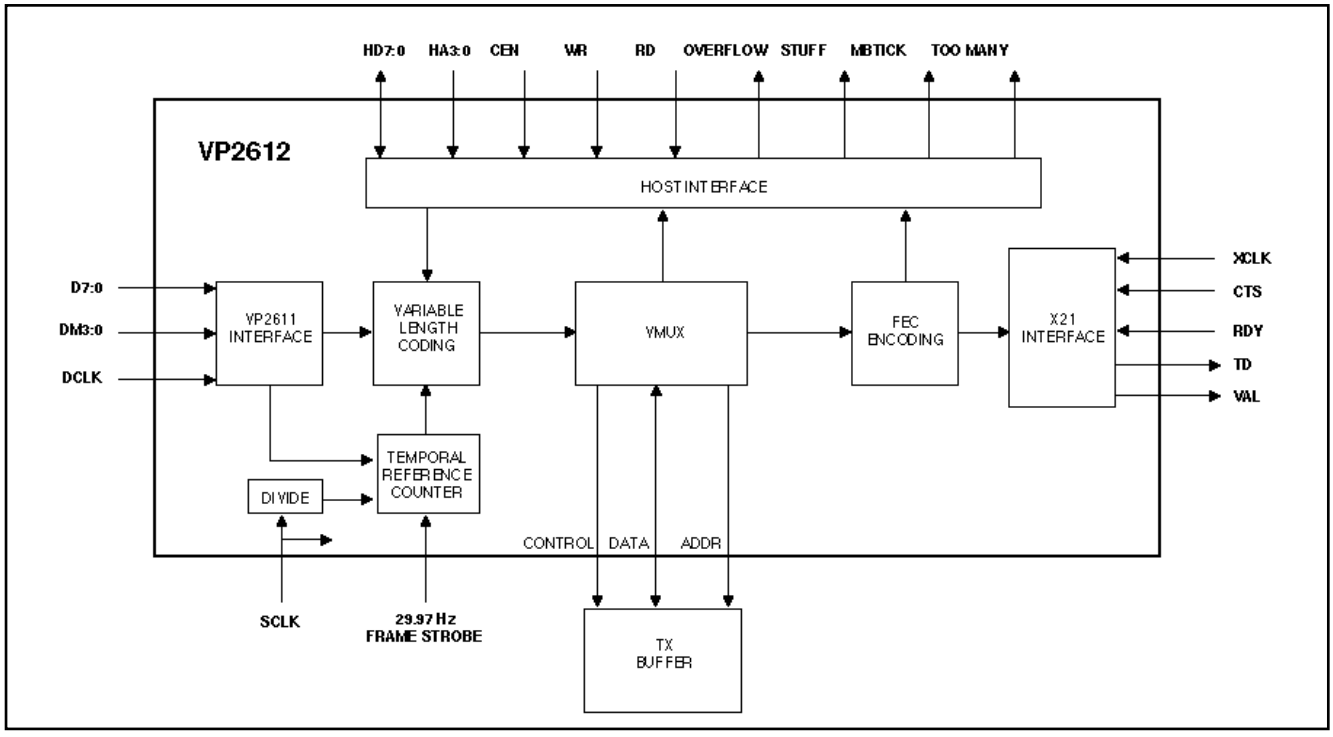


Fig. 1. VP2612 Video Multiplexer

PIN DESCRIPTIONS

DBUS7:0 The input data bus from VP2611. The data type is defined by the value present on DMODE3:0

DMODE3:0 These inputs define the data type present on the data bus D7:0. Polarities are given in Table 1.

DCLK A strobe for DM3:0 and DBUS7:0.The high going edge latches data into the VMUX.

HD7:0 A bidirectional tri-state data bus connecting the VMUX to the system processor.

HA3:0 Four system processor address bits used to address internal registers.

WR An active low write strobe from the system processor.

RD An active low read strobe from the system processor.

CEN An active low chip select input from the system processor.

OVR An active high output which signals impending buffer overflow.

STUFF An active high output that signals that FEC stuffing is occuring.

MTICK An output which pulses high for every macroblock received.

TOOM This active high output indicates that the picture is likely to exceed the allowable number of bits per picture.

VAL This line is taken low to indicate that the VMUX is ready to transmit valid data. The C line in an X21 system.

TD This is the serial data output from the VMUX.

CTS Indicates that the receiver can accept data. The I line in an X21 system.

RDY Indicates that the receiver can accept data. The R line in an X21 system.

XCLK X21 line clock input. 0 to 2.048MHz.

SCLK System clock input. Only the high going edge is used internally, apart from TXWE generation.

FS A 29.97 Hz frame strobe for the temporal reference counter. Must be high for at least 4 SCLK periods.

RES Active low reset signal. Must be low for at least 16 SCLK periods.

TXA14:0 Address output to Transmission buffer.

TXD7:0 Bidirectional data interface to Transmission buffer.

TXE1 Active low chip enable for the Transmission buffer. If a 256kBit buffer is being used this Chip Enable should be used.

TXE2 Active low chip enable for the Transmission buffer. This is used for the optional second memory chip, if a 512kBit buffer is being used.

$\overline{\text{TXWE}}$ Active low write enable for the Transmission buffer.

$\overline{\text{TXOE}}$ Active low O/P enable for the Transmission buffer.

TCK Test clock for JTAG.

TMS Test mode select.

TDI Test data I/P.

TDO Test data O/P.

$\overline{\text{TRST}}$ JTAG reset.

TOE When low ALL O/P pins are high impedance.

NOTE: "Barred" active low signals do not appear with a bar in the main body of the text.

OPERATIONS OF MAJOR BLOCKS

Variable Length Coding

This block is responsible for ordering the data from the VP2611 Encoder into the correct sequence for the H261 bit stream, and for performing the variable length coding. It also uses data supplied by the system controller and the Temporal Reference Counter.

Data for PTYPE, PSPARE, GSPARE is only obtained from the system controller, and only 8 bits of PSPARE and GSPARE information can be transmitted per picture or GOB respectively. The temporal reference can either be obtained from an internal counter, from the VP2611 outputs, or can be written by the system controller. The actual source is determined by bits in a control register as described later. The internal counter is clocked from either a frame clock with a maximum frequency of 29.97Hz, or a 29.97Hz clock derived from the 27MHz system clock, or it simply counts H.261 frames from the encoder.

There is no support provided for macroblock stuffing, however FEC stuffing is implemented, and can be used to provide bit stuffing.

This block is also responsible for converting the absolute values that are output from the V2611 into the relative values that are required in parts of the H261 bitstream. The VMUX has been designed so that it can accept ±15 motion vectors, rather than the +7/-8 motion vectors produced by the VP2611. Thus it will be compatible with any future upgrades to the VP2611 that increase the size of the motion estimator search window.

VMUX Block

The VMUX section performs the bit packing on the data coming from the variable length coder. This data is in the form of a delimiter and a variable number of valid bits. The VMUX section packs these variable length fields into bytes for storage in the transmission buffer.

The transmission buffer is controlled by this block. It thus generates read and write pointers, and performs the arbitration between read and write operations. Buffer level

monitoring is, however, done by the FEC block as described later.

The two address pointers can be read by the system processor, thus allowing the level of the buffer to be monitored. These are provided as 16 bit words with no truncation, and thus require two bytes. The 16 bit value is internally frozen when the most significant byte is requested by the system processor, and for accuracy the write pointer should be read first. There is also a control register bit which selects a buffer size of either 256kbits or 512kbits.

FEC Block

The FEC section performs the framing, and adds the error correction parity bits. If sufficient data for a frame is not available in the transmission buffer, then the frame will be stuffed automatically. There is no absolute threshold at which the FEC will start to stuff, as the buffer level monitor in the FEC only works to a resolution of ±128bits. FEC stuffing can also be forced by setting the "Force FEC stuffing" bit in the VMUX/FEC control register.

If the buffer level reaches a threshold, internally set to 512 short of the buffer being full, the OVERFLOW output is asserted.

DMODE3:0	FUNCTION
0000	GOB Number
0001	MB Number
0010	Control Decisions
0011	Quant Value
0100	Horizontal MV
0101	Vertical MV
0110	Coded Blk Pattern
0111	Sub-Block No.
1000	Zero Run Count
1001	RLC Coefficient
1010	Not Used
1011	Not Used
1100	Not Used
1101	Not Used
1110	Not Used
1111	Wait State

Table 1

This is to warn the system processor that drastic action is needed to avert a buffer overflow, which will result in corruption and loss of data. Since the buffer level monitor only works to resolution of ±128bits, then the overflow detection can only be accurate to ±128bits.

VP2611 Interface

The VMUX has been designed to interface directly to the VP2611 encoder, with no buffering. The interface consists of two buses DBUS7:0 and DMODE3:0, and a strobe signal DCLK. The value on DMODE3:0 identifies the data type on DBUS7:0 during the same period (see Table 1).

The output of the VP2611 is structured such that the data on DBUS7:0 and DMODE3:0 is always valid for at least two cycles, and DCLK is high for minimum of one cycle. The rising DCLK edge occurs one cycle after DBUS7:0 and DMODE3:0 are valid, as shown in Figure 2.

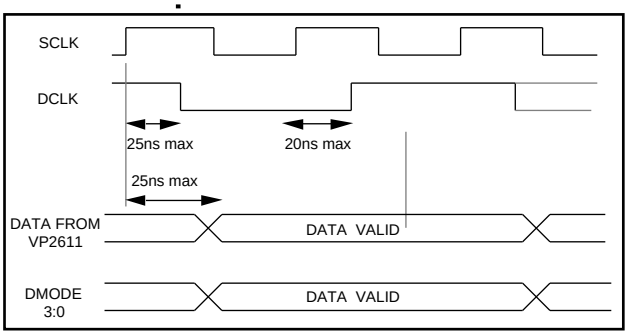


Figure 2. DBUS Timing

The sequence of events, and the duration of each event, is shown in Figure 3. These duration times have been chosen to satisfy the internal requirements of the VP2612, and Wait States are inserted such that the time to transfer a macroblock is always 2064 SCLK periods.

The parameters used by the VP2612 are described in more detail below;

GOB Number : The current GOB Number is provided on DBUS3:0 after the Control Decisions byte. (DBUS3 is MSB).

MB Number : After the GOB Number, the macroblock Number is provided on DBUS5:0 (DBUS5 is MSB).

Control Decisions : This byte shows which control decisions have been taken for the forthcoming macroblock, and is the first in the sequence. DBUS0 will be high if a Fixed Macroblock (FIX MB) was enforced i.e. no new data will be transmitted this macroblock. DBUS1 indicates whether Inter (high) or Intra (low) coding was used for the macroblock. DBUS2 will be high if the macroblock was filtered, and DBUS3 will be high if motion compensation was used. DBUS5 will be high if the current frame is being coded in FAST UPDATE mode. In this mode the complete frame will be intra coded. DBUS6 will be high if the current frame is a SKIP FRAME i.e. not being coded - so no coefficients will be transmitted. DBUS4 and DBUS7 are not used.

Quant Value :The quantisation value used in processing the current macroblock is provided on DBUS4:0 (DBUS4 is MSB). This represents an actual quantisation level between 2 and 62, in steps of 2 and as defined in H.261.

Horizontal MV : If motion compensation was used the horizontal component of the motion vector will be provided on DBUS4:0 (DBUS4 is MSB). (This 5 bit value represents a two's complement number in the range (-15 to +15) (although only vectors in the range +7/-8 are currently possible with the VP2611). If motion compensation was not used this is a don't care value.

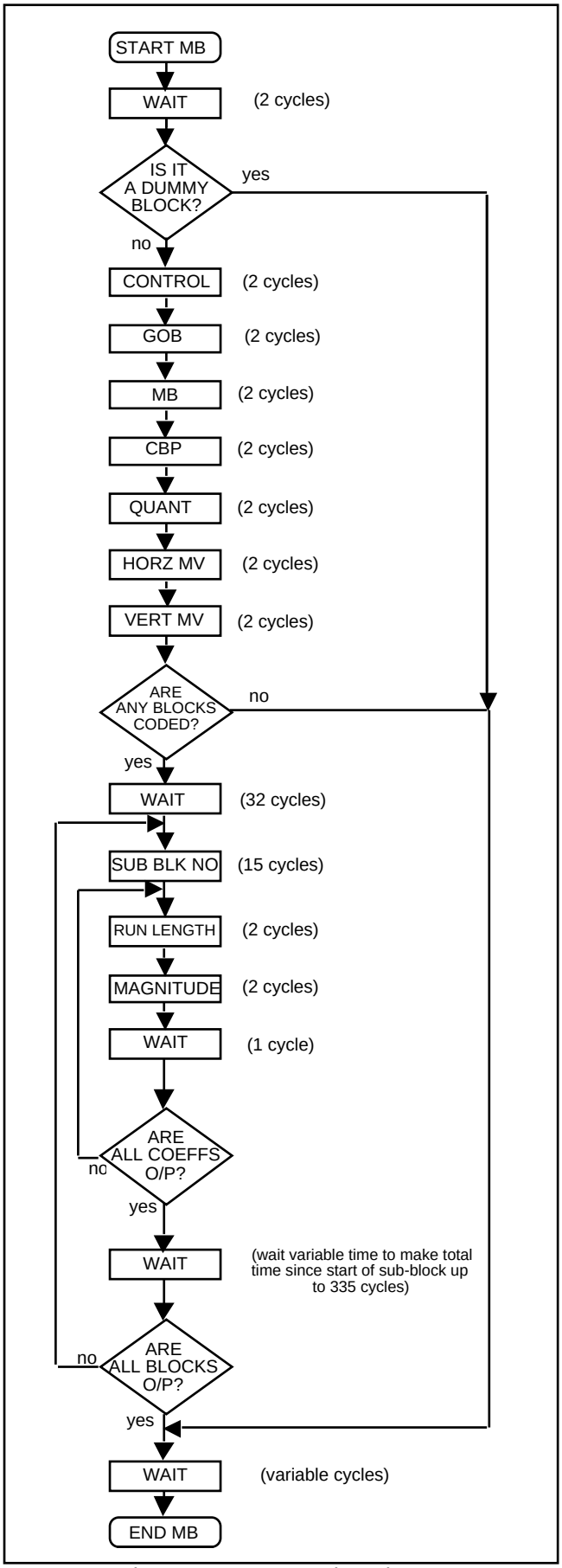


Figure 3. DBUS Port Flow Chart

Vertical MV : If motion compensation was used the vertical component of the motion vector will be provided on DBUS4:0 (DBUS4 is MSB). (This 5 bit value represents a two's complement number in the range ±15 (although only vectors in the range (±7) are currently possible with the VP2611). If motion compensation was not used this is a don't care value.

Coded Block Pattern : This byte contains a 6 bit linear code that indicates which of the sub-blocks actually contain coded data. DBUS6 will be high if sub-block 1 contains coded data, through to DBUS1 being high if sub-block 6 contains coded data. DBUS7 and DBUS0 are not used.

Sub-block Number : An identifier for the run length coded coefficients which are about to be made available. DBUS2:0 contain the coded sub-block number from 1 to 6. All zero sub-blocks will not be produced, and their corresponding numbers will not appear.

Zero Run Count : The number of zero valued coefficents preceding the next non zero coefficient is provided on DBUS5:0 (DBUS5 is MSB). Normally, DBUS7:6 are low, except to signify the end of a Sub-block, when they will both be high. Zero Run Count is always followed by a coefficient, even at the end of a sub-block.

RLC Coefficient : This byte contains the 8 bit coefficient value. It will always be a non-zero value, except when the previous Zero Run Count signalled the end of sub-Block. A zero value is then possible since, as stated above, the run count is always followed by a coefficient byte, which may be zero if the last coefficient is zero.

Wait State : This indicates that no valid data is being output from the DBUS port during this cycle. No DCLK is produced for this state.

SYSTEM PROCESSOR INTERFACE

The system processor interface is a memory mapped microprocessor compatible interface. It has been designed for use with any system processor, and consists of the following buses and signals:

HD7:0	Processor Data Bus
HA3:0	LSBs of address bus
WR	Active Low Write strobe
RD	Active Low Read strobe
CEN	Decoded Active Low chip select

Detailed interface timing is shown in Figure 4. Since there are several internal pipeline registers which are clocked by SCLK, then access times and strobe widths are dependent on the period of SCLK.

Table 2 shows the addresses used for each of the user accessible registers, and the function of each register is described in detail below.

Address	Function	Read / Write
0	PTYPE	W
1	Temporal Reference	W
2	PSPARE	W
3	TR Source	W
4	GSPARE	W
5	Not Used	
6	Not Used	
7	Not Used	
8	TX-buffer Write Address MSB	R
9	TX-buffer Write Address LSB*	R
A	TX-buffer Read Address MSB	R
B	TX-buffer Read Address LSB*	R
C	FEC / VMUX status word	W
D	Bits per Picture Threshold	W
E	Not Used	
F	Not Used	
* N.B. The LSB must be read after the appropriate MSB.		

Table 2. Address Locations

PTYPE This is the picture type as defined in H261. The bits are assigned as follows:

Bit 0 Split screen indicator, "0" off, "1" on.
Bit 1 Document camera indicator, "0" off, "1" on.
Bit 2 Freeze picture release, "0" off, "1" on.
Bit 3 Source Format, "0" QCIF, "1" CIF.
Bit 4:5 Both are set to one as presently defined in the H261 specification

[Bit 0 is LSB].

These values can be changed at will by the system processor, and will be transmitted at the start of each picture.

Temporal Reference If the temporal reference is being written from the system processor, then the 5 LSB's in this register are used to define the next temporal reference value to be transmitted.

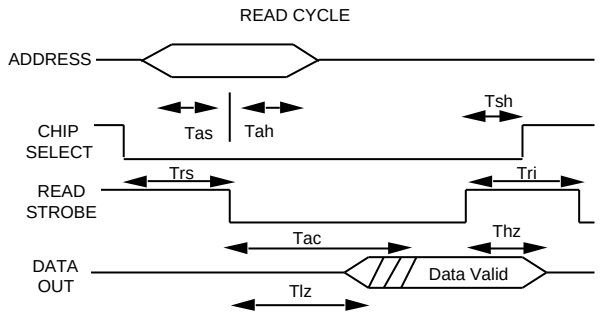
PSPARE This register holds 8 bits of PSPARE information which may be transmitted for each picture. The data in the PSPARE register will be transmitted at the start of the next picture after it has been written. Once an item of data has been transmitted, it will not be re-transmitted until data is written from the system processor. It is the responsibility of the system processor to ensure that it does not rewrite to this register before the previous value has been transmitted. This can be done by utilizing a frame interrupt from the video source in conjunction with the MBTICK output from the VMUX.

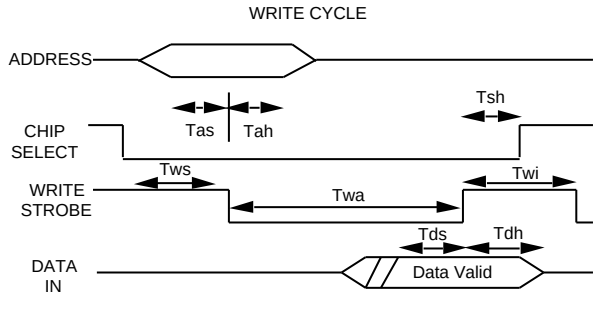
TR Source The 3 LSB's in this register define the source for the strobe used by the 5 bit temporal reference counter. When the sytem processor is selected, the counter value is replaced by the contents of the Temporal Reference Register.

VALUE	SOURCE
0XX	System Processor
100	Actual coded frames from the VP2611 are counted
101	SCLK is divided down to provide a 29.97 Hz frame strobe
110	The strobe is provided by the frame strobe input pin (FS)
111	Illegal

GSPARE This register holds 8 bits of GSPARE information which may be transmitted every GOB. Once written the data is transmitted at the start of the next GOB, but will not be re-transmitted until the system processor again writes to this address. The system processor must ensure that data is not overwritten before it is used.

TX Buffer Addresses These allow the system processor to monitor the level of the buffer. The write pointer should be read first to minimize the error between the the two





CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Cip Select Set Up Time	Trs	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe In active Time	Tri	Øns	
Data Access Time	Tac	4Øns	10 +5Øns
Delay to O/P's low Z	Tlz		25ns
Delay to O/P's high Z	Thz		25ns

NOTE

Ø is the period of the input clock

CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Chip Select Set Up Time	Tws	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe In active Time	Twi	2Øns	
Strobe Active Time	Twa	2Øns	
Data Set Up Time	Tds	10ns	
Data Hold Time	Tdh	10ns	

Figure 4. Host Controller Timing

values. With a 2Mbits/sec line the error will increase at a rate of 0.25 bytes per microsecond. Reading the most significant bytes will trigger the internal latching of the least significant bytes.

FEC / VMUX Control This register controls the operation of the transmission buffer and the FEC block. Actions taken when bits are set are given below;

BIT	FUNCTION
0	Select 512K buffer. The buffer size must not be changed during normal operation and must be defined within 2.4 ms of reset.
1	Enable FEC framing.The option to disable FEC framing is only provided as a test mode.
2	Force FEC stuffing. If force FEC stuffing is selected it will start at the beginning of the next frame and only stop at the start of subsequent frames. The system processor must ensure that the transmission buffer does not overflow with forced stuffing. In normal operation FEC stuffing only occurs when there is insufficient data in the transmission buffer.

Bits Per Picture Register When the number of bits which have been coded has been subtracted from the maximum possible (as defined by H.261), and the result reaches the value in this register, then the TOO MANY interrupt will be generated. The programmed value thus defines in Kbits the number of bits which may still be generated before reaching the maximum allowed. The default value is 8 Kbits, and the maximum number used internally changes between CIF and QCIF.

INTERRUPT OUTPUTS

The special signals listed below are provided to drive timers and interrupt inputs on the system processor.

OVERFLOW (OVR)
FEC STUFF (STUFF)
MACROBLOCK TICK (MTICK)
TOO MANY (TOOM)

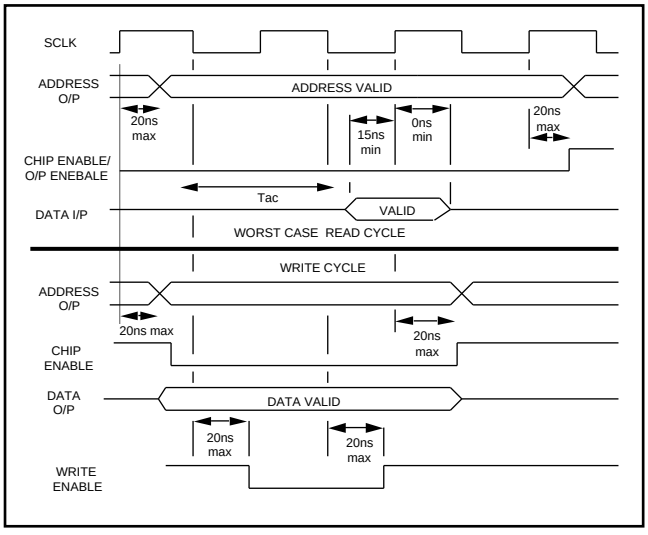


Figure 5. Transmission Buffer Timing

They perform the following functions:

OVR This line signals an impending buffer overflow. When the buffer reaches 512±128 bits from being full this line will be taken high, and will remain high until the buffer level falls below the threshold. It is intended that this line be used as a processor interrupt, to signal that drastic action must be taken.

STUFF This line signals that FEC stuffing is occuring, and can be used to monitor the amount of stuffing being performed. It will pulse high once at the start of each FEC stuffed frame, the length of the pulse being one line clock period. It is intended that this should be used to clock a system processor counter, to keep a running total of the number of FEC stuffed frames.

MTICK This output pulses high once for every Macroblock received from the VP2611. The pulse is 3 clock cycles in duration, and the leading edge will occur 6 SCLK cycles after the Macroblock address was received from the VP2611. It is anticipated that this should be used to clock a counter in the system processor, so that the system processor can keep track of which MB is being processed. In conjunction with the frame pulse this will enable the system processor to write information to the VP2611 at appropriate times.

TOOM This signal indicates that the present picture has reached a threshold relative to the maximum number of bits per picture allowed by H.261 (256k if CIF, 64k if QCIF). It is set when the number of bits remaining before the maximum will be exceeded reaches the value in the Bits Per Picture Register, and stays high until the end of the current picture.

TRANSMISSION BUFFER INTERFACE

The transmission buffer can consist of either one or two 32K x 8 bit static RAMs. Fifteen address outputs are provided for direct connection to the memory devices, and two RAM select pins are provided to define the device in use. If only a single device is being used then CE2 is redundant.
An internal FIFO is provided to average out high speed bursts of transmission buffer cycles. This allows the external SRAM read cycles to occupy at least three SCLK periods. Detailed timing for the buffer is given in Figure 5, and shows that with a 27 MHz clock the RAM must have an access time of less than 39 nanoseconds. Figure 5 illustrates the worst case read access time, which occurs when a second read cycle follows the first without an intermediate write cycle. Chip enable and output enable remain low from the first read cycle.
The write cycle uses two SCLK periods and requires the use of both the falling and rising edges of SCLK. The Write Enable output thus remains active for one SCLK period minus differential rising and falling edge delays. These are limited to two nanoseconds. Note that when consecutive read or write operations take place then Chip Enable will remain active, and not go inactive between cycles.

LINE INTERFACE

A serial interface is provided which facilitates the operation of the encoder and decoder in a back to back configuration. It is similar in operation to an X21 interface but does not support balanced lines. Alternatively the interface can be used in a simple serial manner by tying the control lines to fixed logic levels. It uses the following signals:

XCLK	Line rate clock
VAL	Ready to send
TD	Transmitted Data
CTS	Clear To Send
RDY	Receiver ready

Of these signals XCLK, CTS and RDY are supplied by the receiving device, the latter two indicating that the receiver is ready to accept data. The VAL line is used to signal that the VMUX is ready to start transmitting valid data, and the TD line provides the data. The signaling convention is as follows:

CTS = 1 Receiving device not ready
RDY = 0

CTS = 0 Receiving device ready to accept data
RDY = X

CTS =1 Receiving device ready to accept data
RDY =1

The VAL line is taken high by the reset input, and when the receiving device signals that it is ready to accept data then the VP2612 takes the VAL line low on a falling edge of an XCLK. The data is then clocked out on subsequent falling edges of the XCLK signal, so that it can be sampled by the receiver on the rising edge of the clock.

If a simple serial interface is required, the CTS input should be tied low and the RDY input tied high. It is possible to use a variable rate clock provided the maximum instantaneous bit rate does not exceed 8Mbits/s, and the average clock rate over 32 bits does not exceed 2Mbits/s. Timing delays with respect to the incoming XCLK are shown in Figure 6.

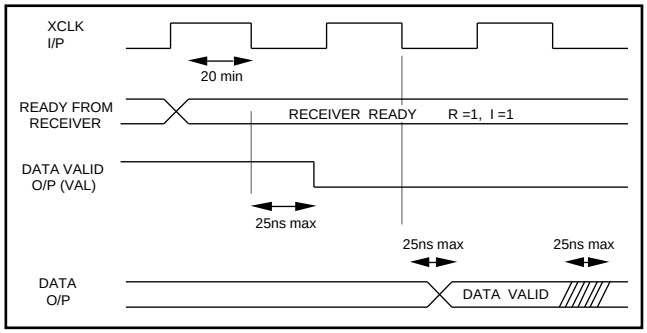


Figure 6. Serial Interface Timing

JTAG Test Interface

The VP2612 includes a test interface consisting of a boundary scan loop of test registers placed between the pads and the core of the chip. The control of this loop is fully JTAG/ IEEE 1149-1 1990 compatible. Please refer to this document for a full description of the standard.

The interface has five dedicated pins: TMS, TDI, TDO, TCK and TRST. The TRST pin is an independent reset for the interface controller and should be pulsed low, soon after power up; if the JTAG interface is not to be used it can be tied low permanently. The TDI pin is the input for shifting in serial instruction and test data; TDO the output for test data. The TCK pin is the independent clock for the test interface and registers, and TMS the mode select signal.

TDI and TMS are clocked in on the rising edge of TCK, and all output transitions on TDO happen on its falling edge.

Instructions are clocked into the 3 bit instruction register (no parity bit) and the following instructions are available.

Instruction Register (MSB first)	**Name**
111	BYPASS
000	EXTEST
010	SAMPLE/PRELOAD

The TAP controller used in this device does not support a separate INTEST instruction but allows EXTEST to drive the internals of the device as well as to drive the output pins. Output enables are thus present in the chain which are not connected to pins but which allow EXTEST to be used to control the impedance of all the outputs. The JTAG signal TXD controls the TXD bus, HD controls the HD bus, and TOPS controls all remaining outputs. The TOE pin, which can separately be used to control the impedance of all the outputs, can be monitored as an input through the scan chain but cannot be used to control the outputs through the TAP controller.

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage VDD	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to VDD + 0.5V
Output voltage V_{OUT}	-0.5V to VDD+ 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	100°C
Package power dissipation	1000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0 C to +70°C VDD = 5.0v ± 5%

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	3.0V for SYSCLK and DCLK
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{DD}
Output S/C current	I_{SC}	10		300	mA	

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	N/C	21	GND	41	HD3	61	TXD1	81	TXA1
2	N/C	22	DCLK	42	HD4	62	TXD0	82	TXA0
3	N/C	23	XCLK	43	HD5	63	TXA14	83	TXWE
4	TOE	24	RDY	44	HD6	64	TXA13	84	TXOE
5	OVR	25	CTS	45	HD7	65	TXA12	85	GND
6	DMODE0	26	TD	46	VDD	66	TXA11	86	VDD
7	DMODE1	27	VAL	47	GND	67	TXA10	87	TXE2
8	DMODE2	28	N/C	48	WR	68	TXA9	88	TXE1
9	DMODE3	29	N/C	49	RD	69	TXA8	89	TDI
10	GND	30	N/C	50	CEN	70	TXA7	90	TMS
11	VDD	31	HA0	51	N/C	71	VDD	91	TRST
12	DBUS0	32	HA1	52	N/C	72	GND	92	TCK
13	DBUS1	33	HA2	53	TXD7	73	TXA6	93	TDO
14	DBUS2	34	HA3	54	TXD6	74	TXA5	94	VDD
15	DBUS3	35	SCLK	55	TXD5	75	TXA4	95	GND
16	DBUS4	36	GND	56	TXD4	76	TXA3	96	RES
17	DBUS5	37	VDD	57	TXD3	77	TXA2	97	MTICK
18	DBUS6	38	HD0	58	TXD2	78	N/C	98	STUFF
19	DBUS7	39	HD1	59	GND	79	N/C	99	TOOM
20	VDD	40	HD2	60	VDD	80	N/C	100	FS

Pin Out Diagram

PAD	TYPE	REG No.	PAD	TYPE	REG No.
TXE1	O/P	88	HD5	(input)	44
TXE2	O/P	87	HD4	(output)	43
TX0E	O/P	86	HD4	(input)	42
TXWE	O/P	85	HD3	(output)	41
TXA0	O/P	84	HD3	(input)	40
TXA1	O/P	83	HD2	(output)	39
TXA2	O/P	82	HD2	(input)	38
TXA3	O/P	81	HD1	(output)	37
TXA4	O/P	80	HD1	(input)	36
TXA5	O/P	79	HD0	(output)	35
TXA6	O/P	78	HD0	(input)	34
TXA7	O/P	77	HD	I/P	33
TXA8	O/P	76	SCLK	I/P	32
TXA9	O/P	75	HA3	I/P	31
TXA10	O/P	74	HA2	I/P	30
TXA11	O/P	73	HA1	I/P	29
TXA12	O/P	72	HA0	I/P	28
TXA13	O/P	71	VAL	O/P	27
TXA14	O/P	70	TD	O/P	26
TXD	I/P	69	CTS	I/P	25
TXD0	(input)	68	RDY	I/P	24
TXD0	(output)	67	XCLK	I/P	23
TXD1	(input)	66	DCLK	I/P	22
TXD1	(output)	65	DBUS7	I/P	21
TXD2	(input)	64	DBUS6	I/P	20
TXD2	(output)	63	DBUS5	I/P	19
TXD3	(input)	62	DBUS4	I/P	18
TXD3	(output)	61	DBUS3	I/P	17
TXD4	(input)	60	DBUS2	I/P	16
TXD4	(output)	59	DBUS1	I/P	15
TXD5	(input)	58	DBUS0	I/P	14
TXD5	(output)	57	DMODE3	I/P	13
TXD6	(input)	56	DMODE2	I/P	12
TXD6	(output)	55	DMODE1	I/P	11
TXD7	(input)	54	DMODE0	I/P	10
TXD7	(output)	53	OVR	O/P	9
CEN	I/P	52	TOE	I/P	8
RD	I/P	51	TOPS	I/P	7
WR	I/P	50	TSE	I/P	6
HD7	(output)	49	DEN	I/P	5
HD7	(input)	48	FS	I/P	4
HD6	(output)	47	TOOM	O/P	3
HD6	(input)	46	STUFF	O/P	2
HD5	(output)	45	MTICK	O/P	1
			RES	I/P	0

JTAG Register Allocation

ORDERING INFORMATION

VP2612 CG GPFR (Commercial - Plastic QFP package)

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