14A, 100V, 0.180 Ohm, N-Channel Power MOSFET

The 2N6756 is an N-Channel enhancement mode silicon gate power field effect transistor designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Ordering Information

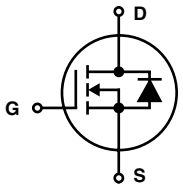
PART NUMBER	PACKAGE	BRAND
2N6756	TO-204AA	2N6756

NOTE: When ordering, use the entire part number.

Features

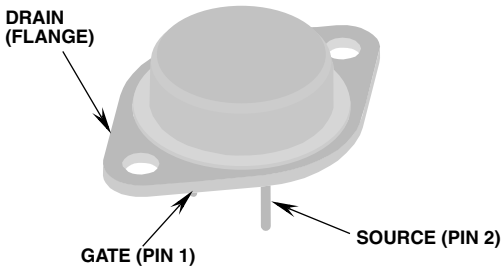
- 14A, 100V
- $r_{DS(ON)} = 0.180\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-204AA



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		2N6756	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100	V
Continuous Drain Current	I_D	14	A
$T_C = 100^oC$	I_D	9.0	A
Pulsed Drain Current (Note 3)	I_{DM}	30	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation (Figure 1)	P_D	75	W
$T_C = 100^oC$	P_D	30	W
Linear Derating Factor (Figure 1)		0.6	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

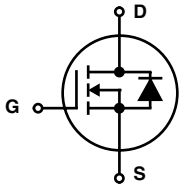
NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 1.0mA, V_{GS} = 0V	100	-	-	V
Gate Threshold Voltage (Note 2)	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 1mA	2	-	4	V
Zero Gate Voltage Drain Current (Note 2)	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	0.1	1.0	mA
		V_{DS} = Max Rating, V_{GS} = 0V, $T_C = 125^oC$	-	0.2	4.0	mA
On-State Drain Voltage (Note 2)	$V_{DS(ON)}$		-	-	2.52	V
Gate to Source Leakage Current (Note 2)	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 9A, V_{GS} = 10V	-	0.14	0.18	Ω
		I_D = 9A, V_{GS} = 10V, $T_C = 125^oC$	-	-	0.33	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 15V, I_D = 9A	4.0	5.5	12.0	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \cong 36V$, I_D = 9A, $Z_O = 15\Omega$ (Figures 12, 13) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	-	30	ns
Rise Time	t_r		-	-	75	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	40	ns
Fall Time	t_f		-	-	45	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 7)	350	600	800	pF
Output Capacitance	C_{OSS}		150	300	500	pF
Reverse Transfer Capacitance	C_{RSS}		50	100	150	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	-	1.67	$^oC/W$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source Current (Body Diode)	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier 	-	-	14	A
Pulse Source Current (Body Diode)	I_{SM}		-	-	30	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_C = 25^oC$, $I_{SD} = 14A$, $V_{GS} = 0V$	0.90	-	1.8	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, $I_{SD} = I_{SM}$, $dI_{SD}/dt = 100A/\mu s$	-	300	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^oC$, $I_{SD} = I_{SM}$, $dI_{SD}/dt = 100A/\mu s$	-	4.0	-	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

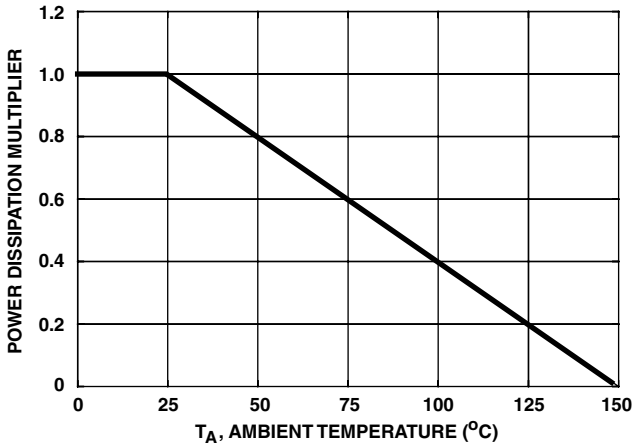


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

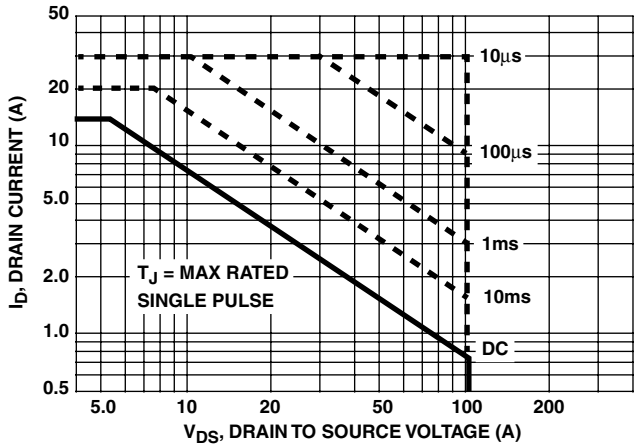


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

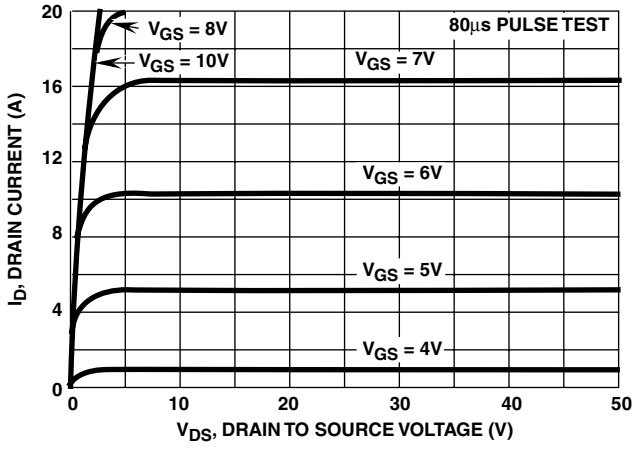


FIGURE 3. OUTPUT CHARACTERISTICS

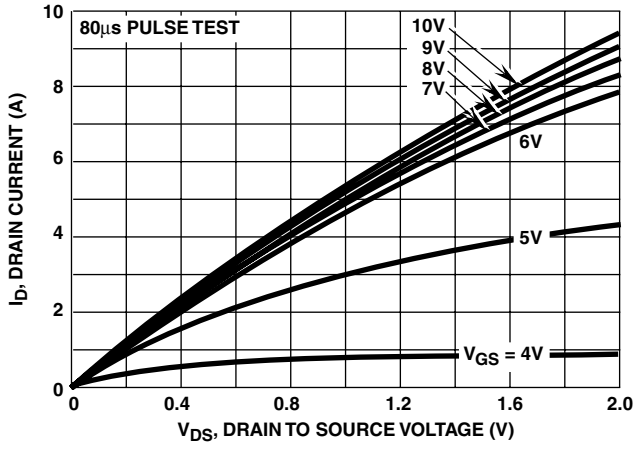


FIGURE 4. SATURATION CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified **(Continued)**

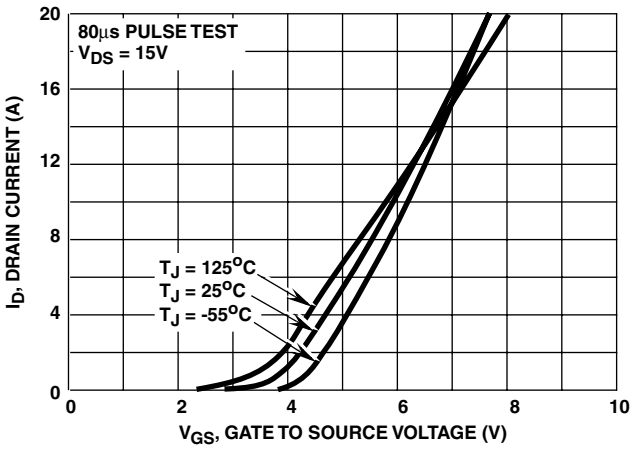


FIGURE 5. TRANSFER CHARACTERISTICS

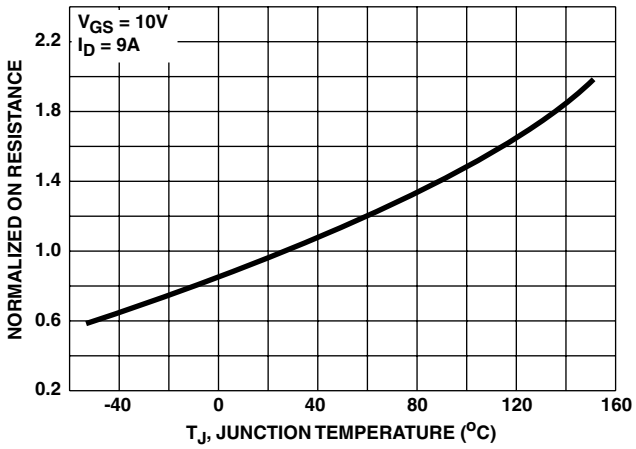


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

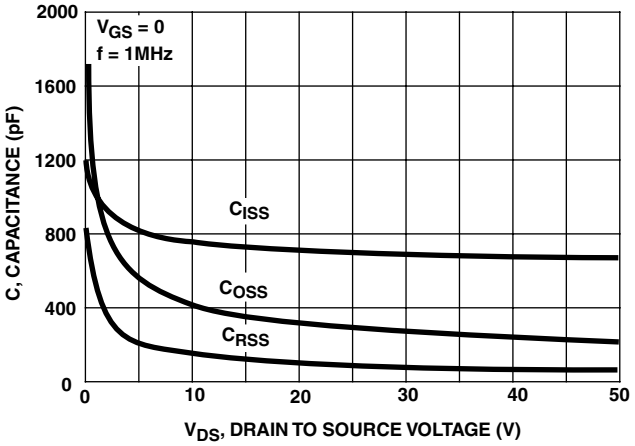


FIGURE 7. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

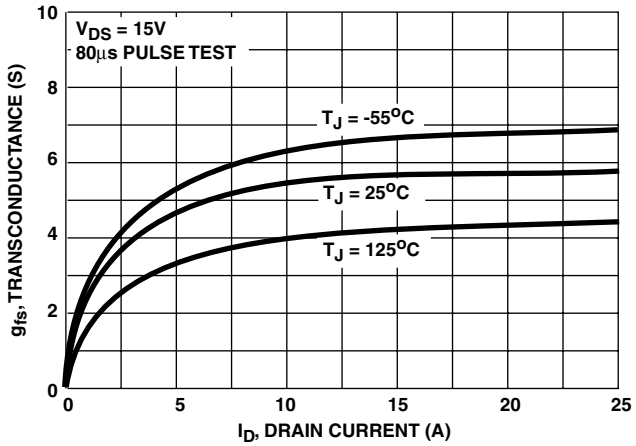


FIGURE 8. TRANSCONDUCTANCE vs DRAIN CURRENT

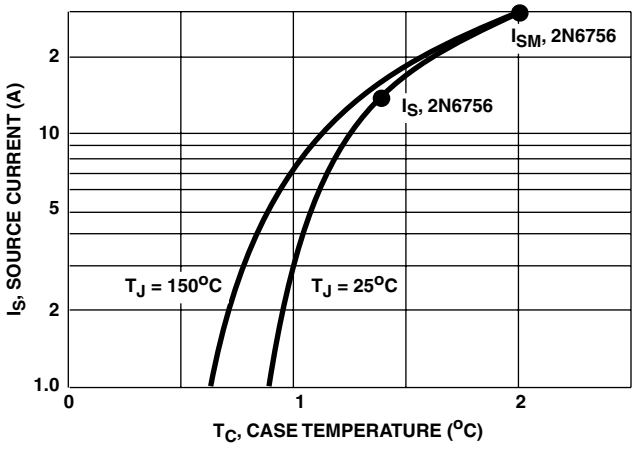


FIGURE 9. SOURCE TO DRAIN DIODE VOLTAGE

Test Circuits and Waveforms

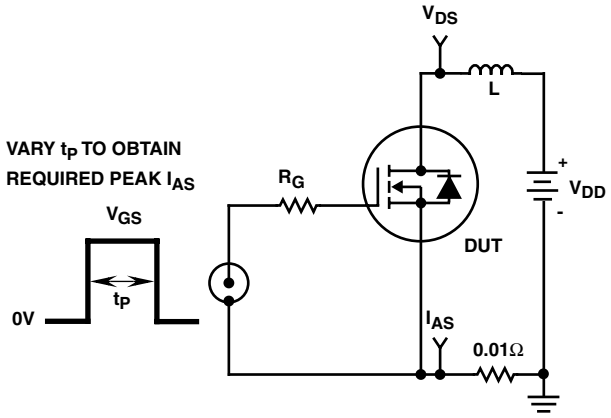


FIGURE 10. UNCLAMPED ENERGY TEST CIRCUIT

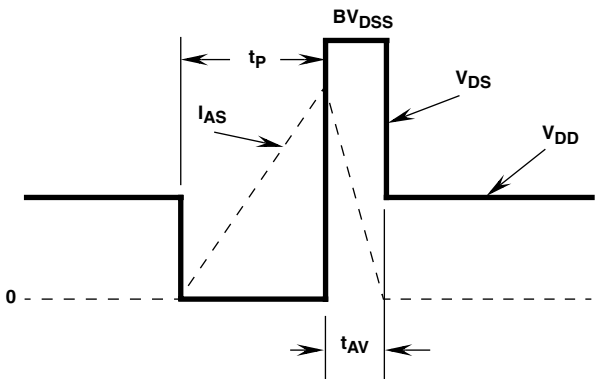


FIGURE 11. UNCLAMPED ENERGY WAVEFORMS

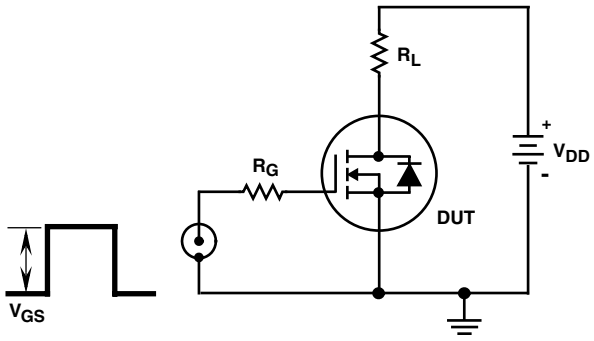


FIGURE 12. SWITCHING TIME TEST CIRCUIT

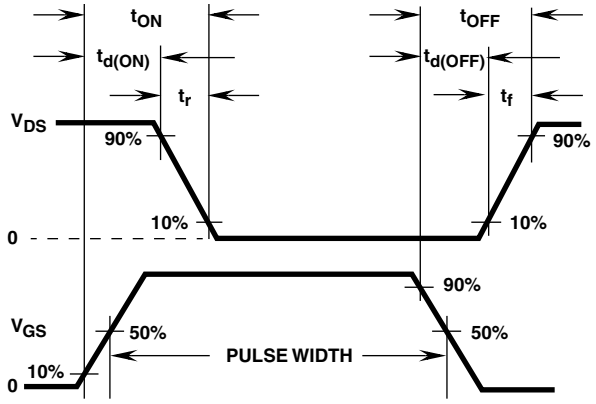


FIGURE 13. RESISTIVE SWITCHING WAVEFORMS

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