MX29VW160T/B

16M-BIT [2M x 8-BIT/1M x16-BIT] SIMULTANEOUS READ/WRITE SINGLE 2.5V OPERATION FLASH MEMORY

FEATURES

- Two Memory Banks for Simultaneous Read/Write operations
  - Host system can program or erase in one bank and simultaneously read from the other bank
  - Zero latency between simultaneous Read/Write operations
  - Read-While-Erase/Program
- Extended Single-supply voltage range from 2.25V to 3.0V for read, erase and write operations
- JEDEC-standard EEPROM commands
- Minimum 100,000 write/erase cycles
- Fast Access time: 120ns
- Optimized block architecture:
  - Bank A
  - Eight 8K Byte (4K Word) blocks
  - Three 64K Byte (32K Word) blocks
  - Bank B
  - Twenty-eight 64K Byte (32K Word) blocks
- $\overline{\text{Data}}$ polling and toggle bit feature for detection of program or erase cycle completion
- Ready/$\overline{\text{Busy}}$ output (RY/$\overline{\text{BY}}$): Hardware method for detection of program or erase cycle completion
- Automatic standby mode: When addresses remain stable,automatically switch themselves to low power mode(1uA Typical)
- Auto erase operation
  - Automatically erases any combination of the blocks or the whole chip
  - Fast erase time: 20ms typical for single block erase and 50ms typical for chip erase and multi-block erase
- Auto page program operation
  - Automatically programs and verifies data at specified addresses
  - Internal address and data latches for 128 Bytes (64 Word) per page in each bank
  - Fast program time: 4ms typical for page program
- Built-in 128 Bytes/64 Words page buffer in each bank
  - Work as SRAM for temporary data storage
  - Fast access to temporary data
- Low power dissipation (typical values at 8MHz)
  - 40mA typical for Read While Write
  - 20mA typical for Read
  - 1uA typical for standby
- Hardware reset pin ($\overline{\text{RP}}$)
  - Reset internal state machine and put the device into standby mode
- Hardware write protect pin ($\overline{\text{WP}}$)
  - Allows protection of the first two 8K Byte blocks, regardless of their orginal protect status.
- Group Protection
  - Hardware method of locking groups to prevent any program or erase operation within that group
  - Any group can be locked in-system or via programming equipment
  - Temporary group unprotect feature allows code change in any previously locked group
- Erase Suspend/Erase Resume
  - Suspends or resumes erasing blocks to allow reading and programming in other blocks.
  - It is not necessary to do erase suspend if reading or programming blocks in the other bank
- Low Vcc write inhibit is equal to or less than 1.6V
- Compatible with JEDEC-standard pinouts
  - 48-pin TSOP (I)
  - 48-ball CSP

GENERAL DESCRIPTION

The MX29VW160T/B is a 16Mbit Flash memory organized as either 2M-byte by 8-bit or 1M-word by 16-bit. To provide simultaneous operation which can read a data while program/erase,the 16Mbits of data is divided into two banks of bank A (2M bit) and bank B(14M bit). Bank A is organized by eight 8K-byte blocks and three 64k-byte blocks. Bank B is organized by twenty-eight 64K-byte blocks.

To allow for simple in-system operation with very low operation voltage, MX29VW160T/B can be operated with a single 2.25V to 3.0V supply voltage.Manufactured with MXIC's advanced nonvolatile memory technology, the device offers access times of 120ns, and a low 1uA typical standby current.

The MX29VW160T/B command set is compatible with the JEDEC single-power-supply flash standard. Commands are written to the command register using standard micro-processor write timings. MXIC's flash memory augments EPROM functionality with an internal state machine which controls the erase and program circuitry. The device RY/$\overline{BY}$ pin provides a convenient way to monitor when a program or erase cycle is complete.

Programming the MX29VW160T/B is performed on a page basis; 128 bytes of data are loaded into the device and then programmed simultaneously.The typical Page Program time is 4ms. The device can also be reprogrammed in standard EPROM programmers. Reading data out of the device is similar to reading from an EPROM or other flash.

Erase is accomplished by executing the Erase command sequence. This will invoke the Auto Erase algorithm which is an internal algorithm that automatically times the erase pulse widths and verifies proper cell margin. This device features both chip erase and block erase. Each block can be erased and programmed without affecting other blocks. Using MXIC's advance design technology, no preprogram is required (internally or externally). As a result, the whole chip can be typically erased and verified in as fast as 50ms.

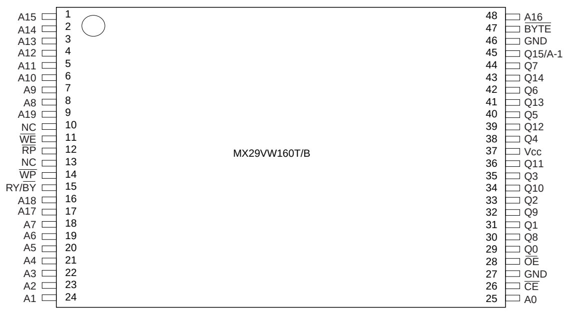
A combined feature of Reset Pin ($\overline{RP}$), a hardware lockout bit, and software command sequences provide complete data protection. First, software data protection protects the device from inadvertent program or erase. Two "unlock" write cycles must be presented to the device before the program or erase command can be accepted by the device. For hardware data protection, the $\overline{RP}$ pin provide protection against unwanted command writes due to invalid system bus condition that may occur during system reset and power up/down sequence. Finally, with a hardware lockout bit feature, the device provides complete core security for the kernal code required for system initialization.

MXIC's flash technology reliably stores memory contents after 100,000 erase and program cycles. The MXIC's cell is designed to optimize the erase and program mechanism. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produce reliable cycling.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to Vcc+1V.

PINOUT

48-PIN TSOP(I) 12mm x 20mm



PIN DESCRIPTION

SYMBOL	PIN NAME
A0 ~ A19	Address Input
Q0 ~ Q14	Data Input/ Output
Q15/A-1	Q15 (word mode)/LSB addr. (byte mode)
CE	Chip Enable Input
OE	Output Enable Input
WE	Write Enable
WP	Write Protect
RP	Reset/Deep Power-down
RY/BY	Ready/Busy Output
BYTE	Word/Byte Selection Input
Vcc	Power Supply Pin (2.25V ~ 3.0V)
GND	Ground Pin
NC	No Internal Connection Pin

48-Ball CSP 8mm x 13mm x 1.2mm(Ball Pitch = 0.8 mm), Top View, Balls Facing Up

	A	B	C	D	E	F	G	H
1	A3	A4	A2	A1	A0	CE	OE	GND
2	A7	A17	A6	A5	Q0	Q8	Q9	Q1
3	RY/BY	WP	A18	NC	Q2	Q10	Q11	Q3
4	WE	RP	NC	A19	Q5	Q12	Vcc	Q4
5	A9	A8	A10	A11	Q7	Q14	Q13	Q6
6	A13	A12	A14	A15	A16	BYTE	Q15/A-1	GND

Table 1 Block Architecture (Word Mode Addr. :A0~A19, BYTE Mode Addr.:A-1~A19)

Byte Mode	Word Mode				
1FFFFF~1FE000	FFFFF~FF000	8K-Byte Block	SA01	GA01	BANK A
1FDFFF~1FC000	FEFFF~FE000	8K-Byte Block	SA02	GA02	
1FBFFF~1FA000	FDFFF~FD000	8K-Byte Block	SA03	GA03	
1F9FFF~1F8000	FCFFF~FC000	8K-Byte Block	SA04	GA04	
1F7FFF~1F6000	FBFFF~FB000	8K-Byte Block	SA05	GA05	
1F5FFF~1F4000	FAFFF~FA000	8K-Byte Block	SA06	GA06	
1F3FFF~1F2000	F9FFF~F9000	8K-Byte Block	SA07	GA07	
1F1FFF~1F0000	F8FFF~F8000	8K-Byte Block	SA08	GA08	
1EFFFF~1E0000	F7FFF~F0000	64K-Byte Block	SA09	GA09	
1DFFFF~1D0000	EFFFF~F8000	64K-Byte Block	SA10		
1CFFFF~1C0000	E7FFF~E0000	64K-Byte Block	SA11		
1BFFFF~1B0000	DFFFF~D8000	64K-Byte Block	SA12	GA10	BANK B
1AFFFF~1A0000	D7FFF~D0000	64K-Byte Block	SA13		
19FFFF~190000	CFFFF~C8000	64K-Byte Block	SA14		
18FFFF~180000	C7FFF~C0000	64K-Byte Block	SA15		
17FFFF~170000	BFFFF~B8000	64K-Byte Block	SA16	GA11	
16FFFF~160000	B7FFF~B0000	64K-Byte Block	SA17		
15FFFF~150000	AFFFF~A8000	64K-Byte Block	SA18		
14FFFF~140000	A7FFF~A0000	64K-Byte Block	SA19		
13FFFF~130000	9FFFF~98000	64K-Byte Block	SA20	GA12	
12FFFF~120000	97FFF~90000	64K-Byte Block	SA21		
11FFFF~110000	8FFFF~88000	64K-Byte Block	SA22		
10FFFF~100000	87FFF~80000	64K-Byte Block	SA23		
0FFFFF~0F0000	7FFFF~78000	64K-Byte Block	SA24	GA13	
0EFFFF~0E0000	77FFF~70000	64K-Byte Block	SA25		
0DFFFF~0D0000	6FFFF~68000	64K-Byte Block	SA26		
0CFFFF~0C0000	67FFF~60000	64K-Byte Block	SA27		
0BFFFF~0B0000	5FFFF~58000	64K-Byte Block	SA28	GA14	
0AFFFF~0A0000	57FFF~50000	64K-Byte Block	SA29		
09FFFF~0E0000	4FFFF~48000	64K-Byte Block	SA30		
08FFFF~080000	47FFF~40000	64K-Byte Block	SA31		
07FFFF~070000	3FFFF~38000	64K-Byte Block	SA32	GA15	
06FFFF~060000	37FFF~30000	64K-Byte Block	SA33		
05FFFF~050000	2FFFF~28000	64K-Byte Block	SA34		
04FFFF~040000	27FFF~20000	64K-Byte Block	SA35		
03FFFF~030000	1FFFF~18000	64K-Byte Block	SA36	GA16	
02FFFF~020000	17FFF~10000	64K-Byte Block	SA37		
01FFFF~010000	0FFFF~08000	64K-Byte Block	SA38		
00FFFF~000000	07FFF~00000	64K-Byte Block	SA39	GA17	
A-1 TO A19	A0 TO A19				

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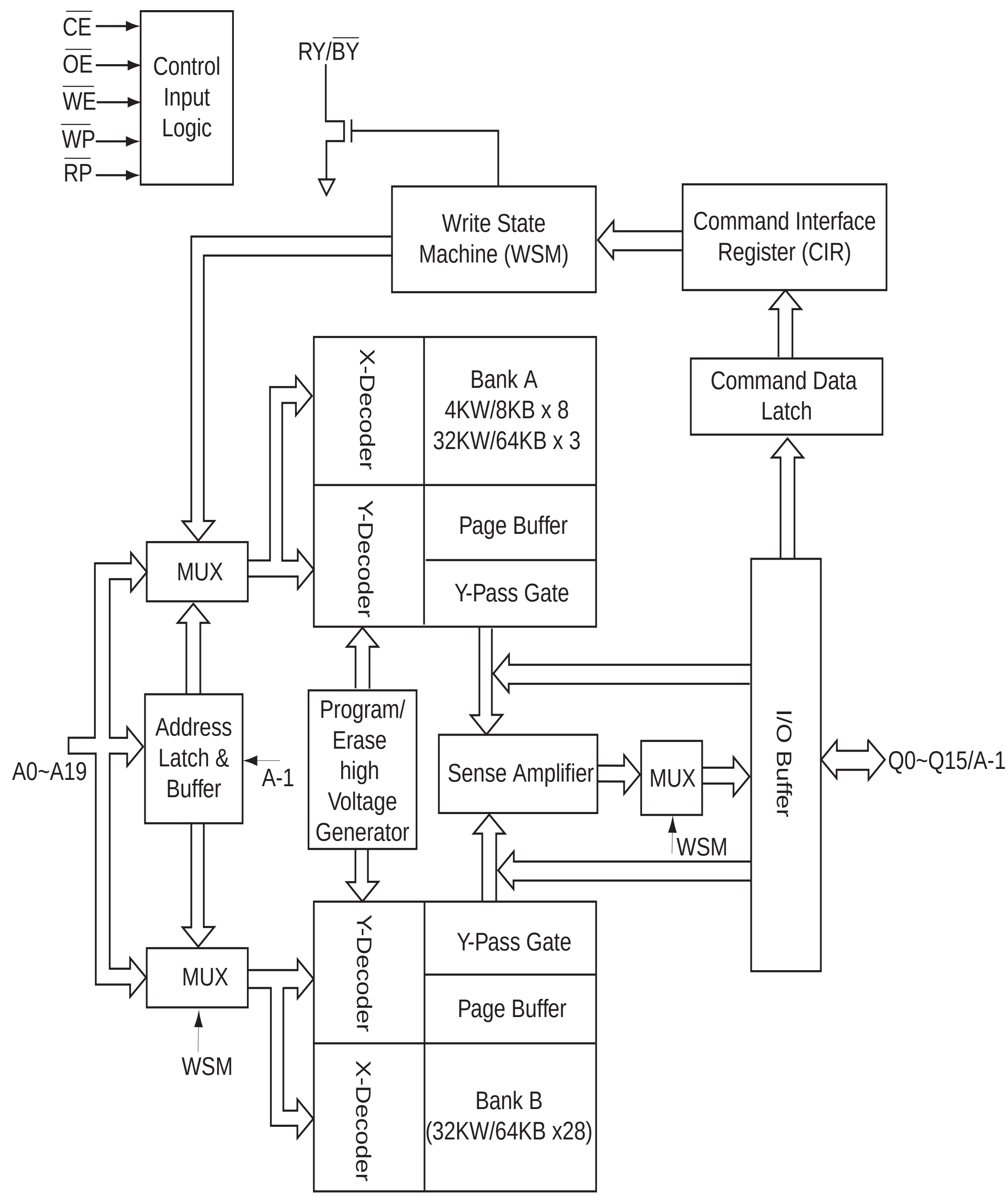
Byte Mode	Word Mode				
1FFFFF~1F0000	FFFFF~F8000	64K-Byte Block	SA01	GA01	BANK A
1EFFFF~1E0000	F7FFF~F0000	64K-Byte Block	SA02	GA02	
1DFFFF~1D0000	EFFFF~E8000	64K-Byte Block	SA03		
1CFFFF~1C0000	E7FFF~E0000	64K-Byte Block	SA04		
1BFFFF~1B0000	DFFFF~D8000	64K-Byte Block	SA05	GA03	
1AFFFF~1A0000	D7FFF~D0000	64K-Byte Block	SA06		
19FFFF~190000	CFFFF~C8000	64K-Byte Block	SA07		
18FFFF~180000	C7FFF~C0000	64K-Byte Block	SA08		
17FFFF~170000	BFFFF~B8000	64K-Byte Block	SA09	GA04	
16FFFF~160000	B7FFF~B0000	64K-Byte Block	SA10		
15FFFF~150000	AFFFF~A8000	64K-Byte Block	SA11		
14FFFF~140000	A7FFF~A0000	64K-Byte Block	SA12		
13FFFF~130000	9FFFF~98000	64K-Byte Block	SA13	GA05	
12FFFF~120000	97FFF~90000	64K-Byte Block	SA14		
11FFFF~110000	8FFFF~88000	64K-Byte Block	SA15		
10FFFF~100000	87FFF~80000	64K-Byte Block	SA16		
0FFFFF~0F0000	7FFFF~78000	64K-Byte Block	SA17	GA06	
0EFFFF~0E0000	77FFF~70000	64K-Byte Block	SA18		
0DFFFF~0D0000	6FFFF~68000	64K-Byte Block	SA19		
0CFFFF~0C0000	67FFF~60000	64K-Byte Block	SA20		
0BFFFF~0B0000	5FFFF~58000	64K-Byte Block	SA21	GA07	
0AFFFF~0A0000	57FFF~50000	64K-Byte Block	SA22		
09FFFF~090000	4FFFF~48000	64K-Byte Block	SA23		
08FFFF~080000	47FFF~40000	64K-Byte Block	SA24		
07FFFF~070000	3FFFF~38000	64K-Byte Block	SA25	GA08	
06FFFF~060000	37FFF~30000	64K-Byte Block	SA26		
05FFFF~050000	2FFFF~28000	64K-Byte Block	SA27		
04FFFF~040000	27FFF~20000	64K-Byte Block	SA28		
03FFFF~030000	1FFFF~18000	64K-Byte Block	SA29	GA09	BANK B
02FFFF~020000	17FFF~10000	64K-Byte Block	SA30		
01FFFF~010000	0FFFF~08000	64K-Byte Block	SA31		
00FFFF~00E000	07FFF~07000	8K-Byte Block	SA32	GA10	
00DFFF~00C000	06FFF~06000	8K-Byte Block	SA33	GA11	
00BFFF~00A000	05FFF~05000	8K-Byte Block	SA34	GA12	
009FFF~008000	04FFF~04000	8K-Byte Block	SA35	GA13	
007FFF~006000	03FFF~03000	8K-Byte Block	SA36	GA14	
005FFF~004000	02FFF~02000	8K-Byte Block	SA37	GA15	
003FFF~002000	01FFF~01000	8K-Byte Block	SA38	GA16	
001FFF~000000	00FFF~00000	8K-Byte Block	SA39	GA17	
A-1 TO A19	A0 TO A19				

MX29VW160B

Block Diagram



BUS OPERATIONS

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. These bus operations are summarized below.

Table 2.1 MX29VW160T/B Bus Operations for Byte-Wide Mode ($\overline{Byte}$ = VIL)

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RP}$	$\overline{WP}$	A0	A1	A6	A9	Q0~Q7	Q8~Q14	Q15/A-1	Notes
Read	L	L	H	H	L/H	A0	A1	A6	A9	DOUT	HighZ	A-1	1,2,7,9
Output Disable	L	H	H	H	X	X	X	X	X	HighZ	HighZ	X	1,6,7
Standby	H	X	X	H	X	X	X	X	X	HighZ	HighZ	X	1,6,7
Hardware Standby	X	X	X	L	X	X	X	X	X	HighZ	HighZ	X	1,3
Manufacturer ID	L	L	H	H	L/H	L	L	X	VID	C2H	HighZ	X	4,8
Device ID	L	L	H	H	L/H	H	L	X	VID	67/68H	HighZ	X	4,8
Block Protect Verify *	L	L	H	H	H	L	H	X	VID	C2H	HighZ	X	
Write	L	H	L	H	L/H/VID	A0	A1	A6	A9	DIN	High Z	A-1	1,5,6,10

Table 2.2 MX29VW160T/B Bus Operations for Word-Wide Mode ($\overline{Byte}$ = VIH)

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RP}$	$\overline{WP}$	A0	A1	A6	A9	Q0~Q7	Q8~Q14	Q15/A-1	Notes
Read	L	L	H	H	L/H	A0	A1	A6	A9	DOUT	DOUT	DOUT	1,2,7
Output Disable	L	H	H	H	X	X	X	X	X	HighZ	HighZ	HighZ	1,6,7
Standby	H	X	X	H	X	X	X	X	X	HighZ	HighZ	HighZ	1,6,7
Hardware Standby	X	X	X	L	X	X	X	X	X	HighZ	HighZ	HighZ	1,3
Manufacturer ID	L	L	H	H	L/H	L	L	X	VID	C2H	00H	0B	4,8
Device ID	L	L	H	H	L/H	H	L	X	VID	67/68H	00H	0B	4,8
Block Protect Verify *	L	L	H	H	H	L	H	X	VID	C2H	00H	0B	
Write	L	H	L	H	L/H/VID	A0	A1	A6	A9	DIN	DIN	DIN	1,5,6,10

* : Valid Sector Address must be provided when doing block protect Verify mode.
Legend : L = Logic Low = VIL, H = Logic High = VIH ,X = VIL or VIH, VID = 8.5~10.5V ,Refer to DC Characteristics for Voltage loads.

Notes:
1. X can be VIH or VIL for address or control pins except for RY/$\overline{BY}$ which is either VOL or VOH.
2. RY/$\overline{BY}$ output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode, RY/$\overline{BY}$ will be at VOH, if it is tied to Vcc through a 1K ~ 100K resistor. When the RY/$\overline{BY}$ at VOH is independent of $\overline{OE}$ while a WSM operation is in progress.
3. $\overline{RP}$< GND+0.2V ensures the lowest consumption current.
4. A0 and A1 at VIL provide manufacturer ID code. A0 at VIH and A1 at VIL provide ID code. A0 at VIL, A1 at VIH and with appropriate block address provide Block Protect Code.(Refer to Table 4)
5.Command or different Erase operations, Data program operations or Group protect operation can only be successfully completed through proper command sequence.
6. RY/$\overline{BY}$ goes to VOH when the WSM is not busy or in erase suspend mode.
7.RY/$\overline{BY}$ may be at VOL while the WSM is busy performing various operations.
8.VID = 8.5V-10.5V
9. Q15/A-1 = VIL, Q0-Q7 = D0-D7 out. Q15/A-1 = VIH, Q0-Q7 = D8-D15 out.
10. When $\overline{WP}$=VIL, the two outer most 8K-Byte blocks be protected.
When $\overline{WP}$=VIH, all blocks remain orginal protect status.
When $\overline{WP}$=VID, all blocks be unprotected.

COMMAND DEFINITIONS

Table 3 Command Definitions

			Bus Cycles											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read		1	RA	RD										
Reset		1	XXXH	F0H										
Manufacturer ID	Word	4	555H	AAH	2AAH	55H	555H	90H	X00H	00C2H				
	Byte		AAAH		555H		AAAH		X00H	C2H				
Device ID	Word	4	555H	AAH	2AAH	55H	555H	90H	X01H	0067H/0068H*				
	Byte		AAAH		555H		AAAH		X02H	67H/68H*				
Block Protect Verify	Word	4	555H	AAH	2AAH	55H	555H	90H	X02H	XX01H/XX00H*				
	Byte		AAAH		555H		AAAH		X04H	01H/00H*				
Group Protect	Word	6	555H	AAH	2AAH	55H	555H	60H	555H	AAH	2AAH	55H	GA	20H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Group Unprotect	Word	6	555H	AAH	2AAH	55H	555H	60H	555H	AAH	2AAH	55H	555H	40H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Page/Byte Program	Word		555H	AAH	2AAH	55H	555H	A0H	PA	PD				
	Byte		AAAH		555H		AAAH							
Single Block Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	20H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Multi Block Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Erase Suspend		1	XXXH	B0H										
Erase Resume		1	XXXH	30H										

Notes:

1. *00H Represents unprotect block & *01H represents protect block in the 4th Bus cycle data of "Block Protect Verify".
2. Address bit A11-A19 = X = "Don't care" for all address commands except for Program Address (PA) and Block Address (SA). 555H and 2AAH address command codes stand for Hex number starting from A0 to A10 in word mode and A-1 to A10 in byte mode.
3. Bus operations are defined in Table 2.
4. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Address are located on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the block to be erase. The combination of A12-A19 will select any block(Refer to Table 1).
   GA = Group address to be protect. The combination of A12-A19 will select any group.
5. RD = Data read from location RA during read operation.
   PD = Data to be Programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
6. Only Q0-Q7 command data is taken, Q8 to Q15 = Don't care.
   *Refer to Table 4.

FUNCTIONAL DESCRIPTION

SIMULTANEOUS OPERATION

The MX29VW160T/B provides the simultaneous read/ write function. The device is capable of reading data from one bank and simultaneously erasing (so as, programming, erase-suspend reading, and erase suspend programming) data from the other bank. The bank selection can be selected by bank address (A16 to A19) with zero latency.

The MX29VW160T/B contains two data banks which are bank A (8K-Byte x 8, 64K-Byte x 3) and Bank B (64K-Byte x 28). Following table describes the detail simultaneous operation.

Simultaneous Operation Table

Bank-A \ Bank-B	standby	Read mode	Single block erase	Multiple block erase (only 1 bank)	Multiple block erase (2 banks)	Chip erase	Erase suspend	Erase resume	Page program	Group protect/ unprotect	Silicon ID read
Standby	O	-	-	-	-	-	-	-	-	-	-
Read mode	-	X	O	O	X	-	O	O	O	X	-
Single block erase	-	O	-	-	-	-	-	-	X	X	-
Multiple block erase (only 1 bank)	-	O	-	-	-	-	-	-	X	-	-
Multiple block erase (2 banks)	-	X	-	-	O	-	O	O	X	X	-
Chip erase	-	-	-	-	-	O	-	-	-	-	-
Erase suspend	-	O	-	-	O	-	-	-	-	X	O
Erase resume	-	O	-	-	O	-	-	-	-	X	-
Page program	-	O	X	X	X	-	-	-	-	X	-
Group protect/ unprotect	-	X	X	-	X	-	X	X	X	-	-
Silicon ID read	-	-	-	-	-	-	O	-	-	-	-

Legend : "o"=Okay,"X"= Not allow, "-"= Not available.

READ ARRAY MODE

The MX29VW160T/B must satisfy two control functions to obtain data output. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.(Figure 11)

Address access time (tACC) is equal to the delay from stable addresses to valid output data. The chip enable access time (tCE) is the delay from state the falling edge of $\overline{CE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least tACC - tCE time.) When reading out a data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from "H" to "L".

READ/RESET COMMAND

The Read or Reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enable for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms (Figure 12) for the specific timing parameters.

READ ID MODE

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29VW160T/B contains a Silicon-ID-Read Operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Read Silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL, A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of 67H for MX29VW160T, 68H for MX29VW160B.

The Silicon-ID-Read Operation also covers the block protection verification. A read cycle with A1=VIH, A0= "Don't care" returns data of 00H for"unprotected block" and 01H for "protected block".

Table 4.1 Read ID Mode Table

TYPE			A12 to A19	A6	A1	A0	A-1	Code (HEX)
Manufacturer ID			X	X	L	L	X	C2H
Device ID	MX29VW160T	Byte	X	X	L	H	X	67H
		Word					X	0067H
	MX29VW160B	Byte	X	X	L	H	X	68H
		Word					X	0068H
Block Protection Verify			Block Address	X	H	X	X	01H/00H*

*01H for "protected block" addresses and 00H for "unprotected block" addresses.

Table 4.2 Extended Read ID Mode Table

TYPE			Code (HEX)	Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Manufacturer's ID			C2H	A-1/0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0
Device ID	MX29VW160T	Byte	67H	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	1	1	0	0	1	1	1
		Word	0067H	0	0	1	0	0	0	1	0	0	1	1	0	0	1	1	1
	MX29VW160B	Byte	68H	A-1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	1	1	0	1	0	0	0
		Word	0068H	0	0	1	0	0	0	1	0	0	1	1	0	1	0	0	0
Block Protection Verify			01H/00H**	A-1/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1/0

Notes:

* Manufacture Code = C2 H, Device Code = 67H/68H when $\overline{BYTE}$ = VIL
Manufacture Code = 00C2H,Device Code =0067H/0068H when BYTE = VIH

** Outputs 01H at protected block address ,00H at unprotected block address.

PROGRAM MODE

PAGE PROGRAM

The MX29VW160T/B is page programmable with one 128-Byte/ 64-Word page buffer in each bank. To initiate Page program mode, a three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the page program command A0H. Any attempt to write to the device without the three-cycle command sequence will not start the internal Write State Machine (WSM), no data will be written to the device.

After three-cycle command sequence is given, a Byte/ Word load is performed by applying a low pulse on the WE or CE input with CE or WE low (respectively) and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE. Maximum of 128-Byte/ 64-Word of data may be loaded into each page. Data loading activity is terminated by issuing same address load twice.

BYTE-WIDE LOAD/WORD-WIDE LOAD

Byte (Word) loads are used to enter the 128 bytes (64 words) of a page to be programmed or the software codes for data protection. A byte load (word load) is performed by applying a low pulse on the WE or CE input with CE or WE low respectively, and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE.

Either byte-wide load or word-wide load is determined (Byte = VIL or VIH is latched) on the falling edge of the WE (or CE) during the 3rd command write cycle.

AUTOMATIC PROGRAM ALGORITHM

Any page to be programmed should have the page in the erased state first, i.e. performing block erase is suggested before page programming can be performed.

The device is programmed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be still in the erased state (i.e. FFH). Once the bytes of the page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. A6 to A19 specify the page address, i.e., the device is page-aligned on 128-byte boundary. The page addresses must be valid (Page Address A6-A19 is latched at the 4th bus write-cycle)during each high to low transition of WE or CE. A-1 to A5 specify the byte address during the page. The byte may be loaded in any order; sequential loading is not required. The load period will also end if the same address is consecutively loaded twice. For the last two same address, the first address and data will be treated as normal data to be programmed. The second one must keep the same address and data as the first one.

The status of program cycle can be determined by checking the Q7 (Data Polling), Q6 (Toggle Bit), or RY/ BY.

The automatic programming operation is completed when Q6 stops toggling (See Table 5 of Hardware Sequence Flags.)

WRITE OPERATION STATUS

Detailed in Table 5 are all the status flags that can determine the status of the bank for the current mode operation. The read operation from the bank where is not operating Automatic algorithm returns a data of memory cell. These bits offer a method for determining whether a Automatic Algorithm is completed properly. The information on Q2 is address sensitive. This means that if an address from an erasing block is consecutively read, then the Q2 bit will toggle. However, Q2 will not toggle if an address from a non-erasing block is consecutively read. This allows the user to determine which blocks are erasing and which are not.

The status flag is not output from bank (non-busy bank) not executing Automatic Algorithm. For example, there is bank (busy bank) which is now executing Automatic Algorithm. When the read sequence is (a)"busy bank" (b)"non-busy bank" and (c)"busy bank" the Q6 is toggling in the case (a) and (c). In case of (b), the data of memory cell is output. In the erase-suspend read mode with the same read sequence, Q6 will not be toggled in the (a), and (c).

In the erase suspend read mode, Q2 is toggled in the (a) and (c). In case of (b), the data of memory cell is output.

Table 5. Hardware Sequence Flags Table

Status			Q7	Q6	Q5	Q3	Q2	RY/$\overline{BY}$
In Progress	Automatic Program Algorithm		$\overline{Q7}$	Toggle	0	N/A	No Toggle	0
	Automatic Erase Algorithm		0	Toggle	0	1	Toggle*	0
	Erase Suspend Mode	Erase Suspend Read (Erase-Suspend Block)	1	No Toggle	0	N/A	Toggle	1
		Erase Suspend Read (Non-Erase-Suspend Block)	Data	Data	Data	Data	Data	1
		Erase Suspend Program (Non-Erase-Suspend Block)	$\overline{Q7}$	Toggle	0	N/A	N/A	0
Exceeded Time Limits	Automatic Program Algorithm		$\overline{Q7}$	Toggle	1	0	1	0
	Automatic Erase Algorithm		0	Toggle	1	1	N/A	0
	Erase Suspend Mode	Erase Suspend Program (Non-Erase-Suspend Block)	$\overline{Q7}$	Toggle	1	0	N/A	0

*. Successive reads from the erasing or erase-suspend block will cause Q2 to toggle. Reading from non-erase suspend block address will indicate logic "1" at the Q2 bit.

ERASE MODE

AUTOMATIC CHIP ERASE

The MX29VW160T/B does not require pre-program operation prior to erase operation. Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command (80H). Two more "unlock" write cycles are then followed by the Chip Erase command (10H).

The system can determine the status of the erase operation by using Q7 ($\overline{Data}$ Polling), Q6 (Toggle Bit), or RY/$\overline{BY}$. The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on Q7 is (See Write Operation Status section.) at which time the device returns to read the mode.

AUTOMATIC BLOCK ERASE

The MX29VW160T/B does not require pre-program operation prior to erase operation. Block erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command (80H). Two more "unlock" write cycles are then followed by the Block Erase command (20H for single-block erase, 30H for multi-block erase). The system is not required to provide any controls or timings during these operations. When erasing a block or blocks the remaining un-selected blocks are not affected. The block address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever happens later, while the command (data) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever happens first. After issue same address (A12-A19) twice ,the device will stop block address loading and start erase operation when at multi-block erase mode.

Before issued the same address twice to the device, any command other than Erase Suspend (B0H) or multi block Erase (30H) will reset the device to read mode and ignore the previous command string.

The system can determine the status of the erase operation by using Q7 ($\overline{Data}$ Polling), Q6 (Toggle Bit), or RY/$\overline{BY}$.

ERASE SUSPEND AND RESUME

The Erase Suspend command ,B0H allows the user to interrupt a Block Erase operation and then perform data reads from or program to a block not being erased. .This command is applicable ONLY during the Block Erase operation. The Erase Suspend command will be ignored if written during the Chip Erase operation or Auto Program Algorithm.

Writing the Erase Suspend command (B0H) during the multiple block erase operation (before issue same address twice to terminate the block address loading and to start the erase operation) results immediate termination of the address loading and suspension of the erase operation.

Writing the Erase Resume command (30H) resumes the erase operation.

When the Erase Suspend command is written during the Block Erase operation, the device will take a maximum of 300us to suspend the erase operation. When the devices have entered the erase suspended mode, the RY/$\overline{BY}$ output pin will be at HighZ . The user must use the Q6 (or RY/$\overline{BY}$ pin) to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

To resume the operation of Block Erase, the Resume command (30H) should be written . Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

STANDBY MODE

MX29VW160T/B can be set into Standby mode with two different approaches. One is using both $\overline{CE}$ and $\overline{RP}$ pins and the other one is using $\overline{RP}$ pin only.

When using both pins of $\overline{CE}$ and $\overline{RP}$, a CMOS Standby mode is achieved with both pins held at Vcc ± 0.3V. Under this condition, the current consumed is less than 1uA (typ.). During Auto Algorithm operation, Vcc active current (Icc2) is required even $\overline{CE}$ = "H". The device can be read with standard access time (tCE) from either of these standby modes.

When using only RP, a CMOS standby mode is achieved with RP input held at Vss ± 0.3V Under this condition the current is consumed less than 1uA (typ.). Once the RP pin is taken high,the device is back to active without recovery delay.

In the standby mode the outputs are in the high impedance state, independent of the OE input.

AUTOMATIC STANDBY MODE

MX29VW160T/B is capable to provide the Automatic Standby Mode to restrain power consumption during read-out of data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To active this mode, MX29VW160T/B automatically switch themselves to low power mode when MX29VW160T/B addresses remain stable during access time of 250ns. It is not necessary to control CE, WE, and OE on the mode. Under the mode, the current consumed is typically 1uA (CMOS level).

During Simultaneous operation, Vcc active current (Icc2) is required.Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically and MX29VW160T/B read-out the data for changed addresses.

OUTPUT DISABLE

With the OE input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

DATA PROTECTION

The MX29VW160T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read Array mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power-up and power-down transitions or system noise.

TEMPORARY GROUP UNPROTECT

This feature allows temoprary unprotection of previously protected group to change data in-system. The Temporary Group Unprotect mode is activated by setting the RP pin to VID(8.5V-10.5V). During this mode, formerly protected groups can be programmed or erased as unprotected group. Once VID is remove from the RP pin,all the previously protected group are protected again.Figure 1 shows the algorithm, for this feature.

GROUP PROTECTION

To activate this mode,a six-bus cycle operation is required. there are two "unlock" write cycle. There are followed by writing the setup command.Two more "unlock" write cycles are then followed by the lock group command-20H. Group address(A12~A19) is latched on the falling edge of CE or WE of the sixth cycle of the command sequence. The automatic Lock operation begins on the rising edge of the last WE pulse in the command sequence and terminates when the Q6 stops toggling(or RY/BY =1) at which time the device stays at the read array mode.

The devcie remains enabled for read array mode until the CIR contents are altered by a valid command sequence (Refer to the table 3).

GROUP UNPROTECT

It is also possible to unprotect all groups,same as the first five write command cycle in activating group protection mode followed by the unprotect group command -40H, the automatic unprotect operation begins on the rising edge of the last WE pulse in the command sequence and terminates when the Q6 stops toggling (or RY/BY =1) at with time the device stays at the read array mode.(Refer to table 3).Note that all groups are unprotected after group unprotection completed.

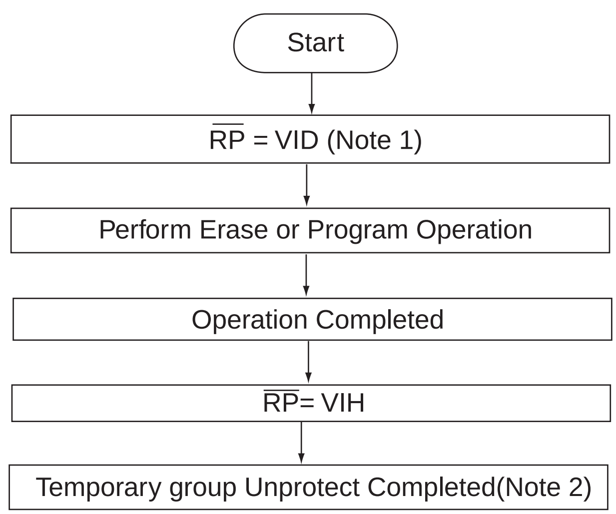
The device remains enable for read array mode until the CIR content are altered by a valid command sequence.

$\overline{WP}$ / $\overline{RP}$	VIL	VIH	VID
VIL	Hardware Standby	The two outer most 8K-Byte be protected, all other blocks remains at original protect status.	The two outer most 8K-Byte blocks be protected, all other blocks be unprotected.
VIH	Hardware Standby	All blocks remain at origined protect status.	All blocks be unprotected.
VID	Hardware Standby	All blocks be unprotected.	All blocks be unprotected.

VERIFY BLOCK PROTECT

To verify Protect status of the block,operation is initiated by writing Silicon ID read command into the command register. Following the command write ,a read cycle from address XXX2H(A1=VIH) and Group Address (A15~A19) returns data of 00H for " unprotected block". A read cycle from XXX2H(A1=VIH) and group address (A15~A19) returns data of 01H for "protected block".

Figure 1 Temporary Block Unprotect Operation



Note : 1. All protected groups are temporary unprotected. VID=8.5V~10.5V
2. All previously protected groups are protected again.

Figure 2 Group Protection Algorithm (Word Mode)

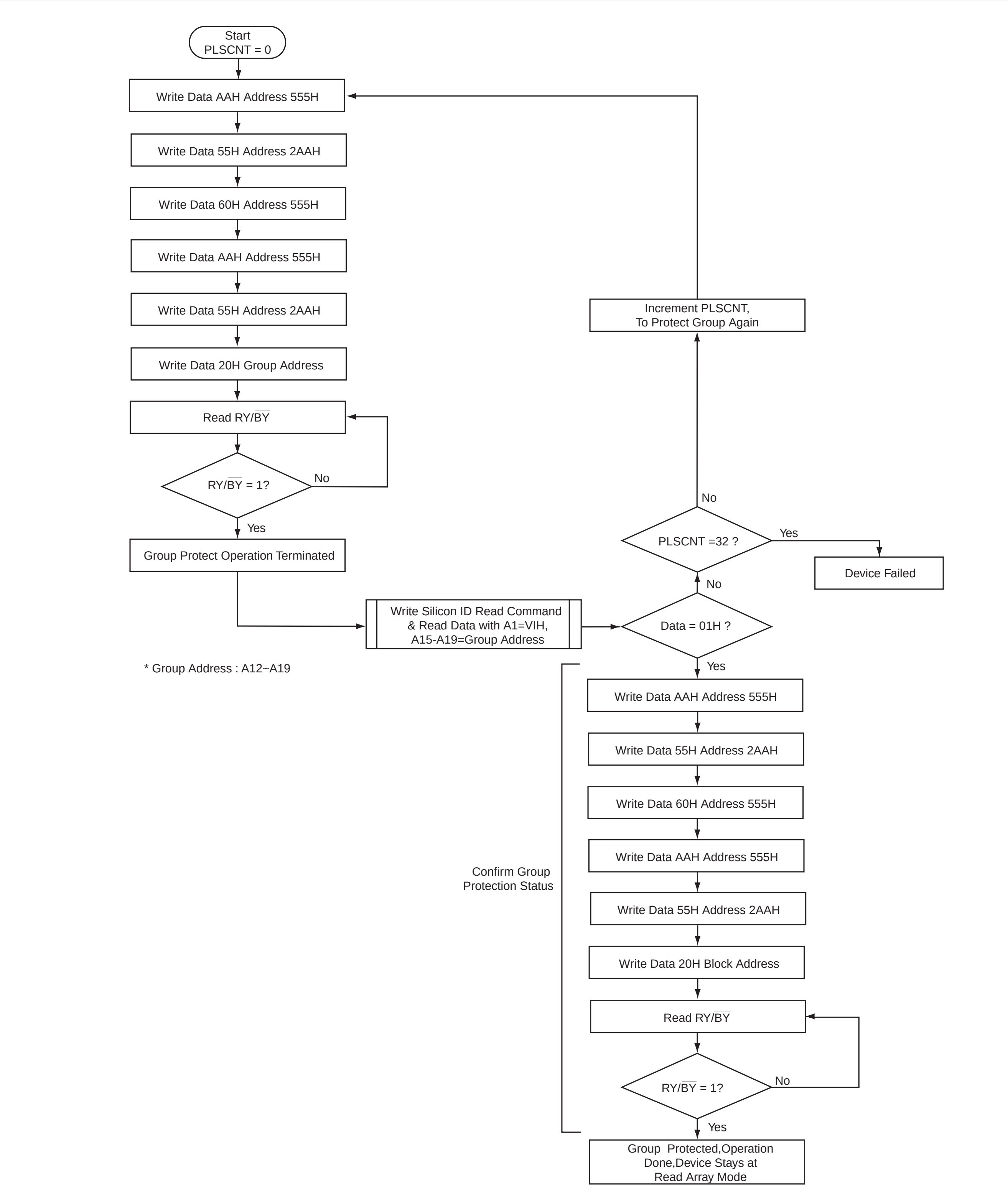
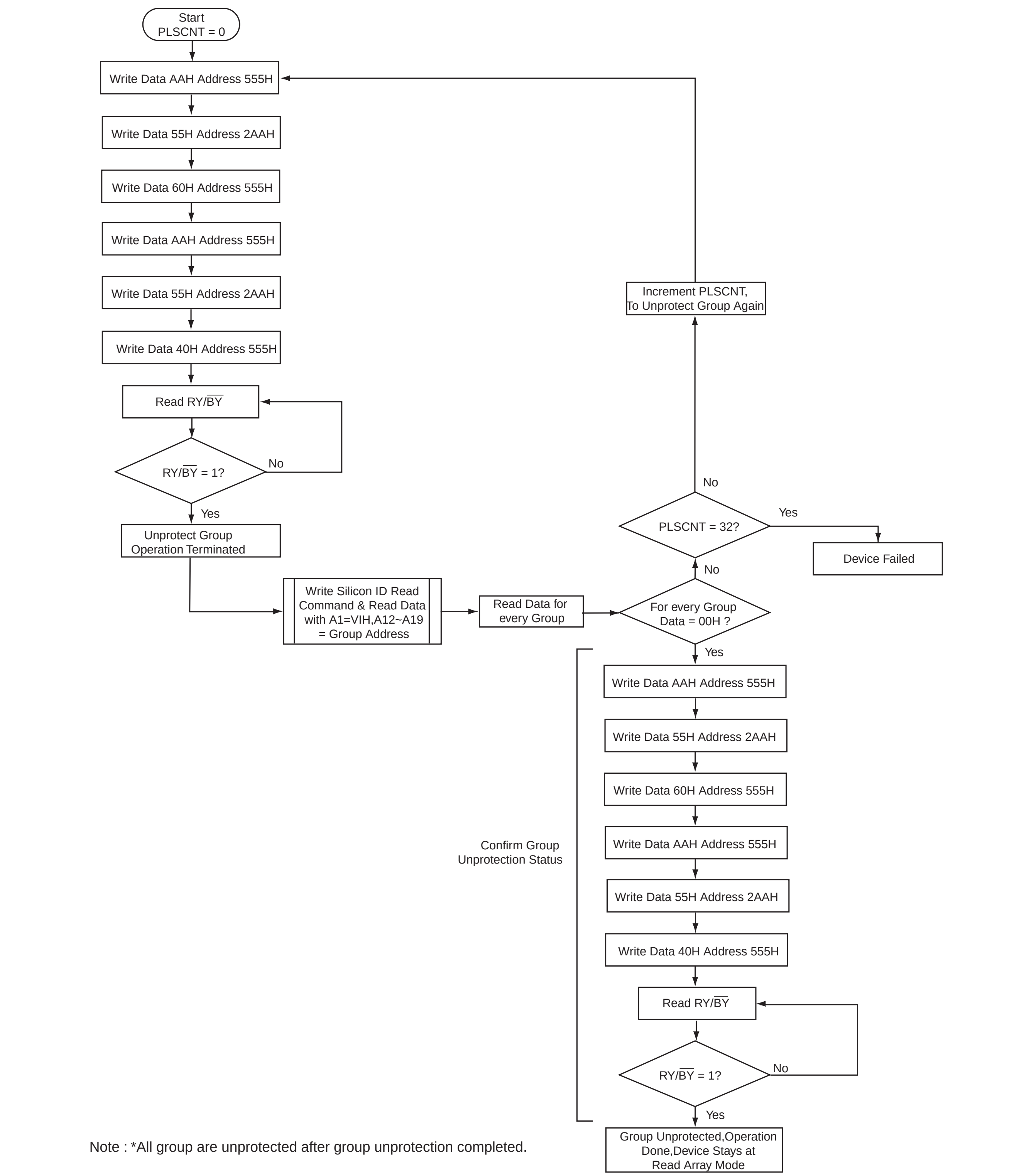


Figure 3 Group Unprotection Algorithm (Word Mode)



Note : *All group are unprotected after group unprotection completed.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typ.) on $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGIC INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH, or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical "0" while $\overline{OE}$ is a logical "1".

POWER-UP SEQUENCE

The MX29VW160T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its Vcc and GND.

Q7: $\overline{Data}$ Polling

The MX29VW160T/B features $\overline{Data}$ Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program algorithm an attempt to read the device will produce the true data last written to Q7. The $\overline{Data}$ Polling feature is valid after terminating load operation for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1" The $\overline{Data}$ Polling feature is valid after the rising edge of the sixth $\overline{WE}$ pulse of six write pulse sequences for automatic chip/block erase.

The $\overline{Data}$ Polling feature is active during Automatic Program/Erase algorithm (see section Q3 Block Erase Status Bit).

RY/$\overline{BY}$: Ready/$\overline{Busy}$

The RY/$\overline{BY}$ is a dedicated, open-drain output pin that indicates whether an Automatic Erase/Program algorithm is in progress or complete. The RY/$\overline{BY}$ status is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence. Since RY/$\overline{BY}$ is an open-drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to Vcc.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 5 shows the outputs for RY/$\overline{BY}$.

Q6: Toggle Bit I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence (prior to the program or erase operation), and during the block erase time-out period.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all blocks selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected blocks are protected, the Automatic Erase algorithm erases the un-protected blocks, and ignores the selected blocks that are protected.

The system can use Q6 and Q2 together to determine whether a block is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which blocks are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected block, Q6 toggles for approximately 1us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 5 shows the outputs for Toggle Bit I on Q6.

Q2: Toggle Bit II

The Toggle Bit II on Q2, when used with Q6, indicates whether a particular block is actively erasing (that is the Automatic Erase algorithm is in process), or whether that block is erase-suspended. Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence.

Q2 toggles when the system reads at addresses within those blocks that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) But Q2 cannot distinguish whether the block is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing or is erase-suspended, but cannot distinguish which blocks are selected for erasure. Thus, both status bits are required for blocks and mode information. Refer to table 5 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/Q2

Whenever the system initially begins reading toggle bit status, it must read Q7~Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7~Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5: Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1" This is a time-out condition which indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during block erase operation, it is specifiesd that a particular block is bad and it may not be reused. However, other blocks are still functional and may be used for program or erase operation. The device must be reset to use other blocks. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active blocks in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of blocks are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire block containing that byte is bad and this block may not be reused. (Other blocks are still functional and can be reused.)

The Q5 time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the device has exceeded timing limits, the Q5 bit will indicate a logical "1" Please note that this is not a device failure condition since the device was incorrectly used.

Q3: Block Erase Status Bit

The MX29VW160T/B provides three difference erase operation :(1) chip erase. (2) single block erase,and (3) mutil-block erase. The device will automatically start erase operation after erase command completed when doing (1) and (2). For the case of (3), toggling the same address (A12 to A19) twice is necessary to terminate the block address loading and start the erase operation . No extra time-out is needed to terminate the block address loading or complete the erase operation .

During the period of issuing the erase command,Q3 will remain low until the erase operation starts.$\overline{\text{Data}}$ polling and Toggle Bit are valid after the initial block erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the block address loading window is still open. If Q3 is high (logical "1" the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If Q3 is low (logical "0", the device will be accept additional block erase command. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent block erase command. If Q3 were high on the second status check, the command may not have been accepted.Note that during the block address loading period,any command other than Multiple Block Erase (30H) or Erase Suspend (B0H) will reset the device to read array mode.

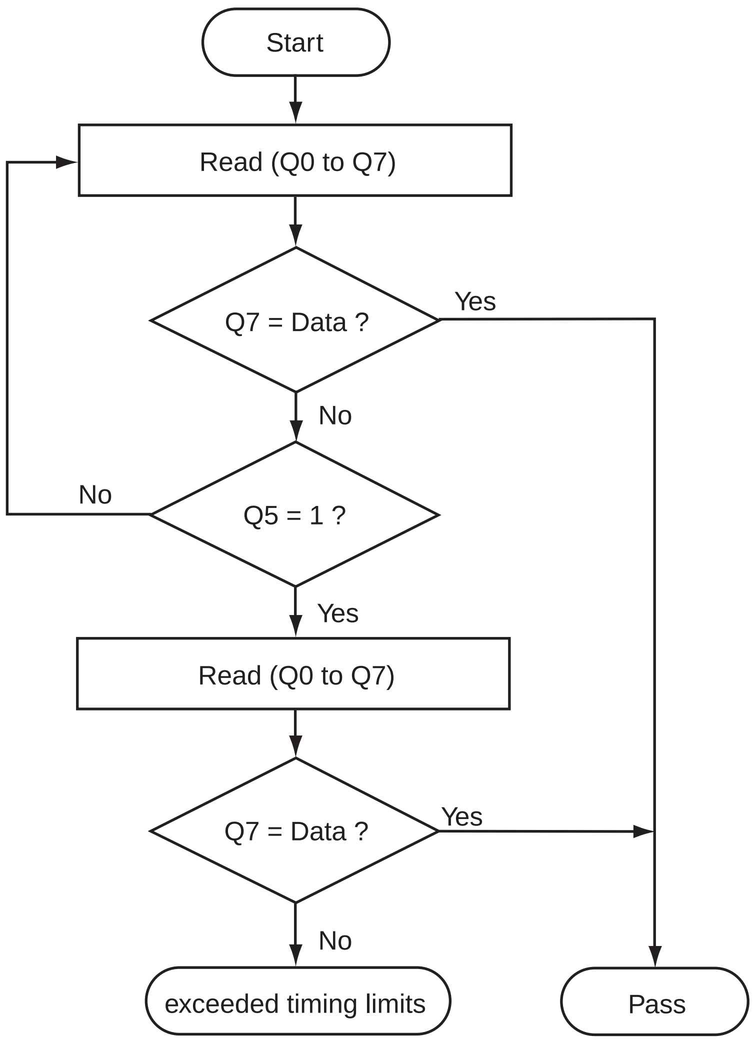
$\overline{\text{WP}}$: Write Protect Pin

When system provides VIL to the $\overline{\text{WP}}$ pin, the two outer most 8K-Byte blocks (SA01 and SA02 of MX29VW160T or SA38 and SA39 of MX29VW160B) will be protected from program and erase operations.

When $\overline{\text{WP}}$=VIH, the two outer most 8K-Byte blocks and all other blocks will remain at (or back to) their original protect status.

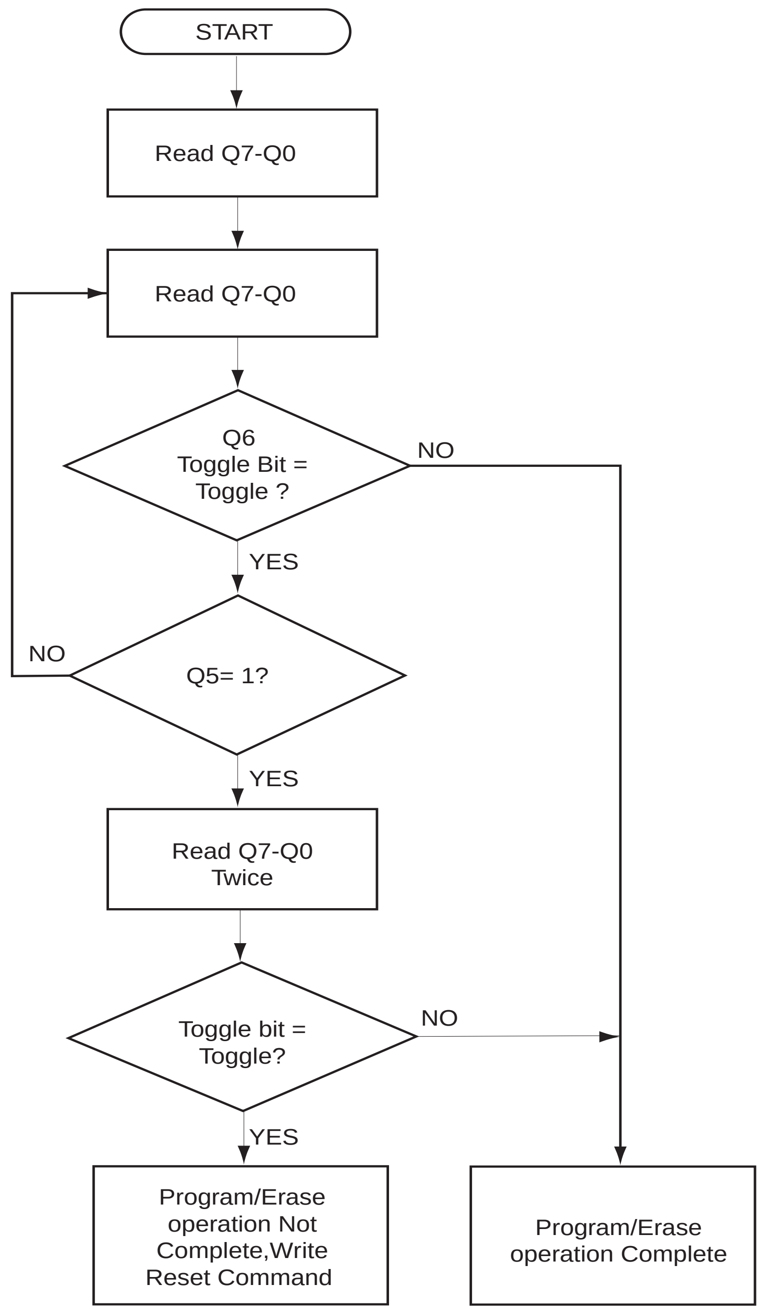
When $\overline{\text{WP}}$=VID, the whole device will be unprotected.

Figure 4 $\overline{\text{Data}}$ Polling Algorithm



NOTE : Q7 is rechecked even if Q5 = "1" because Q7 may change simultaneously with Q5.

Figure 5 Toggle Bit Algorithm



Note:The system should recheck the toggle bit even if Q5="1" because the toggle bit may stop toggling as Q5 changes to "1".See the subsections on Q6 and Q2 for more information.

Figure 6 Automatic Erase Algorithm (Word Mode)

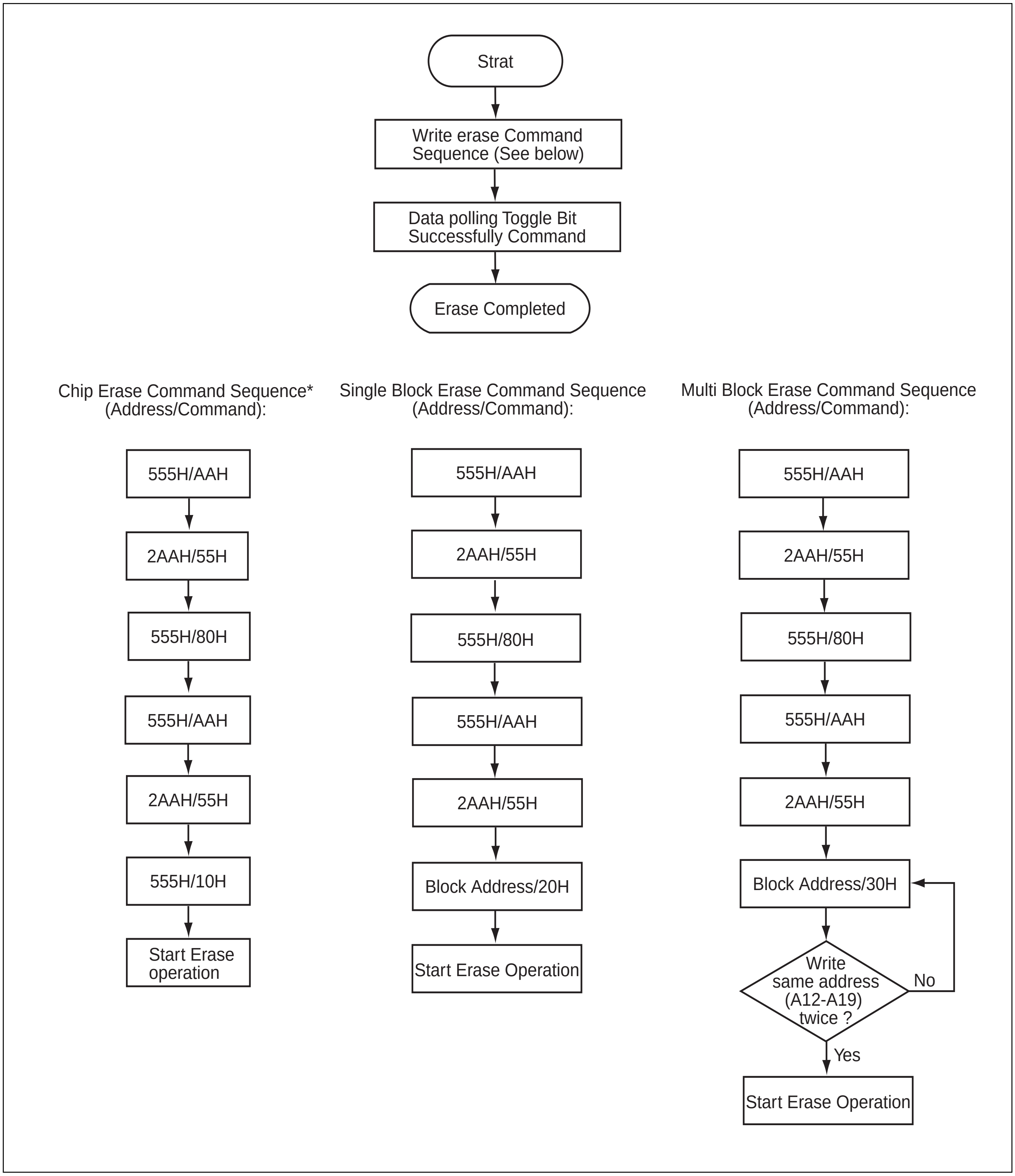


Figure 7 Automatic Page Program Flow Chart (Word Mode)

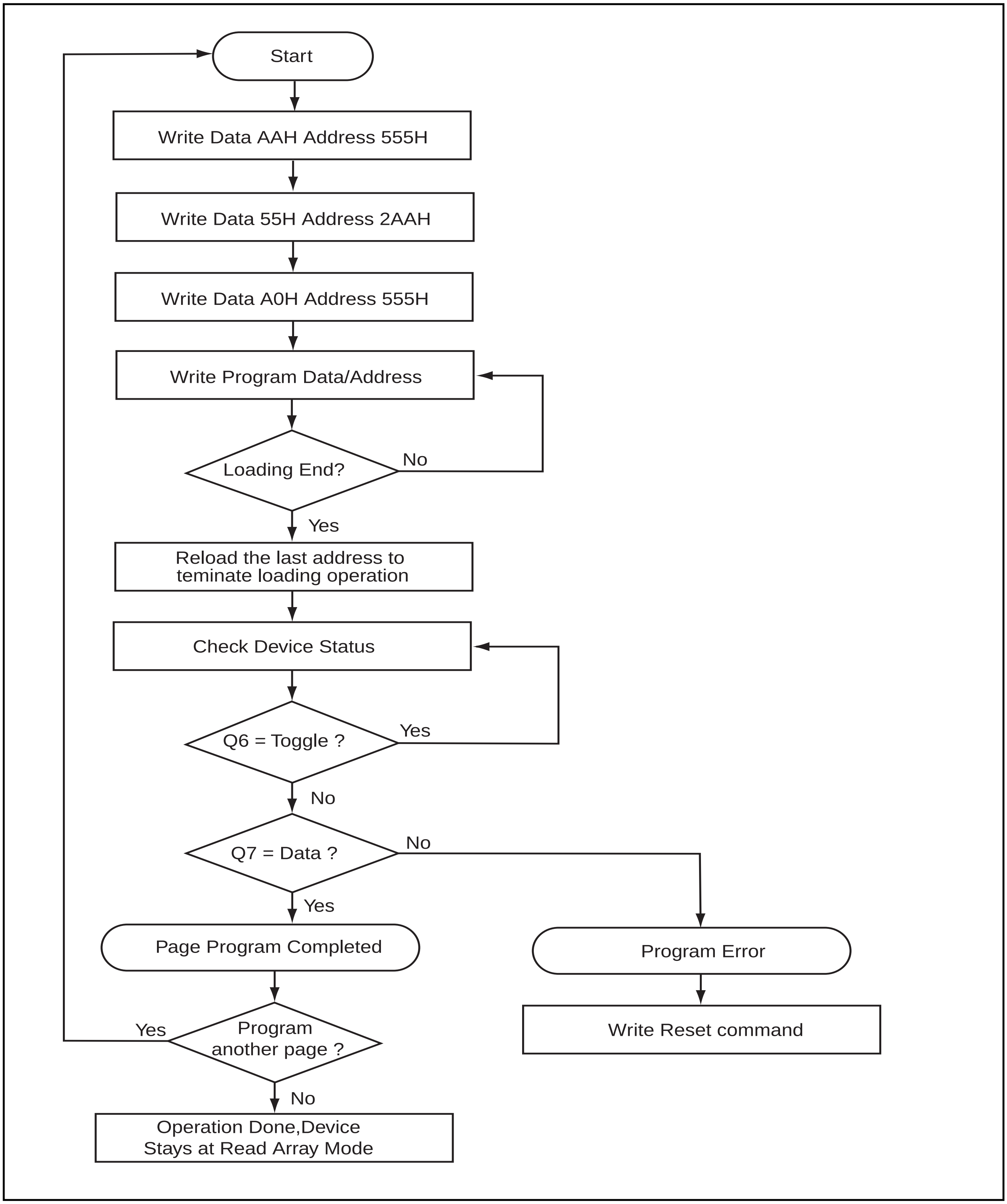


Table 6 DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
IIL	Input Load Current			1	uA	Vcc = Vcc Max VIN = Vcc or GND
ILO	Output Leakage Current			10	uA	Vcc = Vcc Max VIN = Vcc or GND
ISB1	Vcc Standby Current (CMOS)		1	10	uA	Vcc = Vcc Max $\overline{CE}$ = VIH
ISB2	Vcc Standby Current (TTL)			5	mA	Vcc = Vcc Max $\overline{CE}$ = VIH
ICC1	Vcc Read Current		20	27	mA	Vcc = Vcc Max f = 8MHz, IOUT = 0mA
ICC2	Vcc Erase/ Suspend Current		20	35	mA	$\overline{CE}$ = VIH Block Erase Suspend
ICC3	Vcc Program Current		20	35	mA	Program in Progress
ICC4	Vcc Erase Current		8	15	mA	Erase in Progress
ICC5	Vcc Read/Write Current (Note 1)		25	45	mA	Read/Write in Progress
ICC6	Vcc Read/Erase Current (Note 1)		25	45	mA	Read/Erase in Progress
VIL	Input Low Voltage	-0.5		0.8	V	
VIH	Input High Voltage	0.7 x Vcc		Vcc+0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA Vcc = Vcc Min
VOH	Output High Voltage	Vcc-0.4			V	IOH = -100uA Vcc = Vcc Min
		0.85Vcc			V	IOH = -2mA Vcc = Vcc Min
VID		8.5	10	10.5	V	

Table 7 AC CHARACTERISTICS - READ OPERATIONS

SYMBOL	DESCRIPTIONS	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		55	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output High Z (Note 1)		40	ns	$\overline{CE}$=VIL
tOH	Address to Output Hold		0	ns	$\overline{CE}$=$\overline{OE}$=VIL

Note 1: Not 100% Tested.

Figure 8 Key to Switching Waveforms

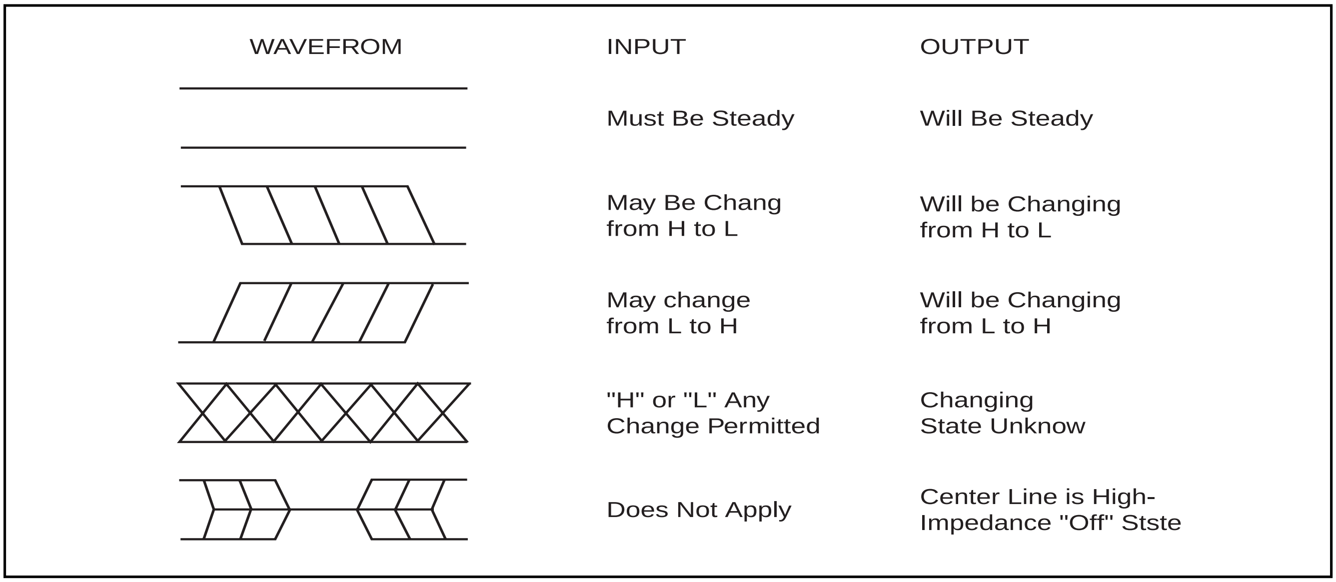
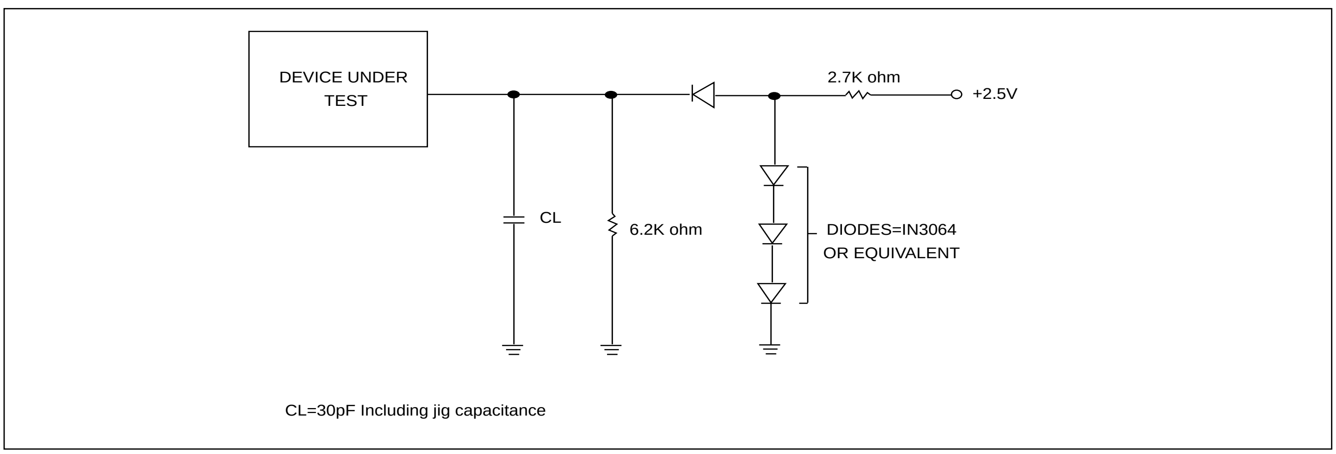


Figure 9 Switching Test Circuits



Test Specifications

Test Condition		Unit
Output Load	1TTL	
Output Load Capacitance,CL (in cluding jig capacitance)	30	pF
Input rise & fall time	5	ns
Input pulse Level	0~2.5	V
Input timing measurement reference levels	1.25	V
Output timing measurement reference levels	1.25	V

Figure 10 Switching Test Waveforms

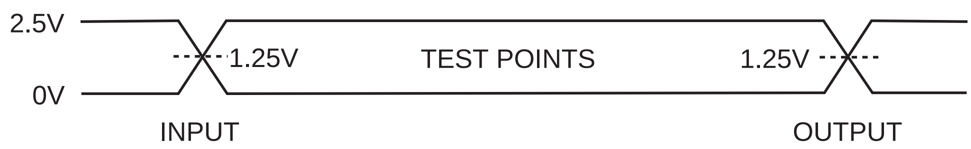


Figure 11 AC Waveform for Read Operations

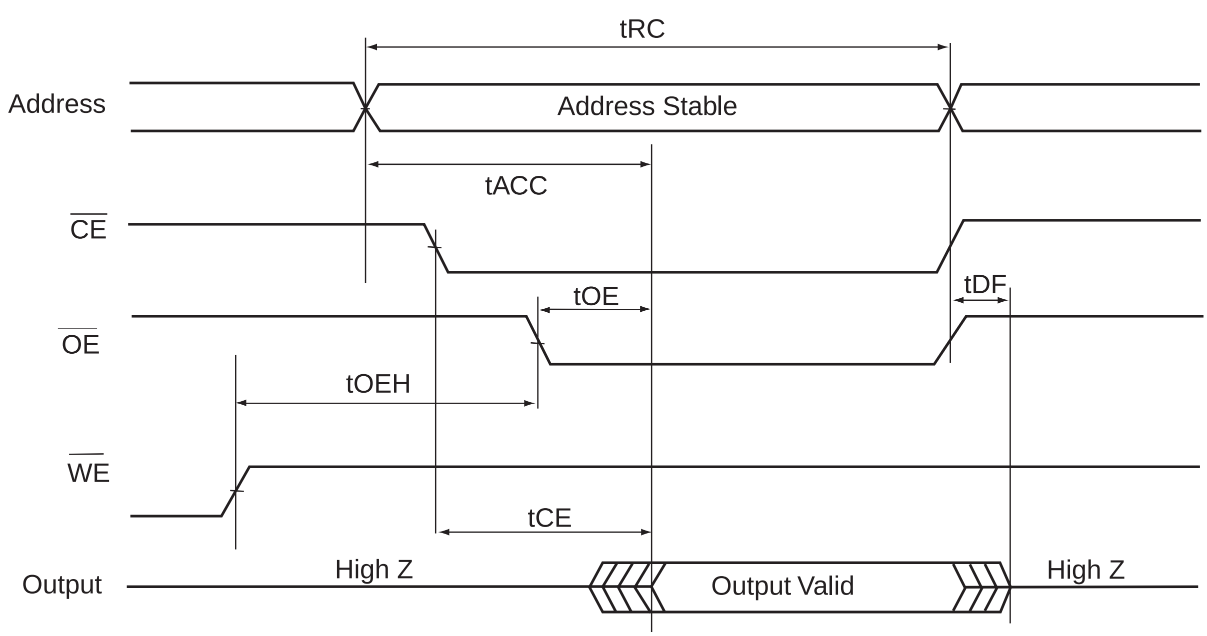


Figure 12 AC Waveform for Hardware Reset/Read Operations

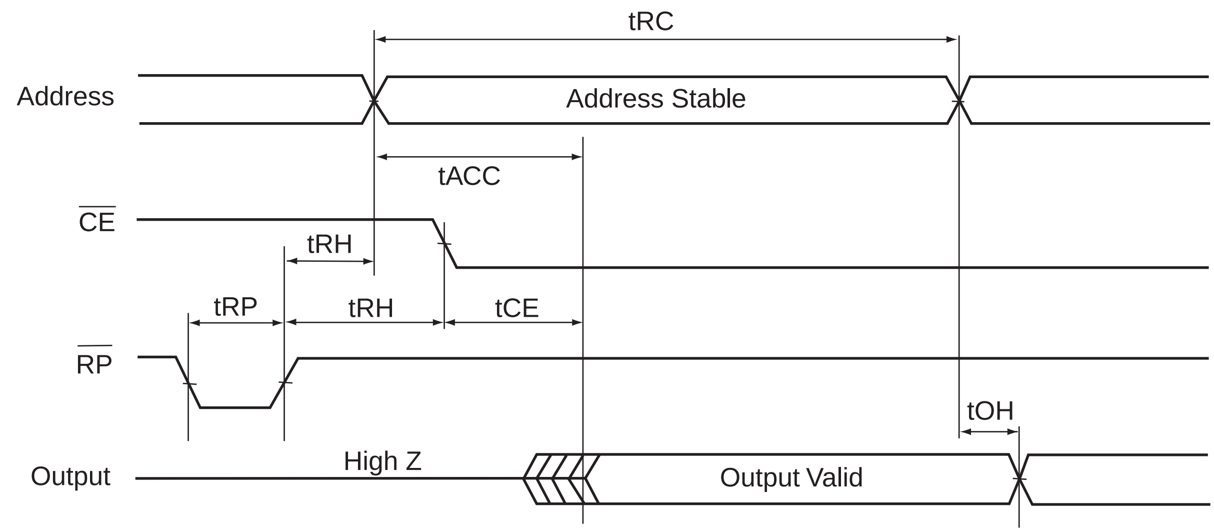
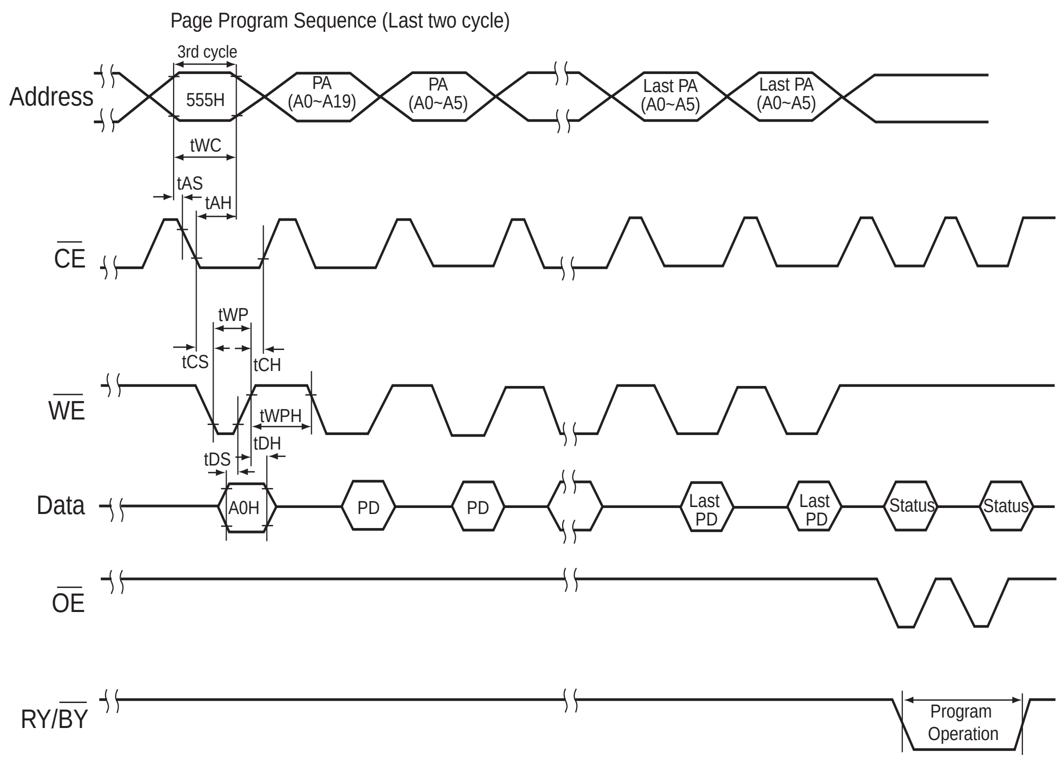


Table 8 AC CHARACTERISTICS-WRITE/ERASE/PROGRAM OPERATION

SYMBOL	DESCRIPTIONS	MIN.	MAX.	UNIT	CONDITIONS
tWC	Write Cycle Time	120		ns	
tAS	Address Setup Time	0		ns	
tAH	Address Hold Time	65		ns	
tDS	Data Setup Time	65		ns	
tDH	Data Hold Time	0		ns	
tOES	Output Enable Setup Time	0		ns	
tCES	$\overline{CE}$ Setup Time	0		ns	
tGHWL	Read Recover Time Before Write	0		ns	
tCS	$\overline{CE}$ Setup Time	0		ns	
tCH	$\overline{CE}$ Hold Time	0		ns	
tWP	Write Pulse Width	65		ns	
tWPH	Write Pulse Width High	35		ns	
tVCS	$\overline{CE}$ setup Before VCC Ready	0		ns	
tBUSY			120	ns	
tRB			0	ns	
tRP		50		ns	
tREADY			300	us	

Figure 13 Automatic Page Program Timing Waveform(Word Mode)



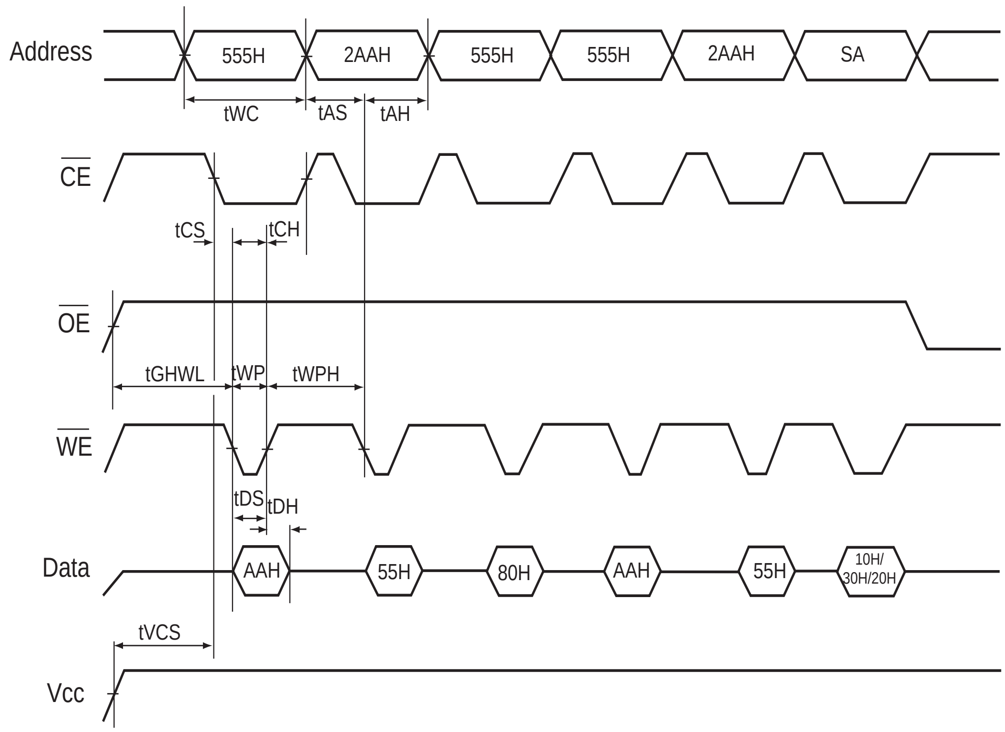
Legend :PA : Program addr. PD : Program data

Note : 1.A6~A19 for page addr.

2.It is necessary to write the last PA twice to terminate PD loading operation.

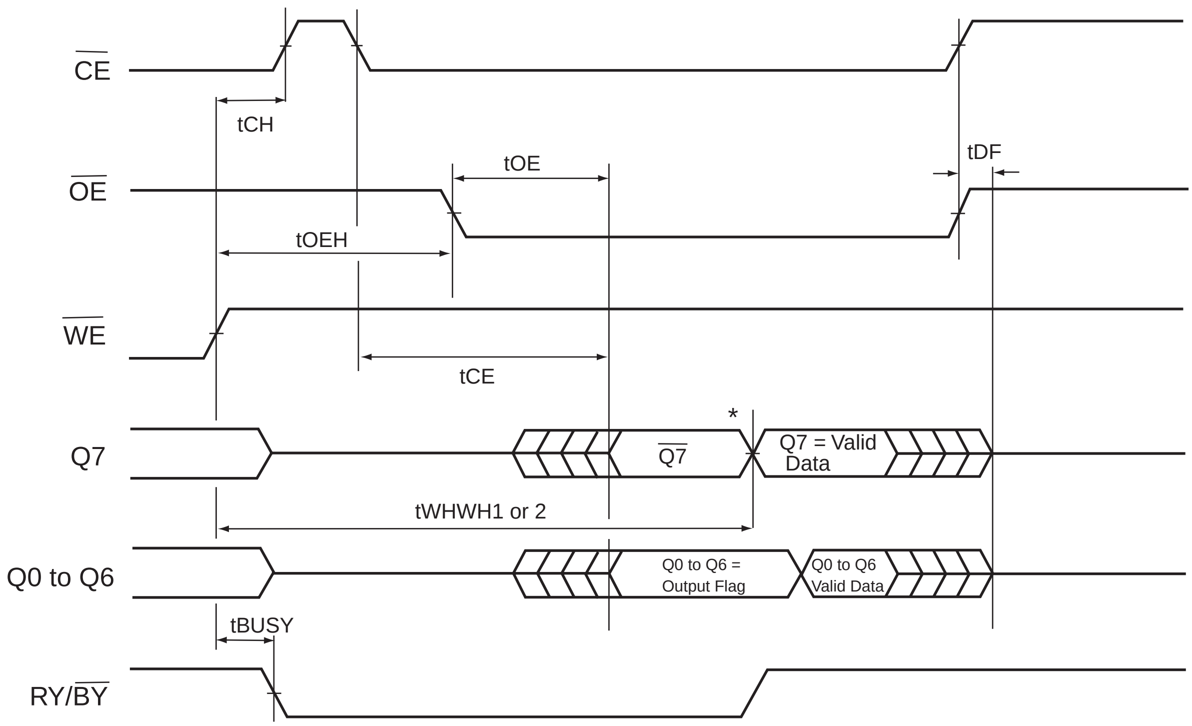
Status:Q7: Data Polling,Q6: toggle bit I,Q5:exceeded timing limits,Q3: Block Erase Status bit ,Q2: toggle bit II.

Figure 14 AC Waveform Chip/Block Erase Operations (Word Mode)



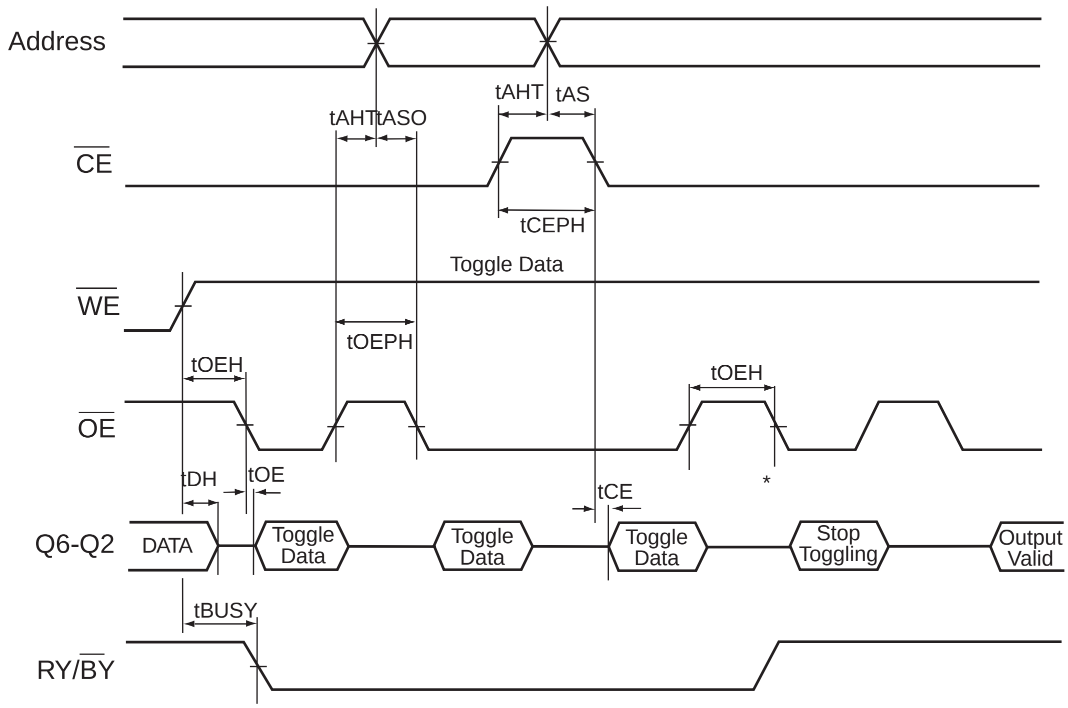
Notes: 1. SA is the sector address for sector Erase Address = 555H(Word),AAAH(Byte) for Chip Erase.
= A12~A19 for Block Erase.
2.These Waveform are for the word mode.(The address differ from byte mode.)
3.It is necessary to write the last SA twice to terminate SA loading operation for multi-block erase.

Figure 15 AC Waveforms for $\overline{Data}$ Polling Automatic Algorithm Operations



*:Q7 = Valid Data (The device has completed the automatic operation).

Figure 16 AC Waveform for Toggle Bit 1 during Automatic Algorithm Operation



*: Q6 stops toggling (The Device has completed the Automatic operation).

Figure 17 RY/BY Timing Diagram during Program/Erase Operation

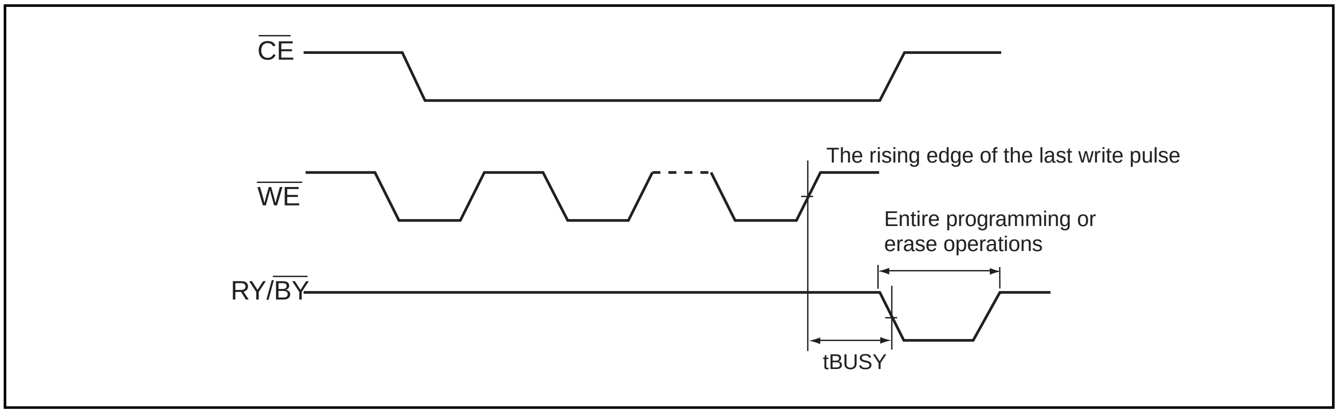


Figure 18 RP/RY/BY Timing Diagram

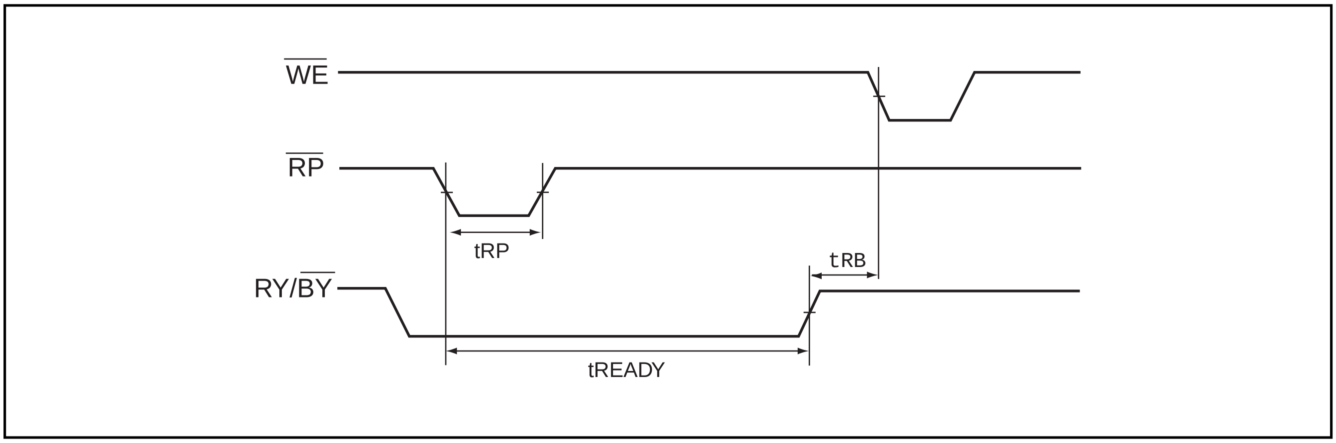


Figure 19 Timing Diagram for Word Mode Configuration

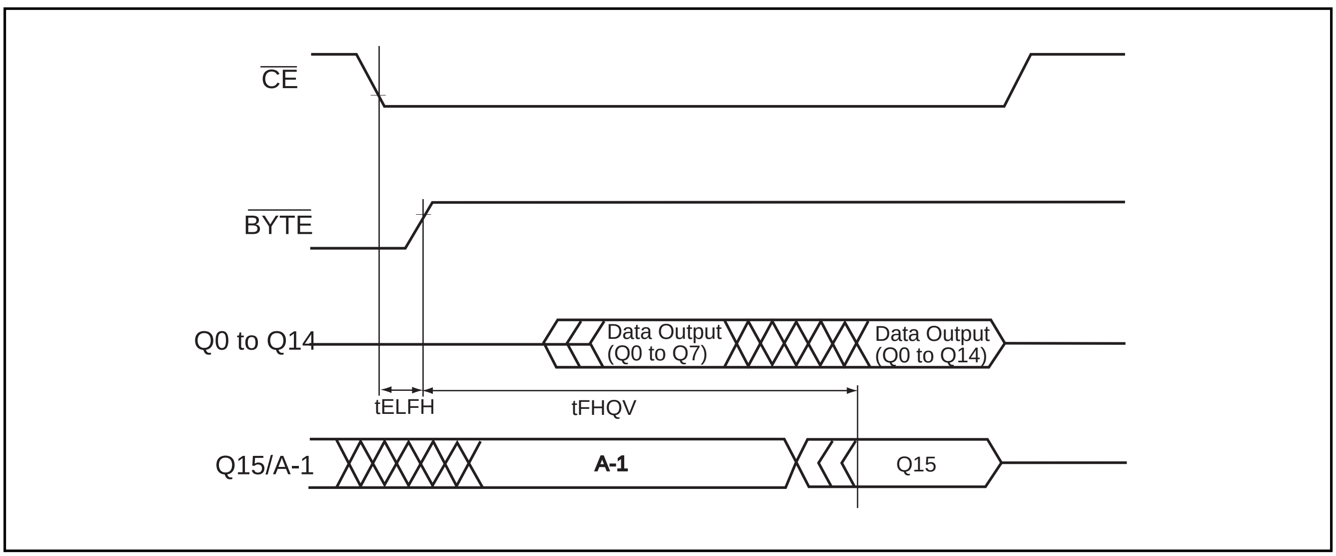


Figure 20 Timing Diagram for Byte Mode Configuration

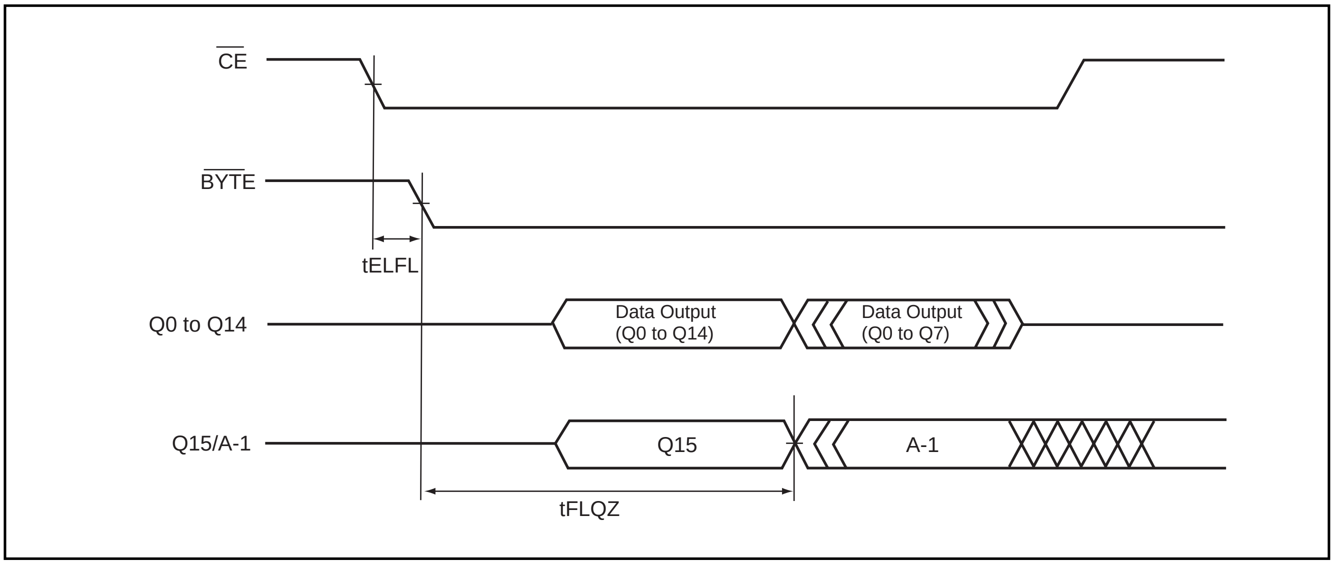


Figure 21 AC Waveform for Group Protection (Word Mode)

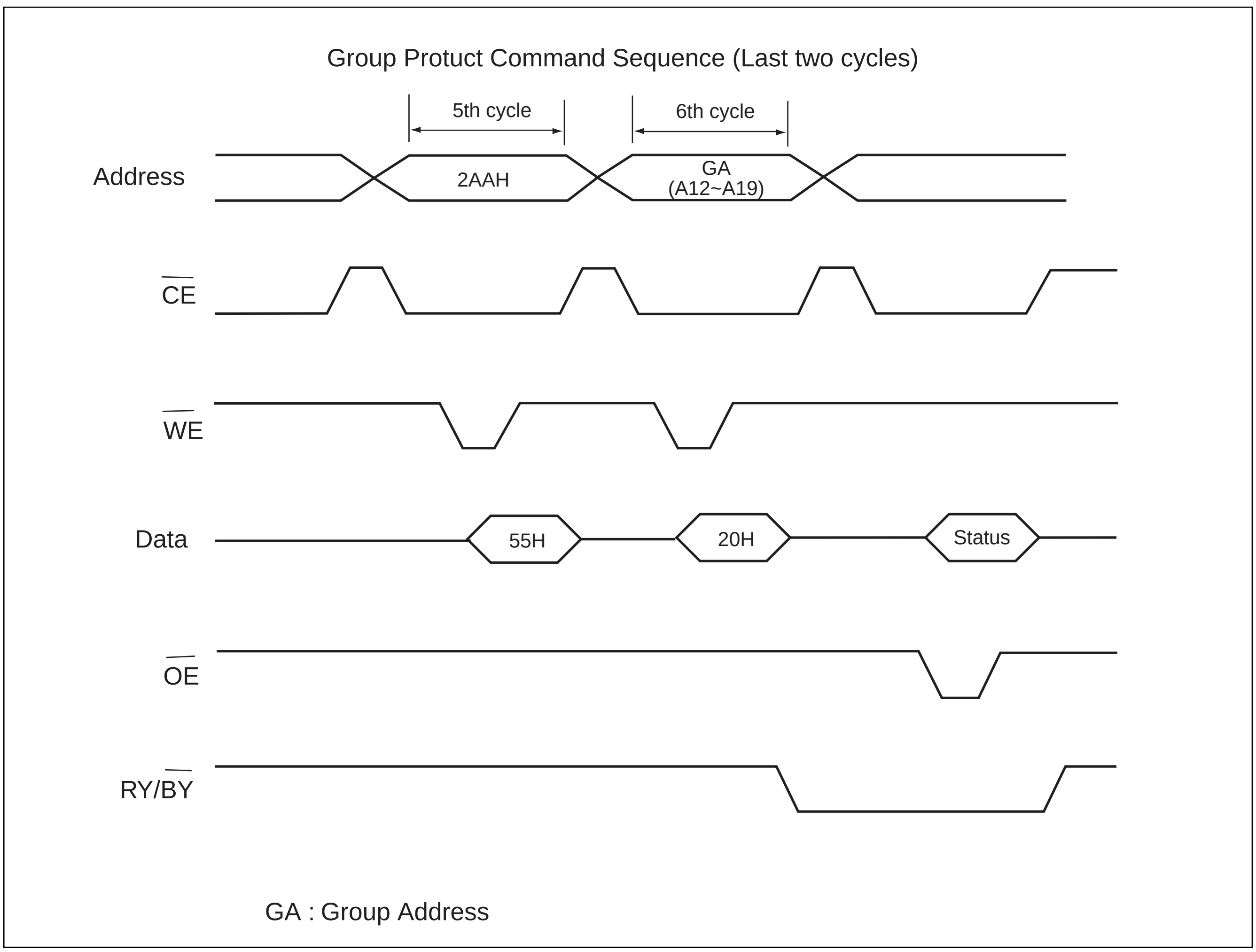


Figure 22 AC Waveform For Group Unprotection (Word Mode)

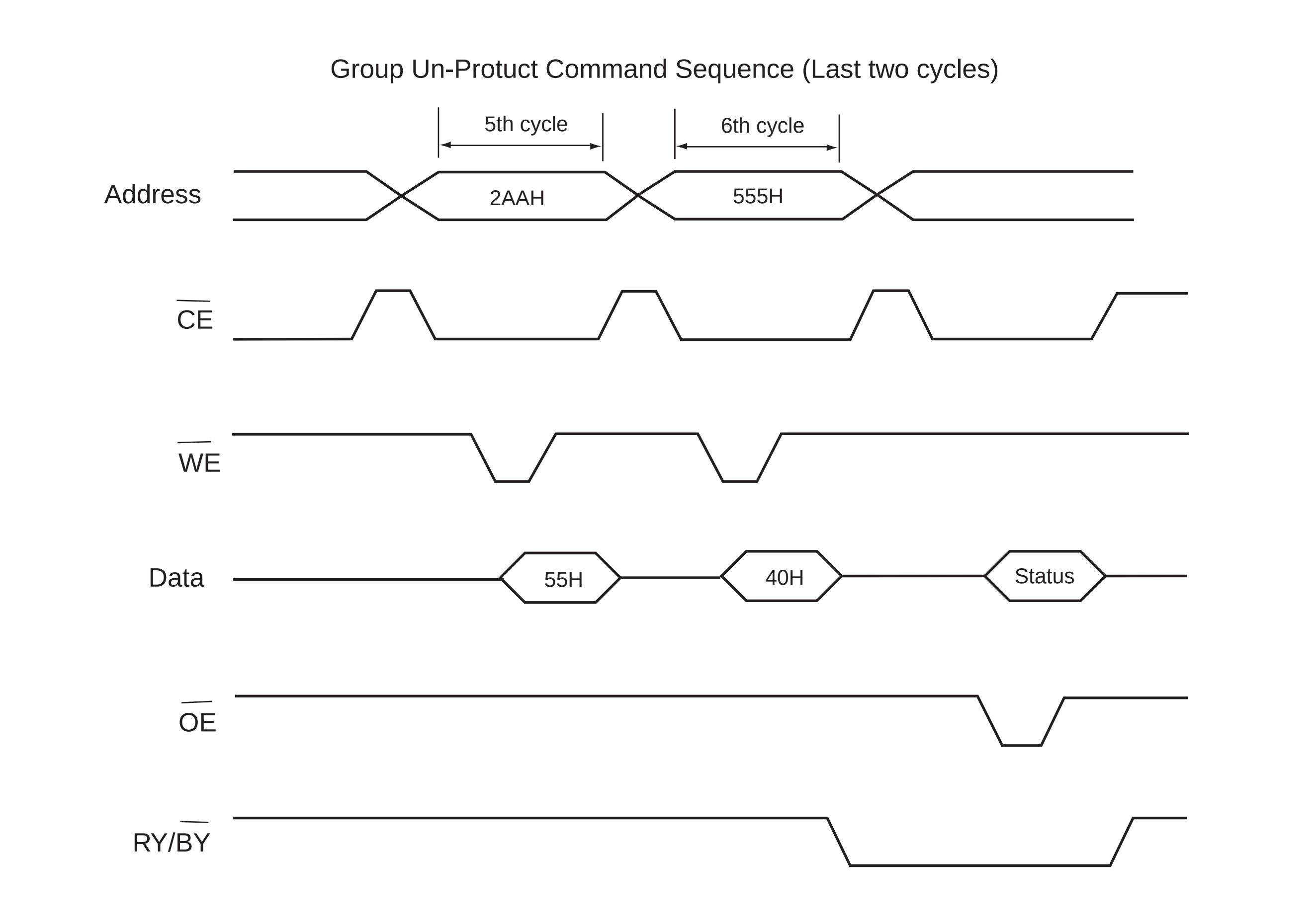


Figure 23 ID Code Read Timing Waveform

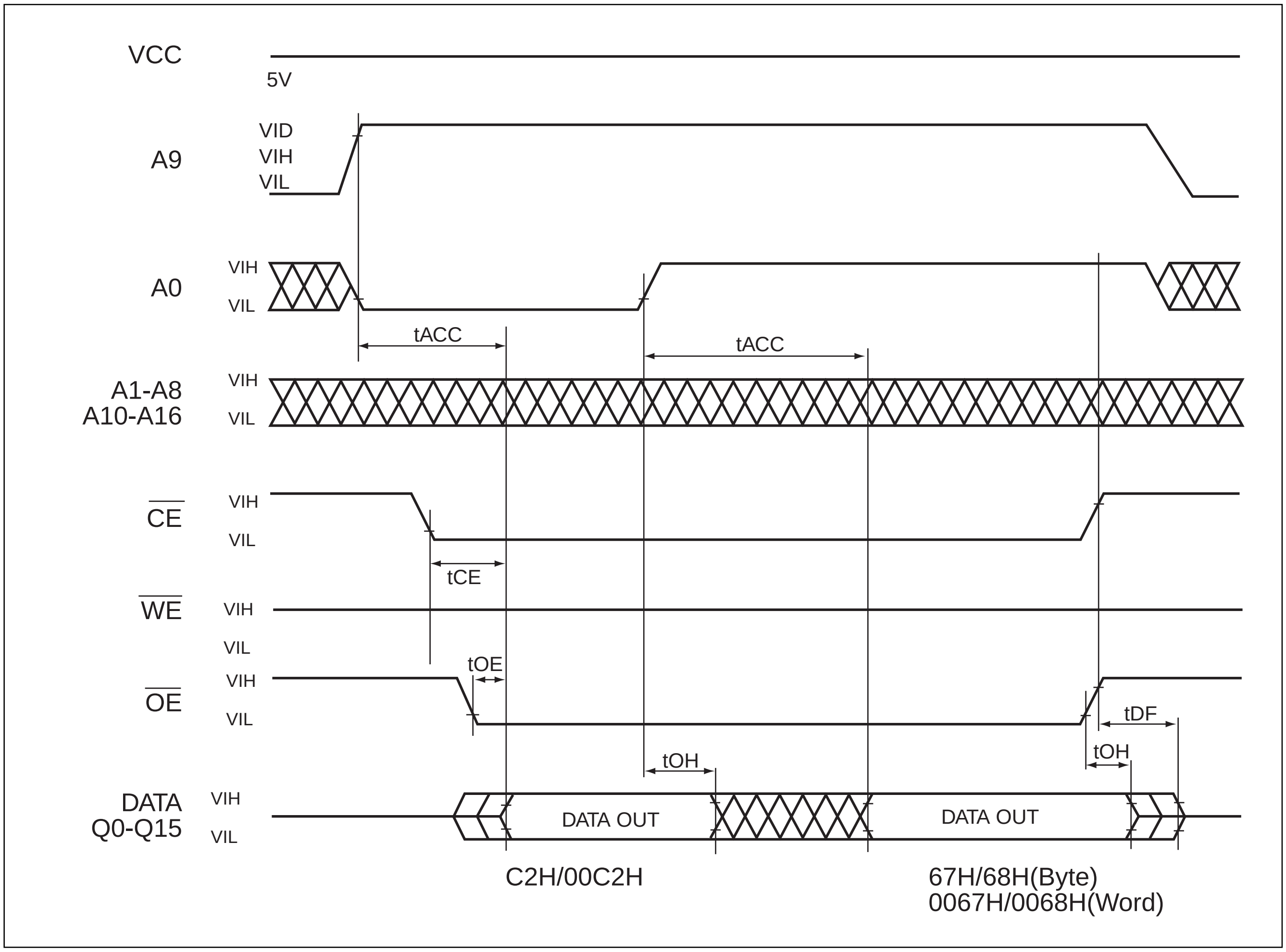
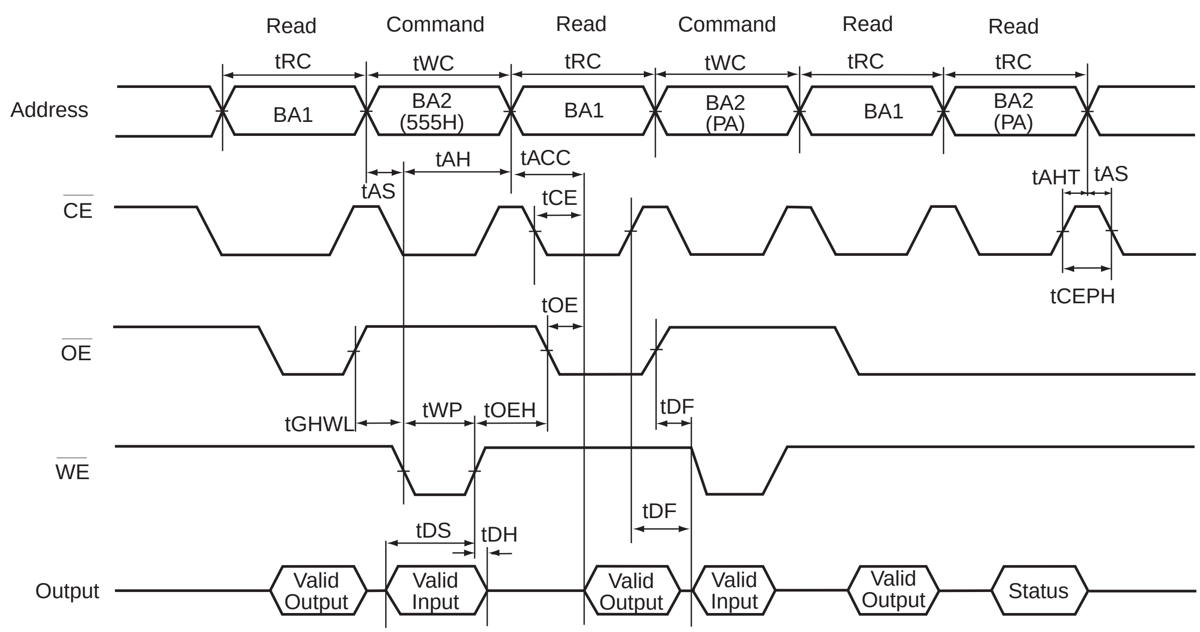
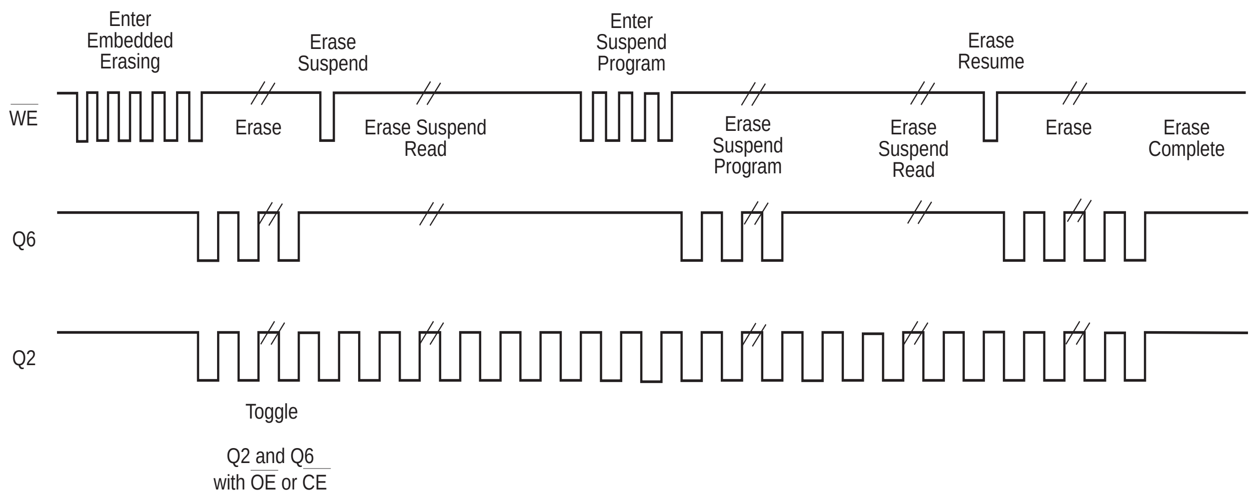


Figure 24 Back to Back Read/Write Timing Diagram



NOTE : This is example of read for Bank 1 and Embedded Alogorithm (Program) for Bank 2.
BA1 :Address of Bank 1.
BA2 : Address of Bank 2.

Figure 25 Q2 Vs Q6



NOTE : Q2 toggles only when read at an address within an erasing or erase-suspended block.

Table 9 ERASE AND PROGRAMMING PERFORMANCE

	LIMITS			
PARAMETER	MIN.	TYP.	MAX.	UNITS
Single/Block Erase Time		20	400	ms
Multi Block Erase Time		50	400	ms
Chip Erase Time		50	400	ms
Page Programming Time		4	80	ms
Chip Programming Time		64	128	sec.
Byte Programming Time (Avg.)		32	640	ms
Erase/Program Cycles	100,000			Cycle

Table 10 LATCHUP CHARACTERISTICS

	MIN.	MAX.	UNITS
Input Voltage with respect to GND on all pins except I/O pins	-1.0	10.5	V
Input Voltage with respect to GND on I/O pins	-1.0	Vcc+1.0	V
Current	-100	+100	mA
Includes all pins except Vcc. Test conditions: Vcc = 3.0V, one pin at a time.			

Table 11 ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40℃ to 85℃
Storage Temperature	-65℃ to 125℃
Applied Input Voltage	-0.5V to Vcc + 4.5
Applied Output Voltage	-0.5V to Vcc +0.6
Vcc to Ground Potential	-0.5V to 5.5V
A9	-0.5V to 13.0V

Table 12 OPERATING RANGES

RATING	VALUE
Ambient Temperature	0℃ to 70℃ (Comm.) -40℃ to 85℃ (Ind.)
Vcc Supply Voltage	2.25V to 3.0V

Ordering Information

Part No.	Access Time(ns)	Temperature Range	Package Type	Package Ball Type	Package Ball Pitch
MX29VW160TTC-12	120	Comm.	48 Pin TSOP		
MX29VW160TTI-12	120	Ind.	48 Pin TSOP		
MX29VW160TXAC-12	120	Comm.	48 Ball CSP	uBGA	0.75mm
MX29VW160TXAI-12	120	Ind.	48 Ball CSP	uBGA	0.75mm
MX29VW160TXBC-12	120	Comm.	48 Ball CSP	BGA	0.80mm
MX29VW160TXBI-12	120	Ind.	48 Ball CSP	BGA	0.80mm

Note:
1. Top Boot Block as an sample.For Bottom Boot Block ones,MX29VW160TXXX will be changed to MX29VW160BXXX)
2. 0.75mm ball pitch uBGA is under evaluation.

REVISION HISTORY

Revision	Description	Page	Date
0.3	CSP package size:7mmx12mm ---> 8mmx13mmx1.2mm	P3	NOV/04/1998
	Add in ICC6:Vcc Read/Erase Current	P25	
	Remove tBACC & tBHZ	P25	
	Remove LGA Package	P41	
0.4	Change Sector structure of the 2Mb-Bank from 16KBx4+ 8KBx8+32KBx4 to 8KBx8+64KBx1	P1, 4, 5, 8	NOV/19/1998
	Add in $\overline{WP}$ pin	P1, 3, 5, 6, 14, 20	
	Change VIP range from 9.5V~10.5V to 8.5V~10.5V	P6, 14, 15, 25	
0.5	Vcc range change to 2.25V~3.0V	P1, 2, 3, 40	NOV/27/1998
0.6	Change Group Addr.: A12~A19	P8, 15, 17, 18, 35	DEC/03/1998
	Correct ID data	P11	
0.7	Block architecture description correction		

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