SL1925

Satellite Zero IF QPSK Tuner IC

Preliminary Information

DS4955 ISSUE 3.1 October 2001

Ordering Information
SL1925/KG/NP2S (Tubes)
SL1925/KG/NP2T (Tape and Reel)

Features

- Single chip system for direct quadrature down conversion from L-band
- High signal handling capability for minimum external component count application, requires external RF AGC of 30dB
- Compatible with DSS and DVB system requirements
- Excellent gain and phase match up to 30MHz baseband
- High output referred linearity for low distortion and multi channel application
- Fully balanced low radiation design
- Integral RF AGC amplifier
- Two selectable varactor tuned local oscillators with buffered output for driving external synthesiser loop
- ESD protection (Normal ESD handling procedures should be observed)

Applications

- Satellite receiver systems
- Data communications systems

Description

The SL1925 is a wideband quadrature converter operating from 950 to 2150 MHz, intended primarily for application in satellite tuners.

The device contains all elements necessary, with the exception of local oscillator sustaining network, to fabricate a high performance I(n-phase) & Q(uadrature) phase splitter and downconverter optimised for systems containing RF AGC gain control. The device allows for systems containing higher power analog interferers. For most applications RF tunable filtering is not essential.

The SL1925 is optimised for use with a low phase noise synthesiser, a range of which are available from Zarlink Semiconductor. This will form a complete front end tuner function for digital satellite receiver systems utilising DSP derotation recovery.

The device includes a very high signal handling front end with AGC, this provides for gain control, reference local oscillator with output buffer, phase splitter with I and Q mixers and baseband buffer amplifiers with external interstage filtering.

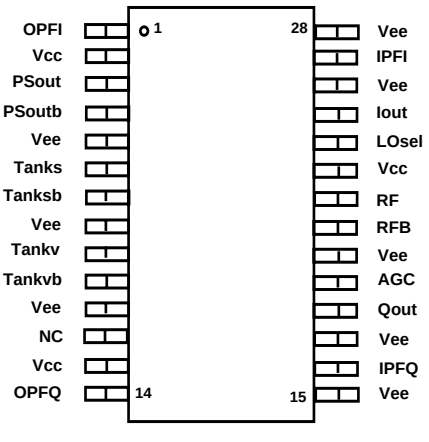


Figure 1 Pin connections

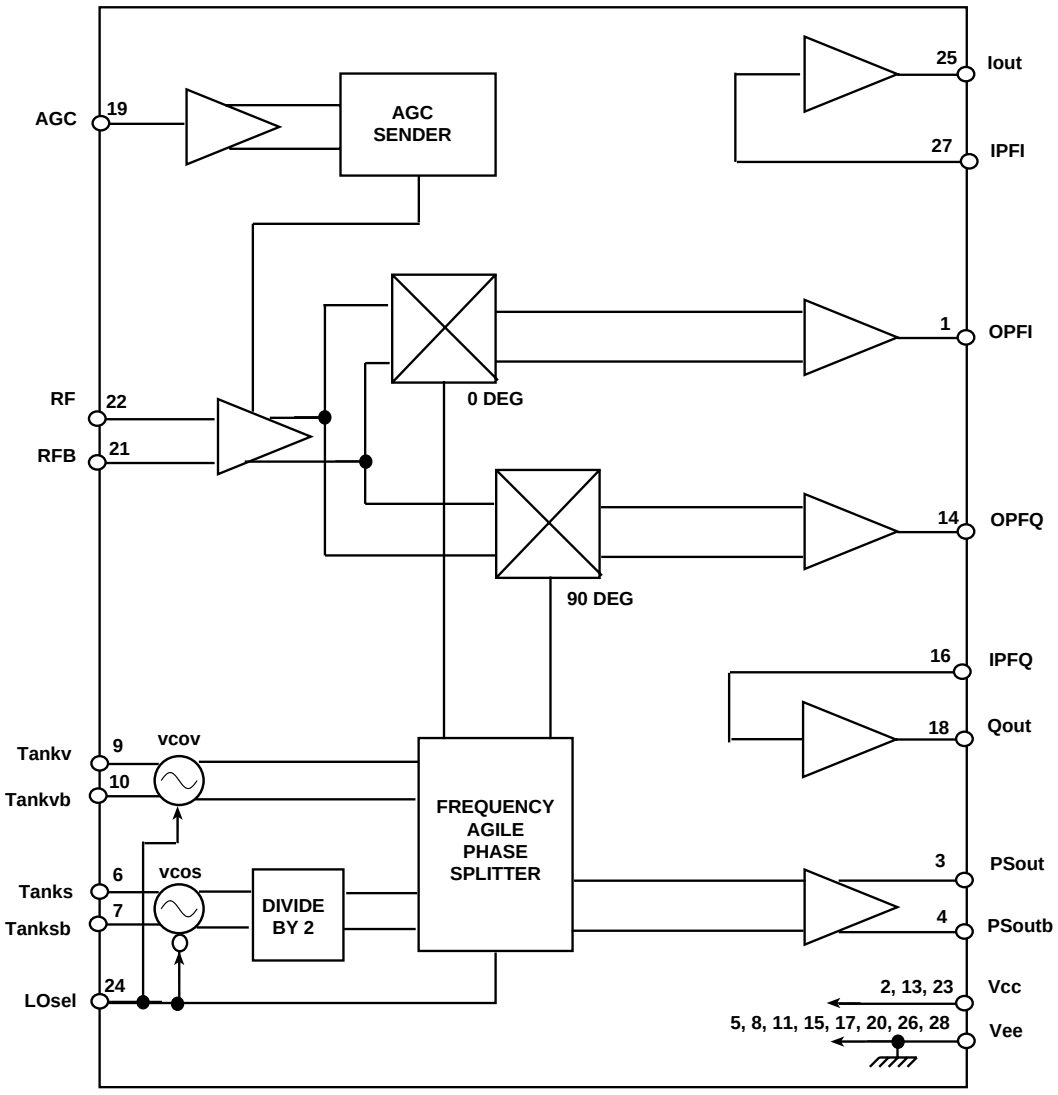


Figure 2 Block diagram

Quick Reference Data

Characteristic		Units
Operating range	950-2150	MHz
Input noise figure, DSB, maximum gain, 1500MHz	19	dB
Maximum conversion gain (assuming 6dB filter loss)	>55	dB
Minimum conversion gain (assuming 6dB filter loss)	<20	dB
$IP3_{2T}$ input referred	113	dBuV
Converter input referred IM3, two tones at 97dBµV	30	dBc
$IP2_{2T}$ input referred	140	dBuV
P1dB input referred	103	dBuV
Baseband amplifier Output limit voltage	2.0	V
Gain match up to 22 MHz	0.2	dB
Phase match up to 22 MHz	0.7	deg
Gain flatness up to 22 MHz	0.5	dB
Local oscillator phase noise across entire 950MHz to 2150MHz band:		
SSB @ 10 kHz offset	-80	dBc/Hz

Table 1

Functional Description

The SL1925 is a wideband direct conversion quadrature downconverter optimised for application in satellite receiver systems. A block diagram is given in Figure 2 and shows the device to include a broadband RF preamplifier with AGC control, two oscillator sustaining amplifiers, a frequency agile 90° phase splitter, I Q channel mixers and I Q channel baseband amplifiers. The only additional elements required are an external tank circuit for each oscillator, and baseband interstage filters. To fabricate a complete tuner an RF AGC stage offering +20dB to -10 dB of gain range and a 2.2 GHz PLL frequency synthesiser are also required. An example application is shown in Figure 16.

In normal application the first satellite IF frequency of typically 950 to 2150 MHz is fed via the tuner RF AGC stage to the RF preamplifier, which is optimised for impedance match and signal handling. The RF preamplifier is designed such that no tracking RF filter is required and also allows for analog interferers at up to 10 dB higher amplitude. The converter RF input impedance is shown in Figure 5. The amplifier signal is then fed to an AGC stage providing a minimum of 35dB AGC control, which together with the RF attenuator provides a possible overall tuner dynamic range of 65dB, to allow for normal operating dynamic range and MCPC systems. The signal is then split into two balanced channels to drive the I and Q mixers. The AGC characteristic, and gain variation of IIP3, IIP2, P1dB and NF are contained in Figs. 6, 7, 8, 9 and 10 respectively.

The required 950MHz to 2150MHz I and Q reference LO frequencies for quadrature direct conversion are generated by the on board oscillators named 'vcos' and 'vcov', and the phase splitter. Oscillator 'vcos' operates nominally from 1900MHz to 3000MHz and is then divided by two to provide 950MHz to 1500MHz. Oscillator 'vcov' operates nominally from 1400MHz to 2150MHz. Only one oscillator is active at any time and selection is made within the phase splitter under the control of the LOsel input. Each oscillator uses an external varactor tuned resonant network optimised for low phase noise with a single varactor line control. A recommended application circuit for the oscillators is shown in Figure 4. The LO from the phase splitter drives a buffer whose outputs 'PSout' and 'PSoutb' can be used for driving an external PLL control loop for the VCO's. The typical LO phase noise is shown in Figure 11.

The mixer outputs are coupled to baseband buffer outputs 'OPFI' and 'OPFQ' which drive external band limit filters. The output impedance of these buffers is contained in Figure 12. The outputs of the filters are then connected to the inputs 'IPFI' and 'IPFQ' of the baseband channel amplifiers. The outputs 'Iout' and 'Qout' provide for a low impedance drive and can be used with a maximum load as in Figure 3. The output impedance of this section is contained in Figure 13. An example filter for application with 30MS/s systems is contained in Figure 14.

All port peripheral circuitry for the SL1925 is shown in Figure 15a and 15b.

The typical key performance data at 5V Vcc and 25°C ambient are shown in the 'QUICK REFERENCE DATA' of Table 1.

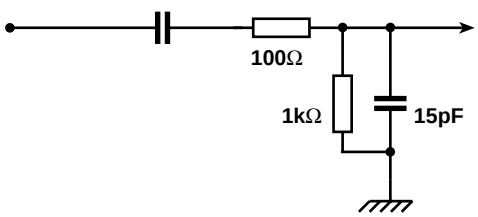
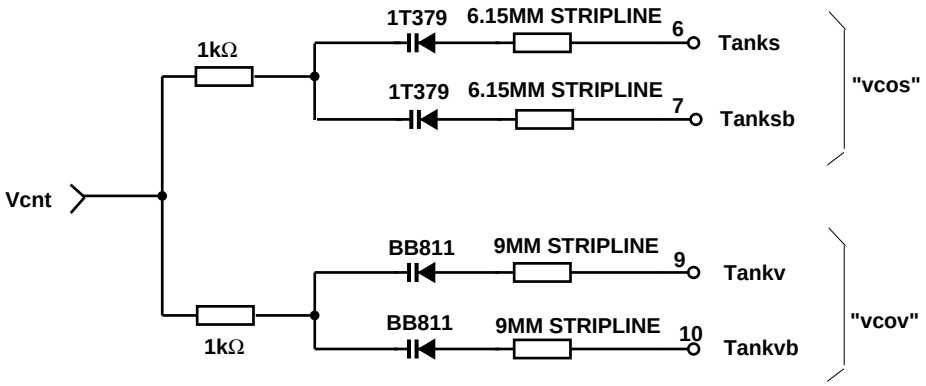
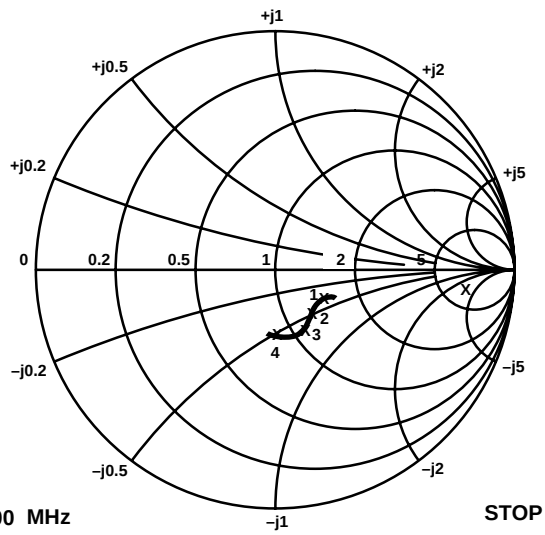


Figure 3 Baseband output load condition



Note: Stripline width =0.44mm,dimensions are approximate.

Figure 4 Local oscillator application circuit



Marker	Freq (MHz)	Zreal Ω	Zimag Ω
1	950	90	-18
2	1350	76	-15
3	1750	63	-35
4	2150	46	-29

START 700 MHz

STOP 2 500 MHz

Normalised to 50Ω

Figure 5 Converter RF input impedance (typical)

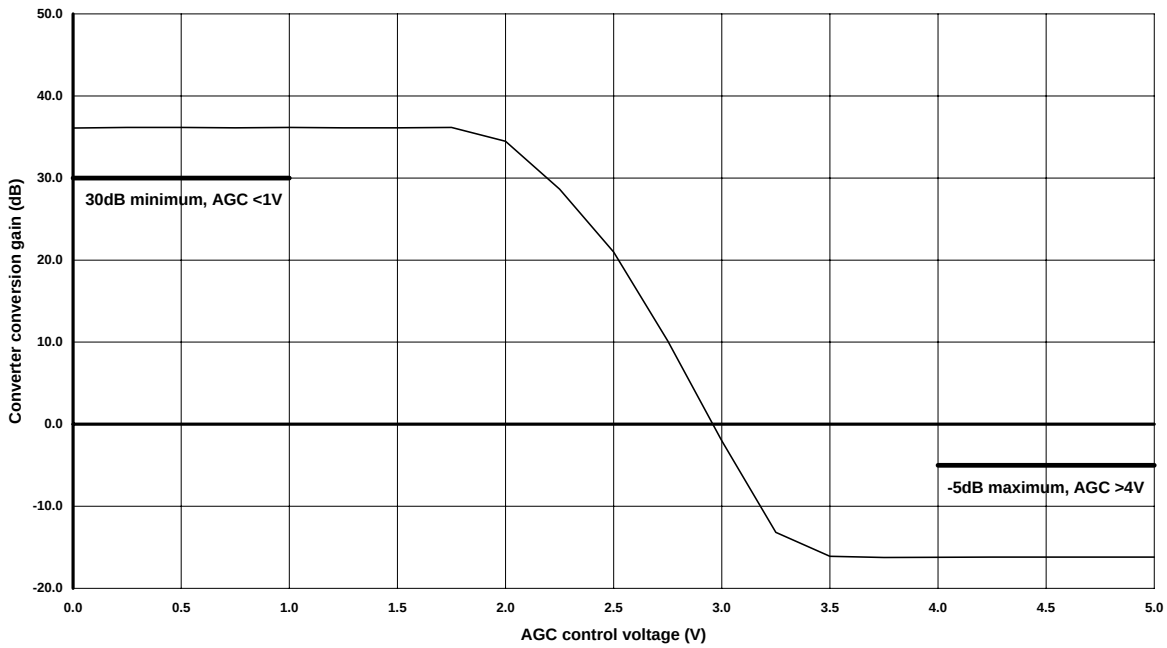


Figure 6 Converter gain variation with AGC voltage (typical)

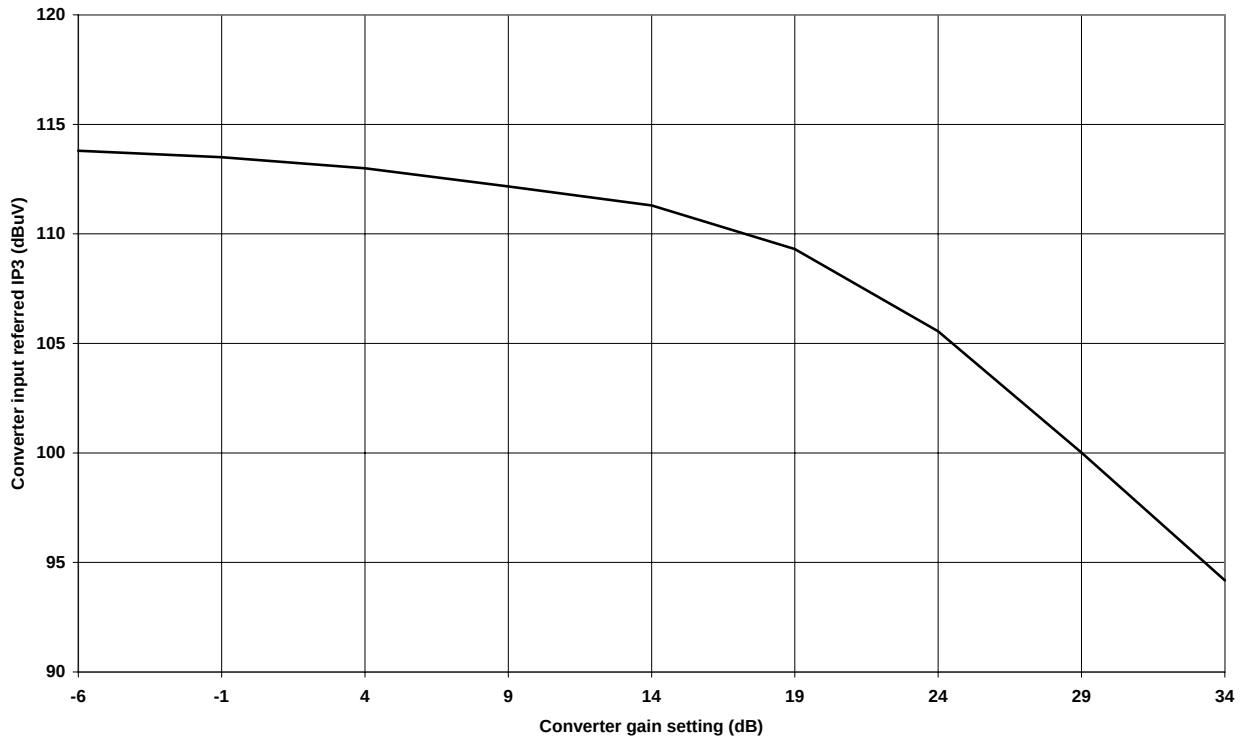


Figure 7 Converter input referred IP3 variation with gain setting (typical)

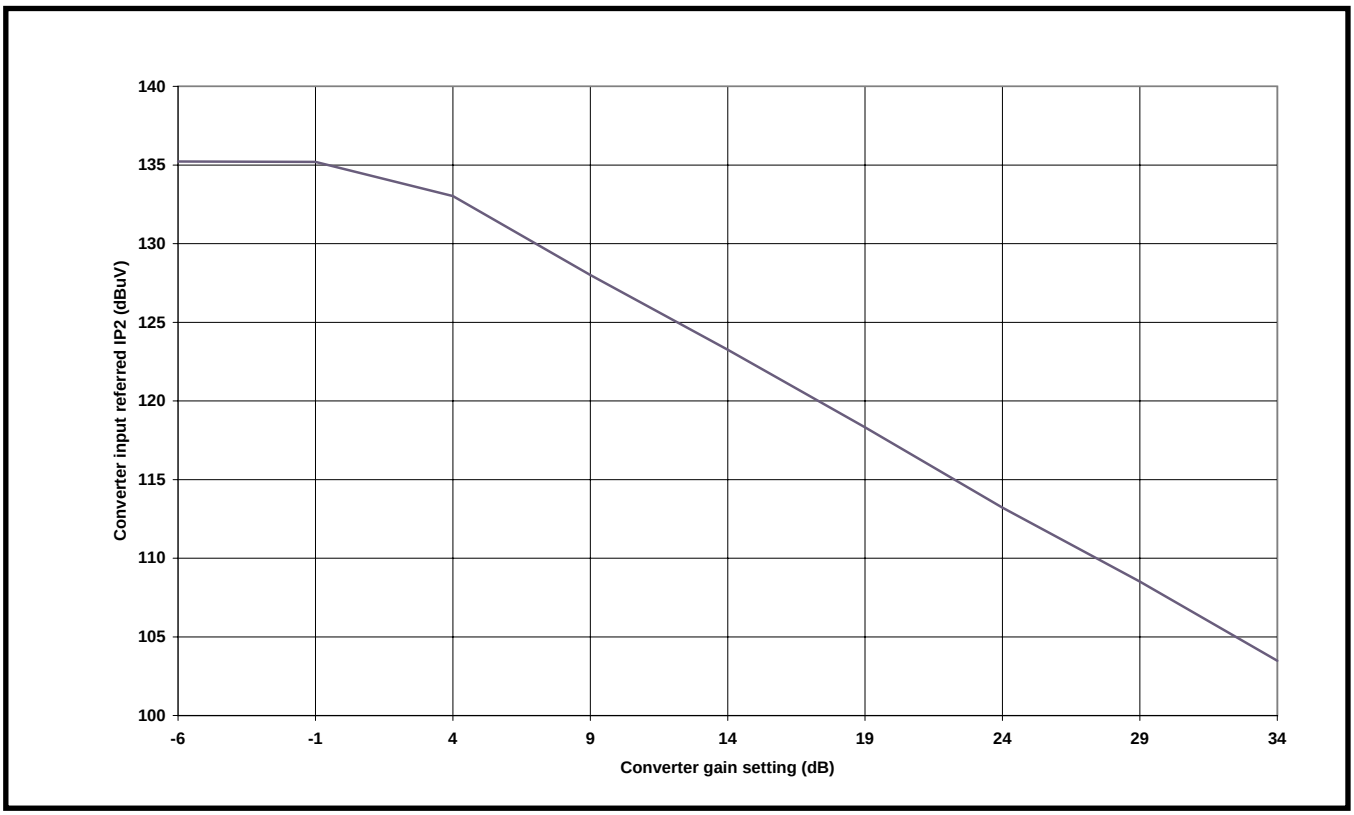


Figure 8 Converter input referred IP2 variation with gain setting (typical)

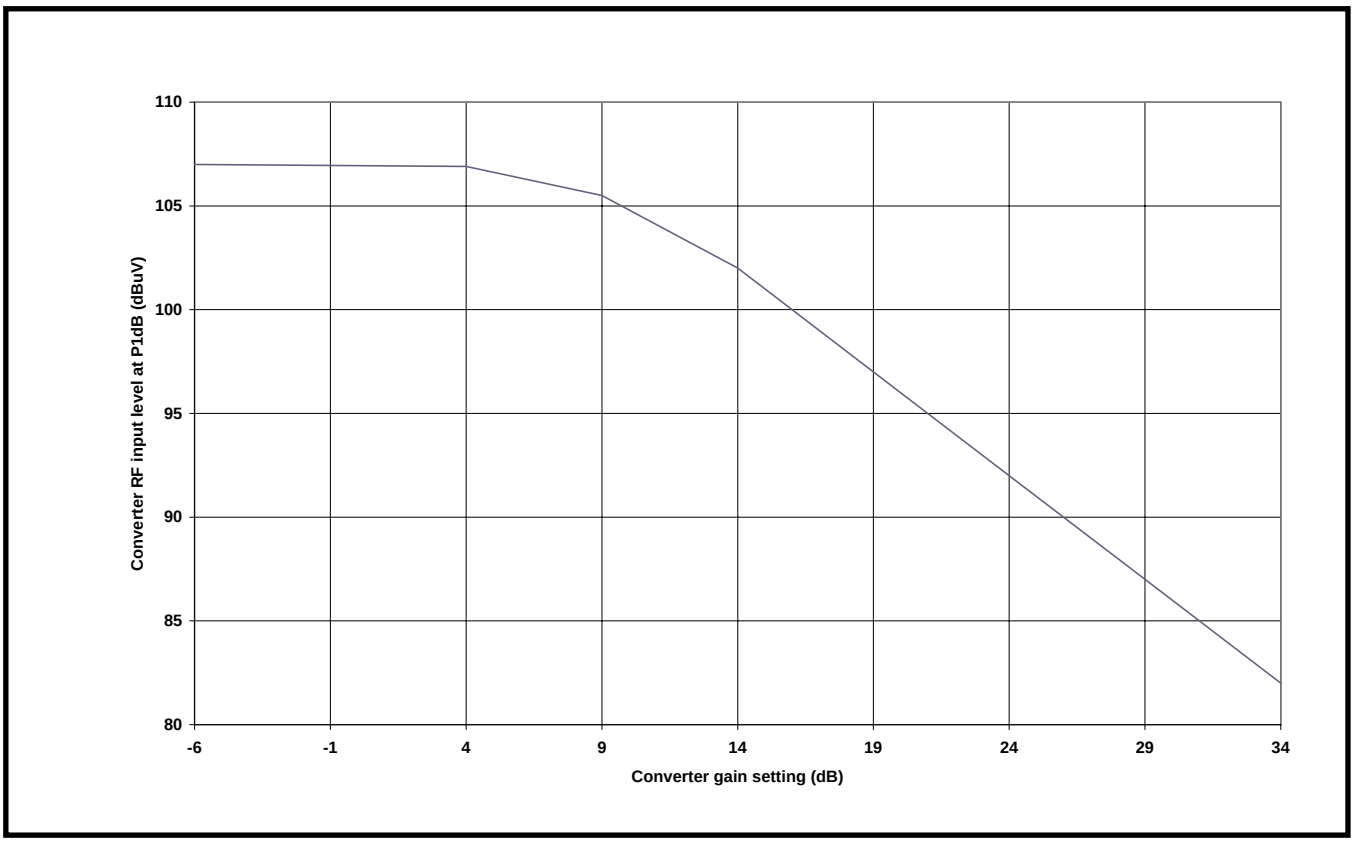


Figure 9 Converter input referred 1dB gain compression, P1dB (typical)

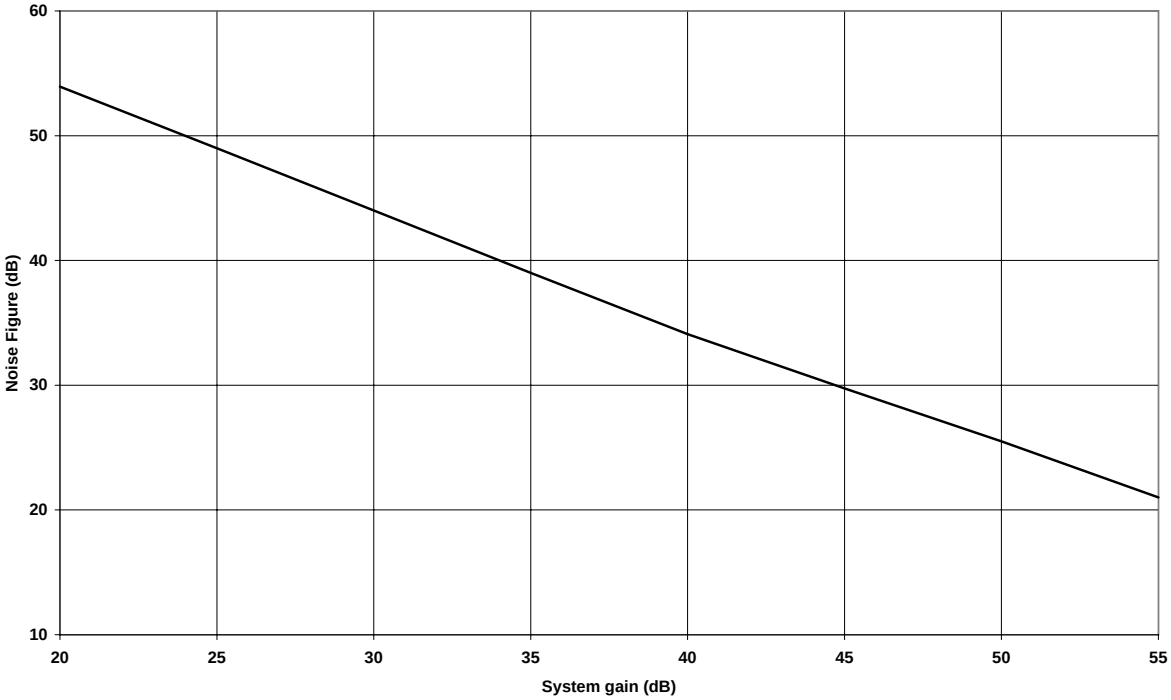


Figure 10 Noise figure variation with gain setting (typical)

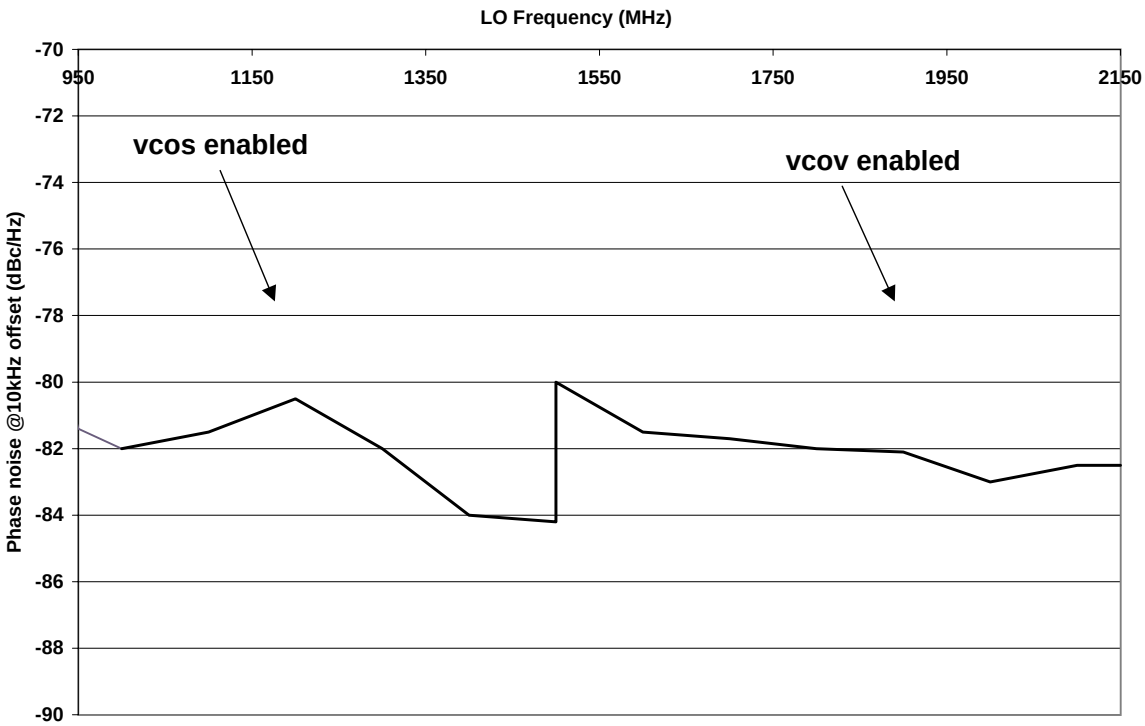
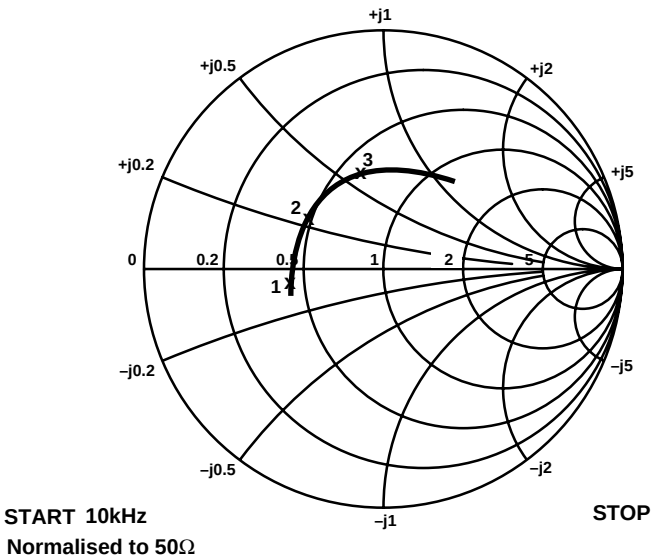
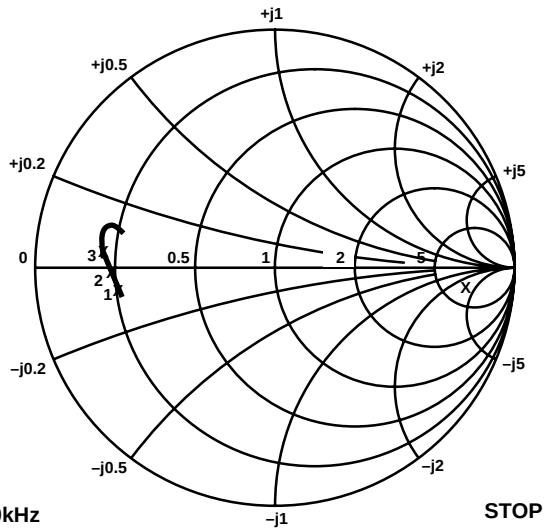


Figure 11 LO phase noise variation with frequency (typical)



Marker	Freq (MHz)	Zreal Ω	Zimag Ω
1	1	24	0.5
2	10	25	11
3	30	30	29

Figure 12 Converter output impedance, OPFI and OPFQ (typical)



Marker	Freq (MHz)	Zreal Ω	Zimag Ω
1	1	11.4	3.4
2	10	9.6	0.2
3	30	7.3	4.7

Figure 13 Baseband output impedance, Iout and Qout (typical)

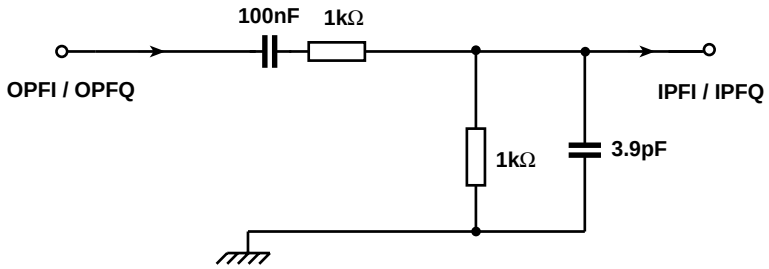
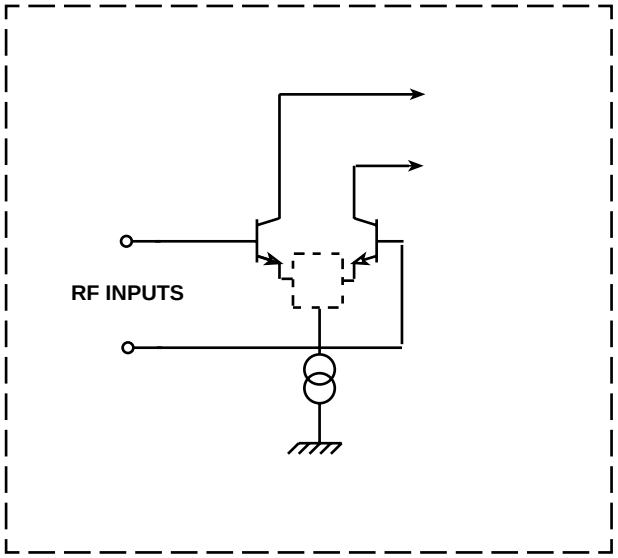
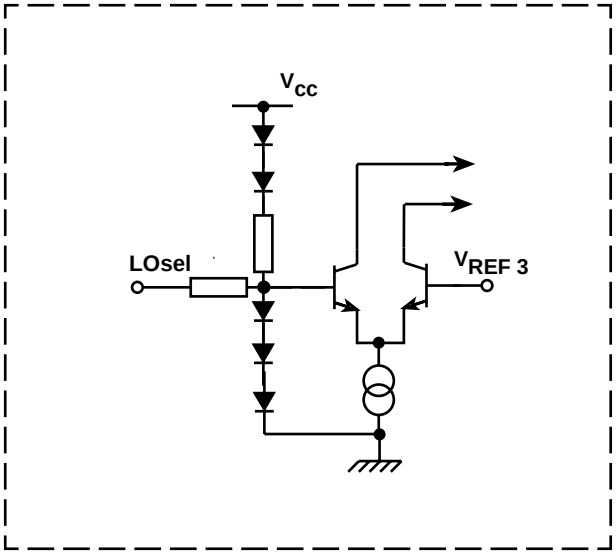


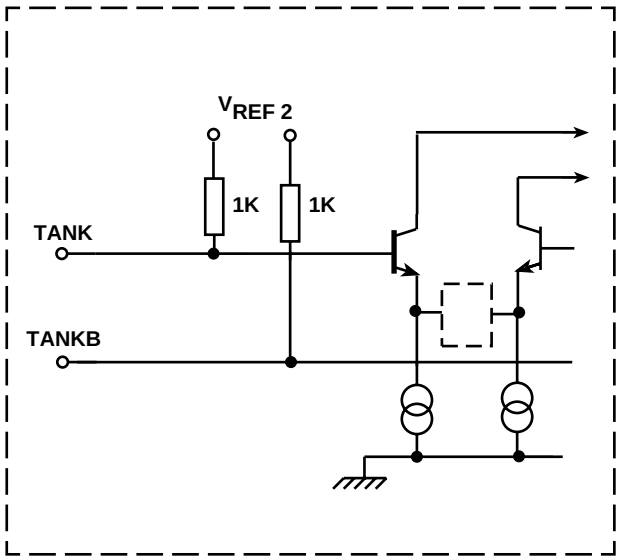
Figure 14 Example baseband interstage filter for 30MS/s application



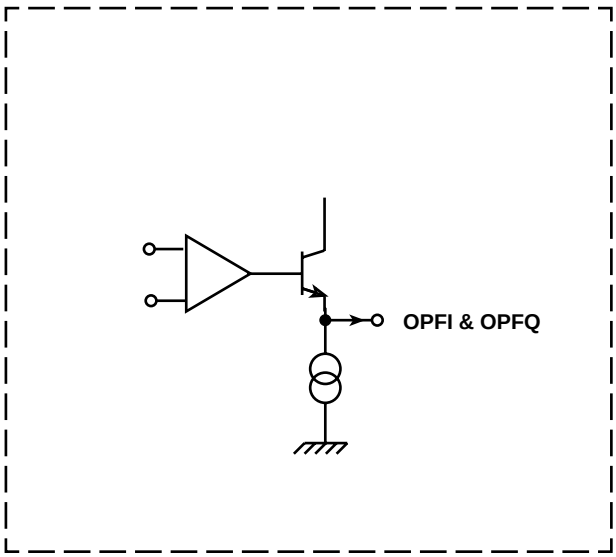
Converter RF inputs (pins 21, 22)



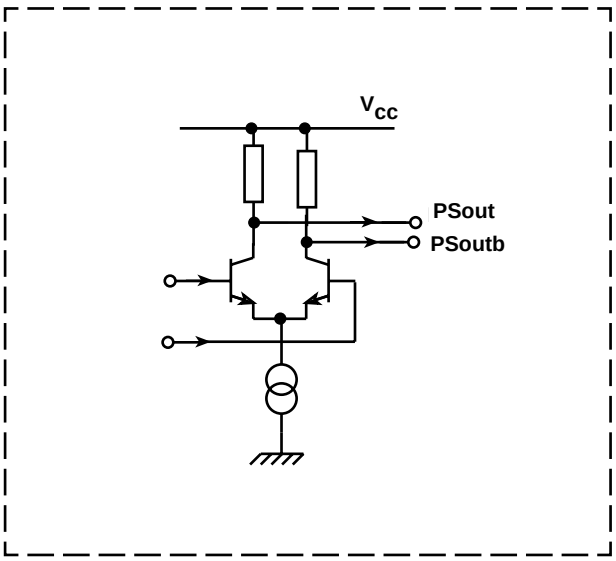
Oscillator select input (pin 24)



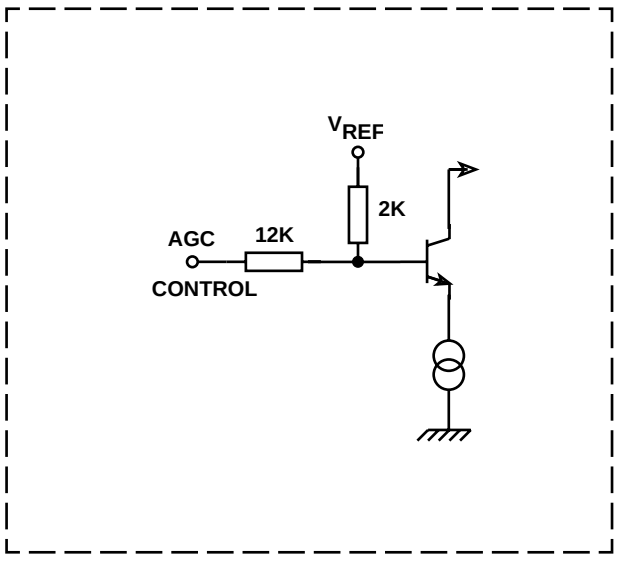
Oscillator inputs (pins 6, 7, and 9,10)



Converter outputs (pins 1, 14)



Prescaler buffer drive (Pins 3,4)



AGC input (pin 19)

Figure15a Input/Output interface circuits

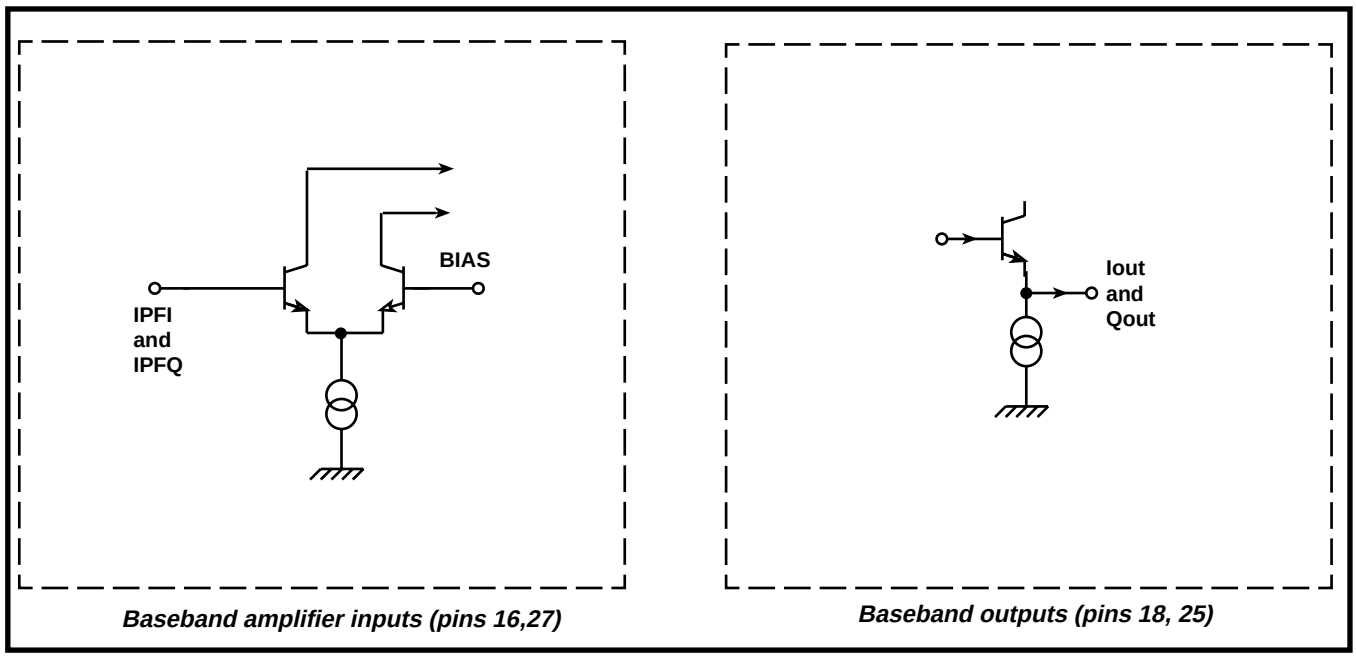


Figure 15b Input/Output interface circuits (continued)

Electrical Charqacterisitics

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

T_{amb} = -20°C to + 70°C, V_{ee}= 0V, Vcc = 4.75V to 5.25V. Desired channel at fc MHz

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current, Icc	2,13,23		130	175	mA	
RF input operating frequency	21,22	950		2150	MHz	
SYSTEM						All system specification items should be read in conjunction with Note 1.
System noise figure, DSB	21,22		19		dB	Maximum gain, AGC = 1V
Variation in system NF with gain adjust	21,22			-1	dB/dB	See Figure 10
System input referred IP2		135	140		dBµV	See Note 2.
System input referred IP3		110	113		dBµV	See Note 3.
System conversion gain						Terminated voltage conversion gain into load as in Figure 3. AGC monotonic from Vee to Vcc, see Figure 6
Minimum AGC gain				20	dB	AGC = 4.0V, 950MHz
Maximum AGC gain		59			dB	AGC = 1.0V, 950MHz
Gain Roll off			5		dB	950MHz to 2150MHz
System I/Q gain match	18,25	-1		+1	dB	Excluding interstage filter stage
System I/Q phase balance	18,25	-3		3	deg	Excluding interstage filter stage
System I & Q channel in band ripple	18,25			1	dB	Excluding interstage filter stage
LO 2nd harmonic interference level			-50		dBc	See Note 5
LNA 2nd harmonic interference level			-35		dBc	See Note 6
All other spurii on I & Q outputs	18,25			78	dBµV	Within 0 →100MHz band, under all gain settings, RF input set to deliver 108dBµV at baseband outputs
CONVERTER						
Converter input impedance	21,22		75		Ω	See Figure 5
Converter input return loss	21,22	10	12		dB	
Converter input referred IP2	21,22	121	130		dBµV	See Note 4
Converter input referred IP3	21,22	110	112		dBµV	See Note 4
Converter input referred IM2	21,22		-33	-24	dBc	See Note 4
Converter input referred IM3	21,22		-30	-26	dBc	See Note 4
Converter input referred 1dB gain compression (P1dB)	21,22					See Figure 9
Converter conversion gain						Terminated voltage conversion gain in load as in Figure 3.
Minimum AGC gain				-5	dB	AGC = 4.0V
Maximum AGC gain		30			dB	AGC = 1.0V
AGC gain control slope variation						Monotonic from Vee to Vcc, see Figure 6
AGC control input current	19	-250		250	µA	AGC bandwidth 100kHz

Electrical Characteristics (continued)

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.
T_{amb} = -20°C to + 70°C, V_{ee}= 0V, Vcc = 4.75V to 5.25V. Desired channel at fc MHz

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Converter output impedance	1,14		25	50	Ω	0.1 to 30MHz. See Figure 12
Converter output limiting	1,14	0.5	1.2		Vp-p	No Load
Converter bandwidth 1dB		40			MHz	No Load
Converter output roll off	1,14	6			dB/oct	
Oscillator vcos operating range Tanks/Tanksb	6,7	1900		3000	MHz	Giving LO = 950MHz to1500MHz Application as in Figure 4.
Oscillator vcov operating range, Tankv/Tankvb	9,10	1450		2150	MHz	Application as in Figure 4.
Local oscillator SSB phase noise	6,7		-80	-76	dBc/Hz	@ 10kHz offset PLL loop BW < 1kHz, application as Figure 4. Measured at baseband outputs of 10MHz
LO leakage to converter input	21,22		59	69	dBµV	
LOsel low voltage	24			0.6	V	Oscillator vcos enabled
LOsel high voltage	24	Vcc-0.7			V	Oscillator vcov enabled
LOsel low current	24			-50	µA	
LOsel high current	24			200	µA	
Prescaler output drive	3,4	88			dBµV	Single ended into 50Ω. Synthesiser should be driven differentially
Prescaler output impedance	3,4		50		Ω	
Prescaler output return loss	3,4	8			dB	
BASEBAND AMPLIFIERS						
Baseband amplifier input impedance	16,27					0.1 -30MHz bandwidth
Resistance		10			kΩ	
Capacitance				5	pF	
Baseband amplifier input referred IP3	16,27	94	97		dBµV	See Note 7
Baseband amplifier input referred IP2	16,27	99	111		dBµV	See Note 7
Baseband amplifier input referred IM3	16,27		-40	-34	dBc	See Note 7
Baseband amplifier input referred IM2	16,27		-34	-22	dBc	See Note 7
Baseband amplifier input referred 1dB compression (P1dB)	16,27	84			dBµV	Terminated voltage gain into load as in Figure 3.
Baseband amplifier gain	16,18 27,25	30			dB	Terminated voltage gain into load as in Figure 3

Electrical Characteristics (continued)

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.
T_{amb} = -20°C to + 70°C, V_{ee}= 0V, Vcc = 4.75V to 5.25V. Desired channel at fc MHz

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Baseband amplifier output impedance	18,25			20	Ω	
Baseband amplifier output limiting	18,25	2.0			Vp-p	pk-pk level at hard clipping. Load as in Figure 3.
Baseband amplifier 1dB bandwidth	18,25	40			MHz	Load as in Figure 3.
Baseband output roll off	18,25	6			dB/oct	Above 3dB point, no load

Notes : 1. Systems specifications refer to total cascaded system of front end converter/AGC stage and baseband amplifier stage with nominal 6dB pad as interstage filter and load impedance as in Figure 3.

2. AGC set to deliver output amplitude of 108dBµV on desired channel, input frequency fc and amplitude of 79dBµV, with two interferers of frequencies fc+146 and fc+155MHz at 97dBµV generating output intermodulation spur at 9MHz. 40MHz 3dB bandwidth interstage filter included.
3. AGC set to deliver output amplitude of 108dBµV on desired channel, input frequency fc and amplitude 79 dBµV, with two interferers of frequencies fc+110 and fc+211MHz at 97 dBµV generating output intermodulation spur at 9MHz. 40MHz 3dB bandwidth interstage filter included.
4. Two tones within RF operating frequency range at 97dBµV, conversion gain set at 4dB.
5. The level of 2.01GHz downconverted to baseband relative to 1.01 GHz with the oscillator tuned to 1 GHz, measured with no input filtering.
6. The level of second harmonic of 1.01 GHz input at -25 dBm downconverted to baseband relative to 2.01 GHz at -40 dBm with the oscillator tuned to 2 GHz, measured with no input filtering.
7. Two tones within operating frequency range at 77dBµV.

Absolute Maximum Ratings

All voltages are referred to Vee at 0V (pins 5,8,11,15,17,20,26,28)

Characteristic	Pin	Value		Units	Conditions
		Min	Max		
Supply Voltage, Vcc	2,13,23	-0.3	7	V	Transient condition only
PSout &PSoutb DC offset	3,4	Vcc-3.0	Vcc+0.3	Vp-p	
RF & RFB input voltage	21,22		2.5	Vp-p	AC coupled, transient conditions only
All other I/O ports DC offset	1,6,7,9	-0.3	Vcc+0.3	V	
	10,12				
	14,16				
	18,19				
	24,25,27				
Storage Temperature		-55	+150	°C	
Junction Temperature			+150	°C	
NP28 package					
Thermal resistance					
Chip to ambient			85	°C/W	
Chip to case			20	°C/W	
Power consumption at 5.25V			893	mW	
ESD protection	All	4		kV	Mil Std-883 latest revision method 3015 class 1

SL1925 Demo Board

The demo board contains an SL1925 direct conversion IC and SP5769 synthesiser. Reference to the specifications for each device may be required in conjunction with these notes.

The board contains all components necessary to demonstrate operation of the SL1925. The schematic and PCB layout of the board are shown in figures 16, 17 and 18. The SP5769 synthesiser is provided to control each of the oscillators of the SL1925.

Supplies

The board must be provided with the following supplies:

5V for the synthesiser, 30V for the varactor line and 5V for the SL1925.

The supply connector is a 5 pin 0.1" pitch pin header.

The order of connections is 5V - GND - 30V - GND - 5V

I^2C Bus Connections

The board is provided with a RJ11 I^2C bus connector which feeds directly to the SP5769 synthesiser. This connects to a standard 4 way cable which is supplied with the interface box.

Operating Instructions

1. Software

Use the Zarlink Semiconductor synthesiser software. Pull down the I^2C bus section menu then select the SP5769. It is suggested that the charge pump setting 130uA is used, and the reference divider is set to 32. These settings give a small loop bandwidth (i.e. 100's Hz), which allows detailed phase noise measurements of the oscillators to be taken, if desired.

2. VCO control

The two VCO's are selected by toggling port P1 on the synthesiser which in turn toggles the LOsel input of the SL1925.

VCOS is switched on (and hence VCOV off) by clicking P1 on - a tick will appear.

VCOS oscillates at twice the LO frequency (lower band) and is then divided by two to provide the required LO frequency in the range 950MHz to 1500MHz approximately.

VCOV is switched on (and hence VCOS off) by clicking P1 off - no tick.

VCOV oscillates at the LO frequency (upper band) in the range 1450MHz to 2150MHz approximatley.

3. AGC control

The AGC input of the SL1925 which determines the conversion gain should be controlled by application of an external voltage to the AGC pin, TP1.

Caution: Care should be taken to ensure the chip is powered ON when +ve voltages are applied to the AGC input so as to avoid powering the chip up via the ESD protection diode of the AGC input. It is recommended that a low current limit is set on the external source used.

4. Free running the VCO's

Select the required VCO using port P1 and then using the software choose an LO frequency which is above the maximum frequency capability of the oscillator. 3GHz is suggested for both oscillators. Under this condition the varactor control voltage is pumped to its maximum value, i.e. to the top of the band. The oscillator frequency may be manually tuned by varying the 30V supply.

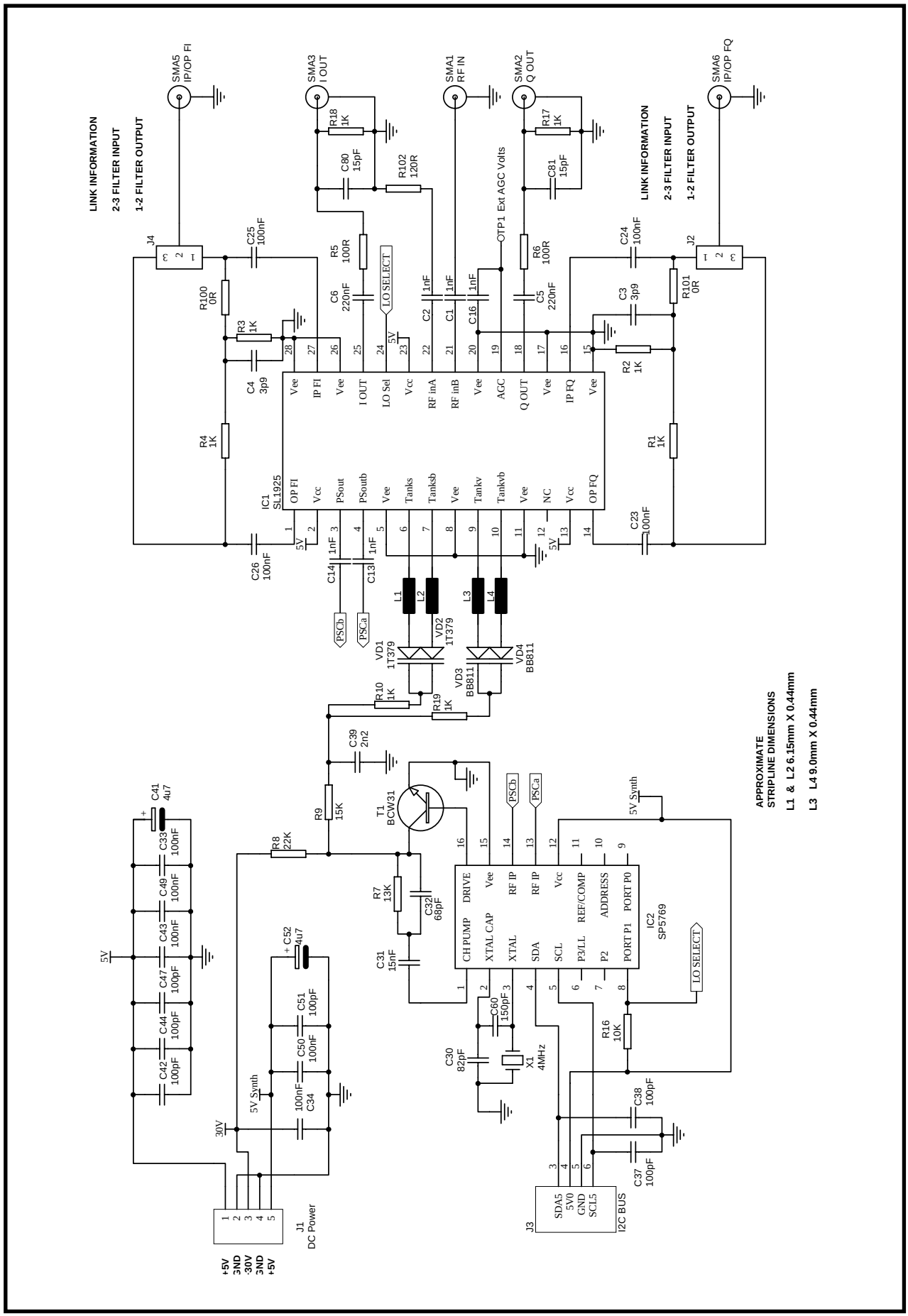

LINK INFORMATION
2-3 FILTER INPUT
1-2 FILTER OUTPUT
SMA5 IP/OP FI
SMA3 I OUT
SMA1 RF IN
SMA2 Q OUT
SMA6 IP/OP FQ
OTP1 Ext AGC Volts
LO SELECT
IC1 SL1925
OP FI
Vcc
PSout
PSoutb
Vee
Tanks
Tanksb
Tankv
Tankvb
NC
OP FQ
IP FI
I OUT
LO Sel
RF inA
RF inB
AGC
Q OUT
IP FQ
PSCb
PSCa
L1
L2
L3
L4
VD1 1T379
VD2 1T379
VD3 BB811
VD4 BB811
T1 BCW31
IC2 SP5769
CH PUMP
XTAL CAP
XTAL
DRIVE
RF IP
SDA
SCL
P3/LL
P2
REF/COMP
ADDRESS
PORT P1
PORT P0
X1 4MHz
J1 DC Power
J3 I2C BUS
SDA5
5V0
GND
SCL5
+5V
GND
-30V
GND
+5V
5V Synth
APPROXIMATE
STRIPLINE DIMENSIONS
L1 & L2 6.15mm X 0.44mm
L3 L4 9.0mm X 0.44mm

Figure 16

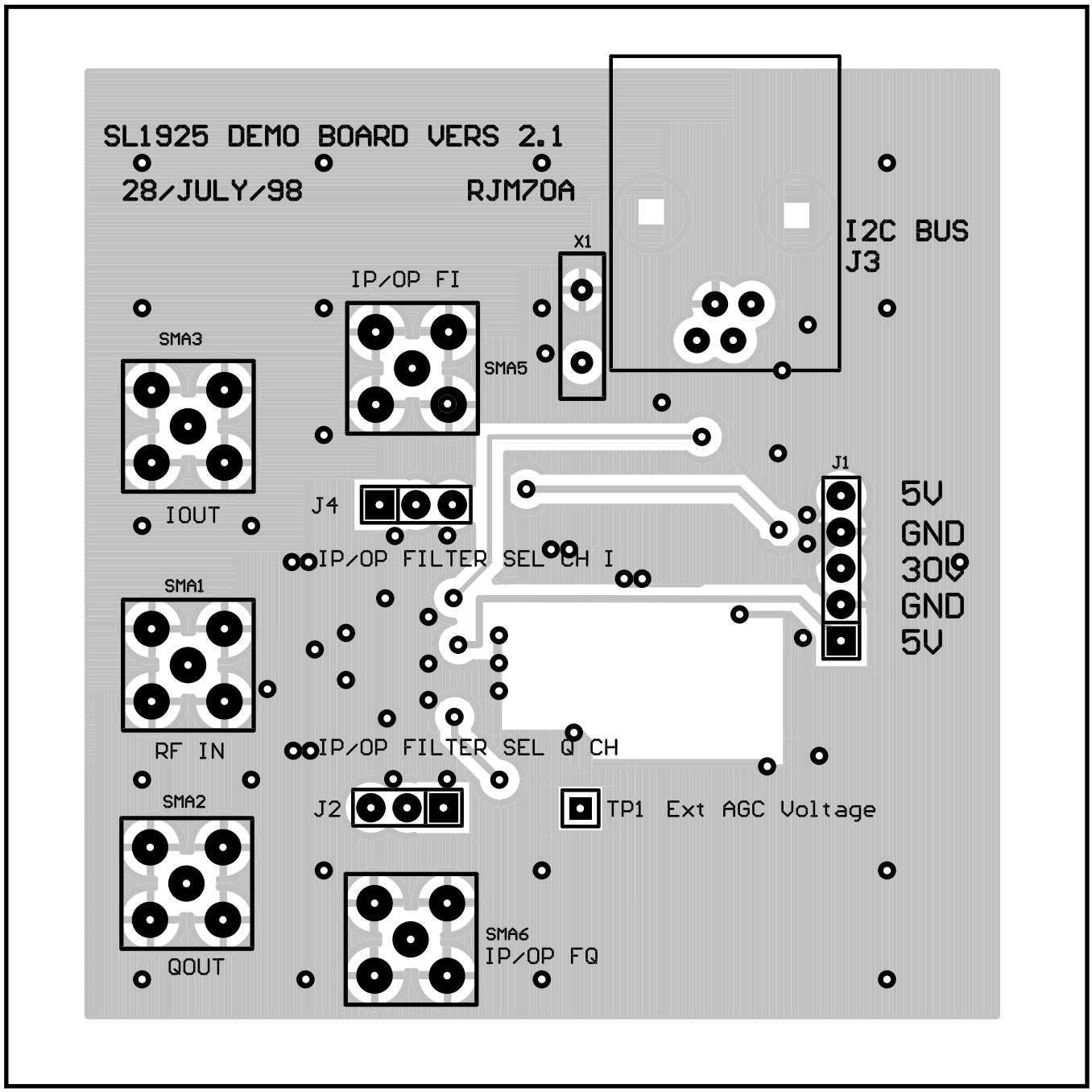


Figure 17 Top View

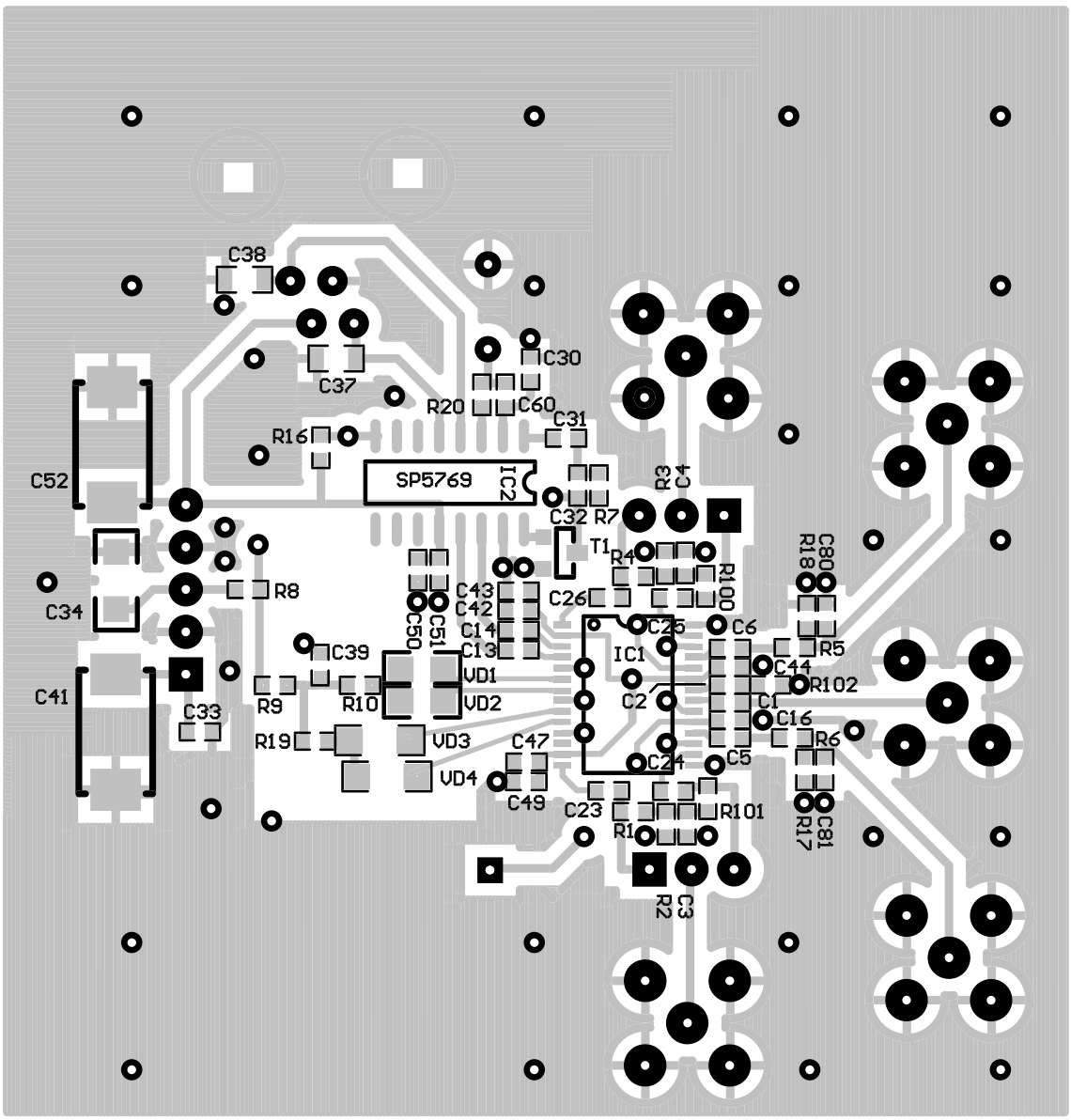
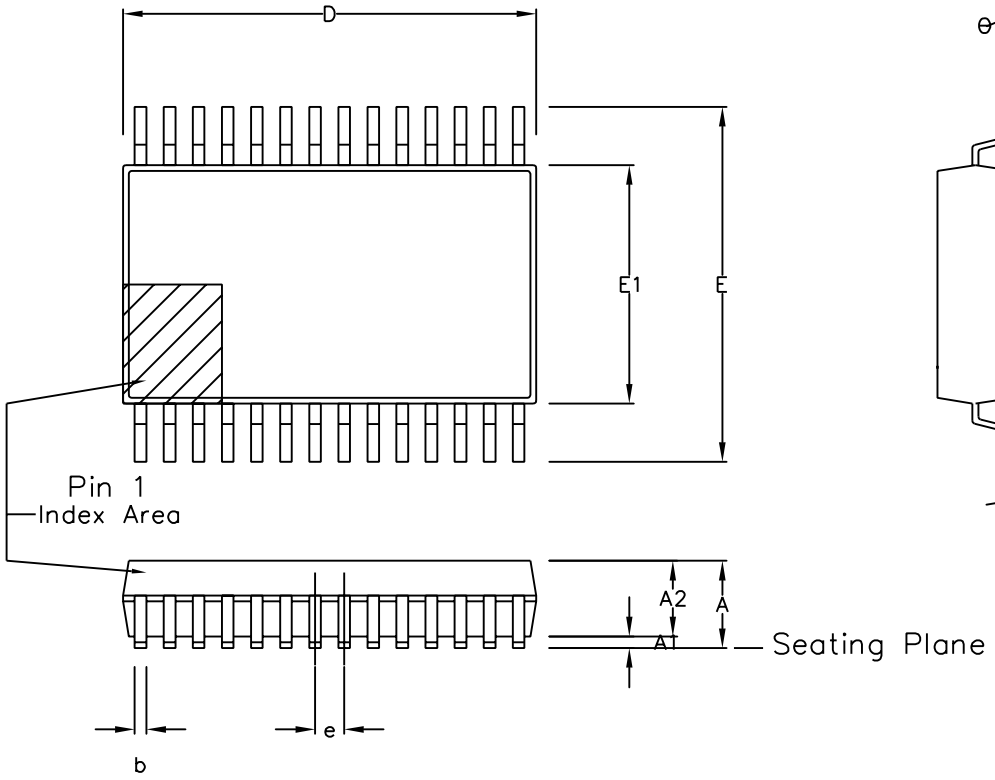


Figure 18 Bottom view



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	9.90		10.50		0.390		0.413
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	28						
Conforms to JEDEC MO-150 AH Iss. B							

This drawing supersedes:-
418/ED/51481/004 (Swindon/Plymouth)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201935	205232	212478	
DATE	27Feb97	25Sep98	3Apr02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for 28 lead SSOP (5.3mm Body Width)

GPD00296

For more information about all Zarlink products visit our Web Site at

www.zarlink.com