PM7385

FREEDM-84A672

REVISION C DEVICE ERRATA

ISSUE 5

December, 2001

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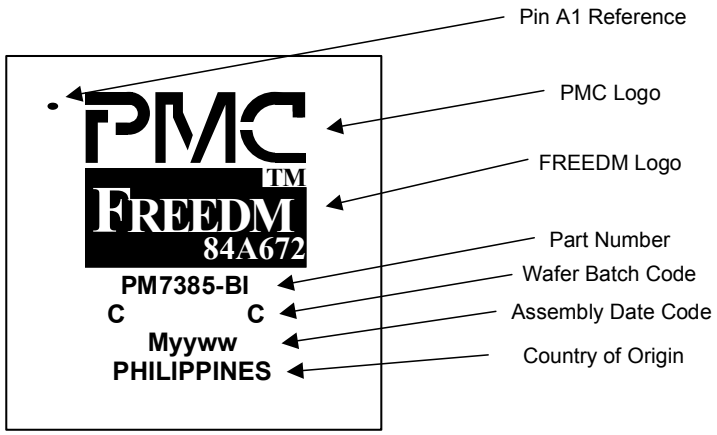
1. Introduction

In this document, Section 2 lists the known functional errata for revision C of PM7385 FREEDM-84A672 and Section 3 lists errors found in Issue 6 of the FREEDM-84A672 datasheet (PMC-1990114).

1.1. Device Identification

The information contained in Section 2 relates to Revision C of PM7385 FREEDM-84A672 only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1.1). PM7385 FREEDM-84A672 Revision C is packaged in a 352-pin Ball Grid Array (SBGA).

Figure 1.1: PM7385 FREEDM-84A672 Branding Format.



Not to Scale

1.2. Reference

- PMC-1990114, FREEDM-84A672 Long Form Data Sheet, Issue 6.

2. FREEDM-84A672 Revision C Functional Deficiency List

This section lists the known functional deficiencies for Revision C of FREEDM-84A672 (as of the publication date of this document). For each deficiency, the known work-around and the operating constraints, with and without the work-around, are also described.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

2.1. Dropped data on unchannelised DS3 SBI SPE.

Description:

When the TCAS672 block is configured to transmit a DS-3 on one of the SBI SPE's, there is a small probability that data bytes may be dropped from the transmit data stream.

Workarounds:

Carrying out the following procedure during configuration will eliminate this problem:

1. Place the SPE into T1 mode (SBI_MODE = 1 in register 440, 444 or 448 hex)

2. Wait at least 125 us

3. Place the SPE into DS-3 mode (SBI_MODE = 0 in register 440, 444 or 448 hex)

Performance with workaround:

With the extra configuration step, FREEDM-84A672 works correctly.

Performance without workaround:

Bytes of transmit data may be dropped during transfer to the SBI bus.

2.2. TEMUX loss of frame may cause data corruption.

Description:

When a link on the TEMUX loses frame, corrupted pointer information may be sent over the SBI Bus to the FREEDM, resulting in data corruption on the FREEDM.

When frame synchronization returns, the TEMUX will automatically recover and begin transmitting data to the FREEDM. However, due to the corrupted pointer information, the FREEDM may not recover and clear the data corruption in all cases.

Workarounds:

The tributaries affected by the loss of framing must be disabled in the EXSBI then reenabled following recovery of framing synchronization on the TEMUX.

Performance with workaround:

With the affected links disabled then reenabled after each failure, the FREEDM-84A672 works correctly.

Performance without workaround:

The affected links may experience data corruption.

2.3. Following recovery from receive FIFO overrun events, truncated data transfers may occur on the receive Any-PHY bus.

Description:

When outputting packets on the receive Any-PHY bus, the FREEDM-84A672 will normally transfer bursts of data containing ((XFER+1)*16) bytes, where XFER is a value between 0 and 15 configurable on a per-channel basis, or alternatively, bursts of data containing fewer bytes but including an end of packet. The Any-PHY interface is intended to operate in such a manner at all times, so that a downstream device may assume that any data transfer, in which REOP is not asserted is of a fixed length.

Following a receive FIFO overrun, however, the FREEDM-32A672 implements an automatic FIFO healing mechanism. The FREEDM-32A672 attempts to drain the overrun FIFO as quickly as possible and, once the FIFO has emptied, resets the internal FIFO control logic. While the FIFO is undergoing the healing operation, however, the FIFO control logic does not guarantee that all 'non-EOP' transfers on the Any-PHY bus are of the programmed fixed length. As a consequence, the FREEDM-32A672 may output a burst of data containing (n*16) bytes of data, where n is less than (XFER+1), but which does not include an end of packet.

After outputting the shortened burst, FREEDM-32A672 will tristate its outputs driving the receive Any-PHY bus. The downstream device, expecting all non-EOP bursts to be of length ((XFER+1)*16) bytes, will therefore read a number of non-existant words. This will manifest itself as extra bytes inserted into the HDLC packet. Depending on what termination has been applied to the Any-PHY bus (pull-ups, pull-downs, etc.), these extra bytes may be all zeros, all ones, or a repetition of the last word output by the FREEDM-32A672 on the Any-PHY bus before it tristated its outputs.

It is important to note that the FIFO healing mechanism referred to above can take some time to complete. (The time to heal is proportional to the difference in speed between the FIFO reader and FIFO writer.) As a result, there may be some delay between a FIFO overrun being reported and a truncated burst being output on the Any-PHY bus.

Workarounds:

There are 4 possible independent workarounds:

i) Set the receive path XFER to 0. All transfers not containing an end of packet will then be 16 bytes and thus of constant length. This workaround may not be suitable in high bandwidth systems, especially if multiple FREEDM-84A672s are sharing an Any-PHY bus.

ii) Attach a pull-down resistor to the RVAL output and monitor this signal to detect truncated data transfers. The pull-down resistor should be of such strength that the non-driven state of the Rx Any-PHY Bus can be detected within 16 RXCLK cycles.

iii) Attach a pull-up resistor to the RERR output and monitor this signal to detect truncated data transfers. The pull-up resistor should be of such strength that the non-driven state of the Rx Any-PHY Bus can be detected within 16 RXCLK cycles. RERR is always logic 0 when the FREEDM-84A672 is outputting data on the Any-PHY bus, except when REOP is asserted. If a pull-up resistor is attached to RERR, a truncated transfer will be indicated by RERR = 1 and REOP = 0. The downstream device can take the appropriate action such as discarding the packet.

iv) Attach pull-down or pull-up resistors to the RXDATA[15:0] outputs and a pull-down resistor to the RXPRTY output. The resistors should be of such strength that the non-driven state of the Rx Any-PHY Bus can be detected within 16 RXCLK cycles. If the FREEDM-84A672 outputs a truncated burst of data and the downstream device is not monitoring RVAL and is expecting a fixed length burst of data, the downstream device will observe parity errors and can take appropriate action such as discarding the packet.

Performance with workaround:

FREEDM-84A672 operates correctly.

Performance without workaround:

The downstream device may sample invalid packet data.

2.4. Incorrect T1 tributary CAS Phase Information may be generated on SBI Bus.

Description:

When a T1 tributary in the transmit direction is configured as a clock slave (CLK_MSTR bit in register 0x698 set to 0) and the T1 tributary is operating at a line rate faster than the FREEDM's base T1 line rate (i.e. the T1 line rate derived from REFCLK, which the FREEDM uses when a tributary is operating as a clock master), there is a risk that this condition can cause the FREEDM's Insert SBI (INSBI) block to generate incorrect Channel Associated Signalling Phase Information. This can result in a downstream transmit framer re-aligning to the incorrect signalling phase and consequently generating incorrect T1 multiframe signalling.

Workarounds:

The generation of incorrect CAS Phase Information over the SBI bus is caused by the underunning of a FIFO within the INSBI block which containing signalling information. The underrun is caused by the faster than nominal T1 tributary rate and excessive delay in responding to this by increasing the rate at which the FIFO is written to. The delay in responding can, however, be reduced by altering a FIFO threshold coefficient located in FREEDM register 0x6A4. This register (Documented in section 3.1 of this document.) defaults to the value 'xxxxxxxx00101110' after reset (i.e. the value 2E hex, with only the 8 least significant bits valid). The register should be re-programmed to the value **6E** hex after device reset. (Bits other than the 8 least significant bits can be set to any value.)

Performance with workaround:

FREEDM-84A672 operates correctly.

Performance without workaround:

Transmit T1 tributaries which are configured as clock slaves may experience T1 multiframe signalling errors if the T1 tributary is operating at a faster than nominal line rate.

2.5. Delay Required After Writes to SBI Master Configuration Registers

Description:

After a write to register 0x04C SBI ADD BUS Master Configuration a delay is required before subsequent access to this or any INSBI register is permitted. Likewise, after a write to register 0x048 SBI DROP BUS Master Configuration a delay is required before subsequent access to this or any EXSBI register is permitted.

Workarounds:

A delay should be implemented after writing to 0x04C SBI ADD BUS Master Configuration register before subsequent accesses to this or any INSBI registers. Likewise, a delay should be implemented after writing to 0x048 SBI DROP BUS Master Configuration register before subsequent accesses to this or any EXSBI registers. The wait period, in each case, must be sufficient to ensure that a C1FP pulse has occurred between the first register write and any subsequent writes.

Performance with workaround:

With the implementation of a wait period sufficient enough to ensure that a CIFP pulse has occurred between the first register write and any subsequent writes, F84A672 will work correctly even on fast micro controller accesses.

Performance without workaround:

Without the implementation of a delay, customers with fast micro controller port accesses to the FREEDM may observe corrupt packets in one or several SBI SPEs.

2.6. Reset of SBI Tributaries are Required if C1FP is Sourced Externally (such as from a TEMUX)

Description:

When the C1FP signal is supplied externally by devices such as the TEMUX or TEMUX-84, the FREEDM84's SBI Insert block may come up in a state where the framing information passed across the SBI Bus does not contain correct framing alignment. There is no means to detect this problem in the FREEDM or the attached TEMUX/TEMUX-84. This problem would be detected at the far end framer where occasion loss of frame would be detected.

Workarounds:

All SBI tributaries in use must be reset when first initialized. This requires the tributaries to be enabled, disabled, and then re-enabled after the C1FP pulse is sourced. When using the SBI Bus in asynchronous mode at least 500us should be allowed to pass after disabling a tributary to ensure the C1FP signal has been sourced at least once, prior to re-enabling the tributary.

Performance with workaround:

The framing alignment passed on the SBI bus will be correct and frame loss should not occur. As a result the FREEDM84 will operate correctly.

Performance without workaround:

The framing information passed on the SBI bus may not contain correct framing alignment. As a result, frame loss may be detected at the far end framer.

3. Documentation Errors

This section lists the known documentation errors in Issue 6 of PMC-1990114 FREEDM-84A672 Datasheet (as of the publication date of this document).

Please report any documentation errors not covered in this document to PMC-Sierra.

3.1. Addition of "SBI INSERT MIN_THR and MAX_THR for T1".

Description:

Register 0x6A4: SBI INSERT MIN_THR and MAX_THR for T1 was omitted from the Datasheet. The following text describes the register:

Register 0x6A4 : SBI INSERT MIN_THR and MAX_THR for T1

Bit	Type	Function	Default
Bit 15 to 8	R/W	Reserved	0000H
Bit 7	R/W	MIN_THR_T1[3]	0
Bit 6	R/W	MIN_THR_T1[2]	0
Bit 5	R/W	MIN_THR_T1[1]	1
Bit 4	R/W	MIN_THR_T1[0]	0
Bit 3	R/W	MAX_THR_T1[3]	1
Bit 2	R/W	MAX_THR_T1[2]	1
Bit 1	R/W	MAX_THR_T1[1]	1
Bit 0	R/W	MAX_THR_T1[0]	0

MIN_THR_T1[3:0]:

The Minimum Threshold for T1 bits (MIN_THR_T1[3:0]) specify the FIFO depth below which a positive justification on the SBI ADD bus is performed, in clock master mode, or a speed up request is made from the INSBI to the SIPO block in clock slave mode.

Note - The value of this field defaults to 2 hex after device reset, but should be set to 6 hex for correct operation with T1 tributaries. (Refer to Section 2.4 of this document for additional information.)

MAX_THR_T1[3:0]:

The Maximum Threshold for T1 bits (MAX_THR_T1[3:0]) specify the FIFO depth which when exceeded will cause a negative justification on the SBI ADD bus to be performed, in clock master mode, or a slow down request from the INSBI to the SIPO block to be made in clock slave mode. The actual Maximum threshold used is the programmed value plus sixteen.

3.2. Figure 32 in Datasheet has Signals Labeled Incorrectly

Description:

Figure 32 – Microprocessor Write Access Timing in the datasheet contains signals labeled A[7:0] and D[7:0]. These should be changed to A[11:2] and D[15:0] respectively.

3.3. PROV and DELIN bits in Register 0x204 are Write-Only

PROV and DELIN bits in Register 0x204 are write-only and not read/write. Changes to the register table are shown below.

Register 0x204 : RHDL Indirect Channel Data Register #1

Bit	Type	Function	Default
Bit 15	~~R/W~~ **W**	PROV	0
Bit 14	R/W	STRIP	0
Bit 13	~~R/W~~ **W**	DELIN	0
Bit 12	R	TAVAIL	X
Bit 11	W	Reserved	X
Bit 10	W	FPTR[10]	X
Bit 9	W	FPTR[9]	X
Bit 8	W	FPTR[8]	X
Bit 7	W	FPTR[7]	X
Bit 6	W	FPTR[6]	X
Bit 5	W	FPTR[5]	X
Bit 4	W	FPTR[4]	X
Bit 3	W	FPTR[3]	X
Bit 2	W	FPTR[2]	X
Bit 1	W	FPTR[1]	X
Bit 0	W	FPTR[0]	X

3.4. 7BIT, INVERT, CRC[1], and CRC[0] bits in Register 0x208 are Write-Only

7BIT, INVERT, CRC[1], and CRC[0] bits in Register 0x208 are write-only and not read/write. Changes to the register table are shown below.

Register 0x208 : RHDL Indirect Channel Data Register #2

Bit	Type	Function	Default
Bit 15	~~R/W~~ **W**	7BIT	0
Bit 14	R/W	PRIORITY	0
Bit 13	~~R/W~~ **W**	INVERT	0
Bit 12		Unused	X
Bit 11	~~R/W~~ **W**	CRC[1]	0
Bit 10	~~R/W~~ **W**	CRC[0]	0
Bit 9	R/W	OFFSET[1]	0
Bit 8	R/W	OFFSET[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	XFER[3]	0
Bit 2	R/W	XFER[2]	0
Bit 1	R/W	XFER[1]	0
Bit 0	R/W	XFER[0]	0

4. Contacting PMC-Sierra

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Issue date: December, 2001