PM7350

S/UNI™ DUPLEX

DSLAM REFERENCE DESIGN:

WAN CARD

RELEASED

ISSUE 3:NOVEMBER 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
3	Nov 2000	Updated list of references. Included latest errata.
2	February 2000	Document updated to reflect removal of jitter attenuation circuitry.
1	August 1999	Document created.

CONTENTS

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1 FEATURES

The DSLAM WAN Card has the following features:

- Demonstrates the WAN Card portion of the DSLAM Reference Design.
- Demonstrates the circuitry necessary to interface UTOPIA Level 2 devices to the S/UNI-DUPLEX.
- An embedded inter-device communications channel, allowing devices on the Core Card to communicate with devices on the WAN Card.
- A high speed LVDS interface:
    - Data rates up to 200 Mb/s
    - Manually selectable for transmission over a backplane or through cables.
    - Supports 1:1 protection switching
- 4 DS-3 interfaces to transport ATM over DS-3 to and from the network.
- Clock synchronization to the DS-3 network, or from the line side interface (via the DSLAM Line and Core cards).
- Front panel status LEDs to indicate:
    - Power Supply status
    - LVDS signal status
    - S/UNI-QJET Framer Status for each DS-3 port
- Onboard hot swap controller to monitor current flow onto the board for live insertion and extraction.
- CompactPCI (cPCI) compatability.

2 REFERENCES

1. PCI Industrial Computers Manufacturers Group (PICMG), “CompactPCI Specification 2.0 R 2.1”, Wakefield MA, September 1997.

2. PMC-Sierra Inc., PMC-1981025, “S/UNI-VORTEX and S/UNI-DUPLEX Technical Overview”, June 1999, Issue 2.

3. PMC-Sierra Inc., PMC-1980581, “S/UNI-DUPLEX Dual Serial Link PHY Multiplexer Data Sheet”, April 2000, Issue 5.

4. PMC-Sierra Inc., PMC-1960835, “S/UNI-QJET Long Form Data Sheet”, July 1999, Issue 6.

5. PMC-Sierra Inc., PMC-1990357, “DSLAM Reference Design: System Design”, July 2000, Issue 3.

6. PMC-Sierra Inc., PMC-1990815, “DSLAM Reference Design: Core Card”, July 2000, Issue 3.

7. PMC-Sierra Inc., PMC-1990354, “DSLAM Reference Design: Line Card”, July 2000, Issue 3.

8. PMC-Sierra Inc., PMC-1950946, “Interfacing the D3MX to the SSI 78P7200 DS-3 LIU”, September, 1995, Issue 1.

3 OVERVIEW

3.1 Scope

The purpose of this reference design is to assist engineers in designing their products using PMC-Sierra's S/UNI-DUPLEX device.

The DSLAM Reference Design is composed of the following four main documents:

1. DSLAM Reference Design: System Design
2. DSLAM Reference Design: Core Card
3. DSLAM Reference Design: WAN Card
4. DSLAM Reference Design: Line Card

The DSLAM Reference Design: System Design document provides an overview of the DSLAM Reference Design system architecture. The remaining documents describe the functionality and implementation specific details for each individual card.

This document only describes the design for the DSLAM WAN card.

A block diagram is shown for the design. A description is then given for the functional blocks of the design. A detailed implementation description then follows.

4 HIGH LEVEL DESIGN

The block diagram of the WAN Card reference design is shown in Figure 1.

As can be seen, the design consists of the following functional blocks:

- S/UNI-DUPLEX
- S/UNI-QJET
- Microprocessor block
- Power block
- Clock distribution block
- UTOPIA Bus Interface
- DS-3 Line Interface
- Compact PCI Interface
- Front Panel Interface

Figure 1 on the next page indicates that the LVDS lines are jumper configurable for transmission over the backplane or via cables connected to the front panel. LVDS over the backplane is used on single shelf systems, whereas multi-shelf systems will require the use of the front panel LVDS interface. The reference design will also support a mix of LVDS over backplane and LVDS over cables.

The WAN Card design will be based on the Compact PCI 6U (233.35mm by 160mm) board size. The board will connect to the system backplane via connector J1, and to the DSLAM backplane via connector J5. The DSLAM reference design supports location independence for the WAN Card, allowing it to be placed in any slot, if the host CPU is not present. If the host CPU is present, WAN Cards will usually reside in slots 7 and 8. The board will support hot swapping, allowing the board to be inserted or removed from a live system.

The following sections describe each of the above blocks in further detail.

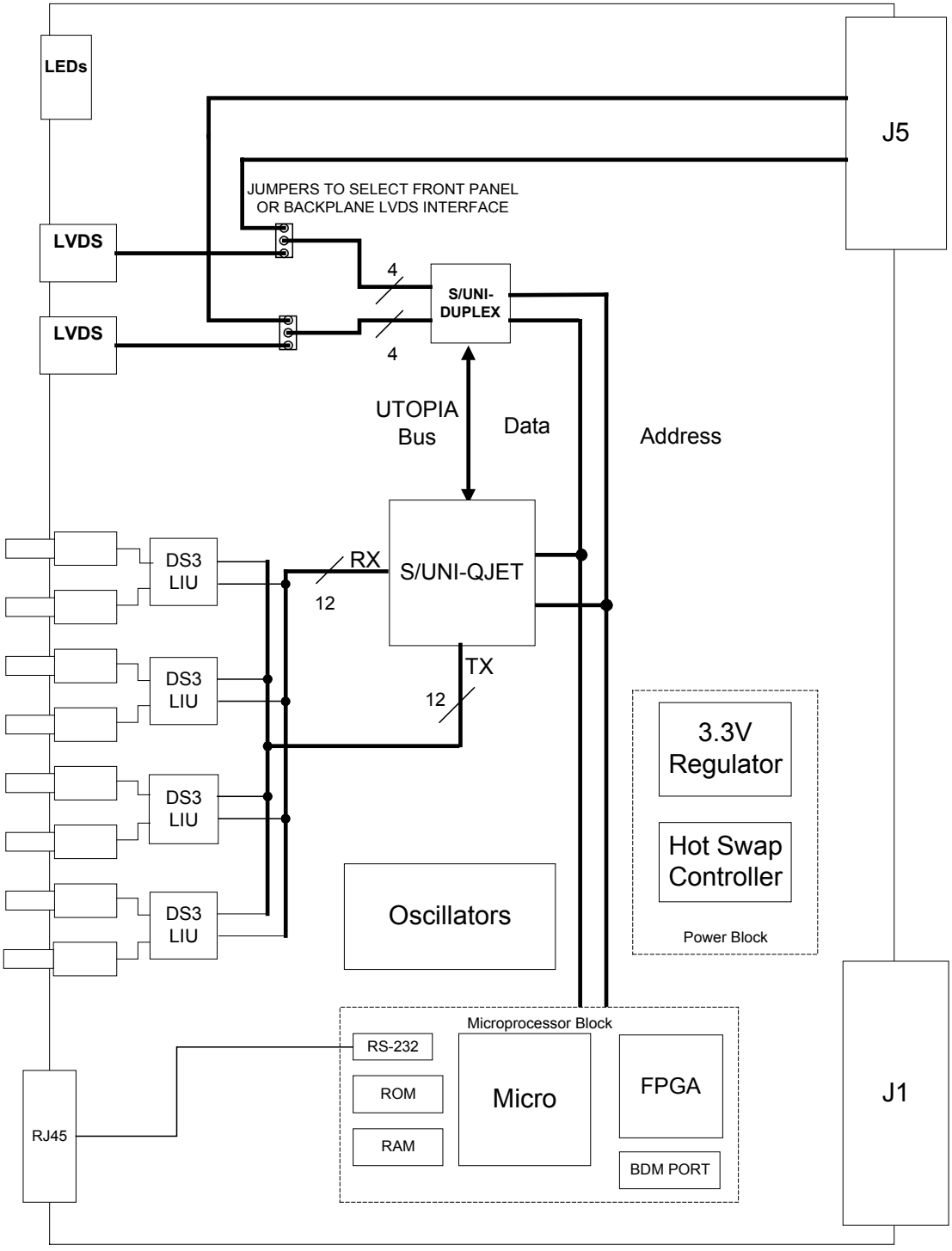


Figure 1. WAN Card Block Diagram.

4.1 S/UNI-DUPLEX

The S/UNI-DUPLEX provides a UTOPIA L2 interface or a clocked serial data interface. The design contained in this document utilizes the UTOPIA Level 2 Interface. Please refer to the DSLAM Line Card reference design [7] for an application utilizing the clocked serial data interface.

4.1.1 S/UNI-DUPLEX Functional Description

The PM7350 S/UNI-DUPLEX is a monolithic integrated circuit typically used for traffic concentration within a Digital Subscriber Line Access Multiplexer (DSLAM).

The device is ATM specific. It exchanges contiguous 53 byte cells with PHY devices. The PHY interface can be either clocked serial data or a parallel bus.

The S/UNI-DUPLEX supports three different parallel bus specifications. These are:

Utopia Level 2 – The industry standard ATM Forum PHY to ATM layer bus specification. Also referred to as Utopia L2. It is available from the ATM Forum web site at www.atmforum.com.

SCI-PHY Level 2 – Also referred to as SCI-PHY L2. PMC-Sierra's superset extension to the Utopia bus specification to allow the following enhancements:

- 32 PHY maximum instead of 31.
- Extended cells: SCI-PHY supports user defined bytes prepended or postpended to the standard 53 byte cells allowed by Utopia. This particularly useful when switching tags are to be attached to the cell by an ATM layer device such as the S/UNI-ATLAS. SCI-PHY allows cells to be up to 64 bytes long.

ANY-PHY – PMC-Sierra's extension to the Utopia bus specification to allow the following enhancements:

- Addressing for an unlimited number of logical PHYs.
- Fixed cell or arbitrary length packet transfers. Only cell mode transfers are used by the S/UNI-VORTEX and S/UNI-DUPLEX.

- Extended cells: This includes optional prepend or postpend cell extensions plus the additional overhead bytes used for in-band PHY addressing and selection.

- In the transmit direction, separation of PHY status polling (using bus pins) from PHY selection during start of cell or packet transfer (using in-band addressing).

- In the receive direction, cell overhead bytes can be used to identify the source PHY of the cell.

- Relaxed decode response time to simplify device status polling circuitry.

With a SCI-PHY master interface, the S/UNI-DUPLEX coordinates cell exchanges with up to 32 PHY devices. In the upstream direction, the PHY devices are polled in a pure round robin manner and cells are queued in two cell FIFOs dedicated to each PHY device. In the downstream direction, the cell buffer is logically partitioned into a four cell FIFO for each PHY device to avoid head-of-line blocking. Those PHY devices associated with non-empty FIFOs are polled round robin.

The SCI-PHY/Any-PHY interface may also be configured as a bus slave to support various card interconnection scenarios. The output port appears as a single addressable SCI-PHY Level 2 or Any-PHY slave that respects the receive protocol. The S/UNI-DUPLEX autonomously multiplexes the traffic from up to 32 logical channels and presents it as a single cell stream. A prepended word identifies the logical channel. The input port presents itself as 32 PHY entities, each of which can be polled to determine availability of empty cell buffers. Logical channel selection can occur either through presentation of the logical channel's index on IADDR[4:0] or through encoding of the index in a prepended word.

Regardless of the PHY interface configuration, all cell streams are multiplexed into a high-speed serial stream. The high-speed interfaces use NRZ data-only differential signals compatible with LVDS levels. The internal transmit clock is synthesized from a lower frequency reference. An extended cell format provides four extra bytes for the encoding of flow control, timing reference, PHY identification and link maintenance information. A redundant link is provided to allow connection to two cell processing cards.

A microprocessor port provides access to internal configuration and monitoring registers. The port may also be used to insert and extract cells in support of a control channel.

For further information, please see the S/UNI-DUPLEX Datasheet PMC-1980581 [3].

4.1.2 S/UNI-DUPLEX in the WAN Card

The S/UNI-DUPLEX on the DSLAM WAN Card operates in a fully UTOPIA L2 master mode. A demonstration of the S/UNI-DUPLEX in slave mode is shown in the DSLAM Reference Design: Core Card document [6].

In the upstream direction (from the core card to the WAN), the S/UNI-DUPLEX receives high speed data from the core card via the LVDS links. Both links are available over the system backplane, or via firewire connectors on the front panel. The S/UNI-DUPLEX, acting as the bus master, then sends ATM cells over the UTOPIA bus to the S/UNI-QJET.

In the downstream direction (from the WAN via the S/UNI-QJET to the core card), the S/UNI-DUPLEX receives ATM cells from the S/UNI-QJET over the UTOPIA bus. The S/UNI-DUPLEX then sends the data over the active LVDS link to the core card.

The S/UNI-DUPLEX should be configured to operate with scrambled cells, and perform cell delineation by HEC.

4.2 S/UNI-QJET

The S/UNI-QJET is configured as an ATM PHY device for the WAN Card Reference design.

4.2.1 S/UNI-QJET Functional Description

The PM7346 S/UNI-QJET is a quad ATM physical layer processor with integrated DS-3, E3, and J2 framers. PLCP sublayer DS1, DS-3, E1, and E3 processing is supported as is ATM cell delineation.

The S/UNI-QJET contains integral DS-3 framers, which provide DS-3 framing and error accumulation in accordance with ANSI T1.107, and T1.107a, integral E3 framers, which provide E3 framing in accordance with ITU-T Recommendations G.832 and G.751, and integral J2 framers, which provide J2 framing in accordance with ITU-T Recommendation G.704 and I.432.

When configured for DS-3 transmission system sublayer processing, the S/UNI-QJET accepts and outputs both digital B3ZS-encoded bipolar and unipolar signals compatible with M23 and C-bit parity applications.

In the DS-3 receive direction, the S/UNI-QJET frames to DS-3 signals with a maximum average reframe time of 1.5 ms and detects line code violations, loss of signal, framing bit errors, parity errors, path parity errors, AIS, far end receive failure and idle code. The DS-3 overhead bits are extracted and presented on serial outputs. When in C-bit parity mode, the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channels are extracted. HDLC receivers are provided for Path Maintenance Data Link support. In addition, valid bit-oriented codes in the FEAC channels are detected and are available through the microprocessor port.

Error event accumulation is also provided by the S/UNI-QJET. Framing bit errors, line code violations, parity errors, path parity errors and far end block errors are accumulated, when appropriate, in saturating counters for DS-3, E3, and J2 frames. Loss of Frame detection for DS-3, E3, and J2 is provided as recommended by ITU-T G.783 with integration times of 1ms, 2ms, and 3ms.

In the DS-3 transmit direction, the S/UNI-QJET inserts DS-3 framing, X and P bits. When enabled for C-bit parity operation, bit-oriented code transmitters and HDLC transmitters are provided for insertion of the FEAC channels and the Path Maintenance Data Links into the appropriate overhead bits. Alarm Indication Signals can be inserted by using internal register bits; other status signals such as the idle signal can be inserted when enabled by internal register bits. When M23 operation is selected, the C-bit Parity ID bit (the first C-bit of the first M sub-

frame) is forced to toggle so that downstream equipment will not confuse an M23-formatted stream with stuck-at 1 C-bits for C-bit Parity application.

The S/UNI-QJET also supports diagnostic options which allow it to insert, when appropriate for the transmit framing format, parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, all-zeros, AIS, Remote Alarm Indications, and Remote End Alarms.

The S/UNI-QJET provides cell delineation for ATM cells using the PLCP framing format, or by using the header check sequence octet in the ATM cell header as specified by ITU-T Recommendation I.432. DS1, DS-3, E1 and E3 based PLCP frame formats can be processed. Non-PLCP-based cell delineation is accomplished with either bit, nibble, or byte-wide search algorithms, depending on the line interface used. An interface consistent with the generic physical interface defined by ITU-T Recommendation I.432 is provided for arbitrary rates up to 52 Mbit/s. This interface is used to provide physical layer support for transmission systems that do not have an associated PLCP sublayer, or to provide an efficient means of directly mapping ATM cells to existing transmission system formats (such as DS-3 and DS1).

In the PLCP receive direction, framing, path overhead extraction and cell extraction is provided. BIP-8 error events, frame octet error events and far end block error events are accumulated.

In the PLCP transmit direction, the S/UNI-QJET provides overhead insertion using inputs or internal registers, DS-3 nibble and E3 byte stuffing, automatic BIP-8 octet generation and insertion and automatic far end block error insertion. Diagnostic features for BIP-8 error, framing error and far end block error insertion are also supported.

In the cell receive path, idle cells may be dropped according to a programmable filter. By default, incoming cells with single bit HCS errors are corrected and written to the FIFO buffer. Optionally, cells can be dropped upon detection of a HCS error. Cell delineation may optionally be disabled to allow passing of all cells, regardless of cell delineation status. The ATM cell payloads are optionally descrambled. ATM cell headers may optionally be descrambled (for use with PPP packets). Assigned cells containing no detectable HCS errors are written to a FIFO buffer. Cells data is read from the FIFO using a synchronous 50 MHz 8-bit wide or 16-bit wide SCI-PHY^{TM} and Utopia Level 2 compatible interface. Cell data parity is also provided. Counts of error-free assigned cells, and cells containing HCS errors are accumulated independently for performance monitoring purposes.

In the cell transmit path, cell data is written to a FIFO buffer using a synchronous 50 MHz 8-bit wide or 16-bit wide SCI-PHY^{TM} compatible interface. Cell data

parity is also examined for errors. Idle cells are automatically inserted when the FIFO contains less than one full cell. HCS generation, cell payload scrambling, and cell header scrambling (for use with PPP packets) are optionally provided. Counts of transmitted cells are accumulated for performance monitoring purposes.

Both receive and transmit cell FIFOs provide buffering for four cells. The FIFOs provide the rate matching interface between the higher layer ATM entity and the S/UNI-QJET.

The S/UNI-QJET is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be identified, acknowledged, or masked via this interface.

For further information, please see the S/UNI-QJET Datasheet PMC-1960835 [4].

4.2.2 S/UNI-QJET in the WAN Card

In the upstream direction (from the WAN card to the WAN), the S/UNI-QJET will receive ATM cells from the S/UNI-DUPLEX over the UTOPIA Bus (see section 4.7). The S/UNI-QJET then sends DS-3 frames to the line interface unit.

In the downstream direction, the S/UNI-QJET receives DS-3 frames from the line interface unit, and then sends ATM cells over the UTOPIA bus to the S/UNI-DUPLEX.

The S/UNI-QJET should be configured to operate with scrambled cells, and perform cell delineation by HEC.

4.3 Microprocessor Block

The on board microprocessor is used to monitor and control the S/UNI-DUPLEX and S/UNI-QJET devices. It should provide the following features:

- 8-bit data bus
- Interrupt controller
- Programmable Chip Selects
- Address decoder
- Serial interface
- Background Debug Module

The Motorola MC68340 was chosen for this reference design.

A block diagram of the microprocessor, with associated RAM and ROM, is shown in Figure 2. The FPGA will decode chip selects for the S/UNI-DUPLEX and S/UNI-QJET, and will perform the multiplexing function found in the clock distribution block, (see Section 4.4). The VHDL code for the FPGA can be found in Appendix D.

The DSLAM WAN Card will make use of the programmable nature of the active low chip selects provided by the 68340 microprocessor. A base address register for each chip select programs the base address, while an address mask register sets the block size (from 256 bytes to 4 Gbytes in 2^N increments) and the port size (8 or 16 bits).

The microprocessor will provide the signals listed in Table 1 to the FPGA.

Table 1. Microprocessor signals.

SIGNAL	NAME	DESCRIPTION/USE
A_M<7..0>	Address Bus	Bits 7 down to 0 are used to address the internal registers of the FPGA. These bits are not buffered prior to reaching the FPGA.
A_M<17..15>	Address Bus	Bits 17 down to 15 are used to select between the S/UNI-DUPLEX, S/UNI-QJET, and the FPGA's internal registers. These bits are not buffered prior to reaching the FPGA.
D<7..0>	Data Bus	Data bus bits 7 down to 0 are used to write to the

SIGNAL	NAME	DESCRIPTION/USE
		internal registers of the FPGA.
CS0B	Chip Select 0	Active Low Chip Select 0 is used in two ways: 1) Operation from PROM: The microprocessor asserts CS0B (which selects the PROM) for every address after a reset occurs, until the V-Bit is set in the CS0B base address register. 2) Operation from Debug (BDM) Port: The FPGA uses CS0B and CS1B to select either the most significant byte SRAM or the least significant byte SRAM.
CS1B	Chip Select 1	The microprocessor asserts CS1B to read from or write to SRAM. The actual SRAM selected is determined by the setting of the SIZ0 and A0 bits. When operating from the Debug (BDM) port, CS1B is combined with CS0B to select the SRAM.
CS2B	Chip Select 2	The microprocessor asserts CS2B to select either the S/UNI-QJET, S/UNI-DUPLEX, or FPGA.
DSB	Data Strobe	Active low Data Strobe is asserted by the microprocessor in a read cycle to signal to the external device to place data on the bus. In a write cycle, DSB indicates to the external device that the data on the bus is valid.
ASB	Address Strobe	Active low Address Strobe is asserted by the microprocessor to indicate to external devices that the address and bus control signals are valid.
SIZ0	Transfer Size 0	SIZ0 indicates the size of the current transfer. If 1, the bus transfer consists of 1 byte. If 0, the transfer is 1 word (16 bits).
R/WB_M	Read/ Write	When 0, a write operation is taking place, when 1, a read operation is occuring.

It should be restated that the data bus is 16 bits. Therefore, care must be taken to ensure that bus transfers occur on the proper word or byte boundary. When A0 is low, the address is even and a byte and word boundary is selected. When high, it is a byte boundary only. Word transfers may only occur on word boundaries (when A0 is low). In addition, the 8 bit data ports of the S/UNI-QJET and S/UNI-DUPLEX must interface to the microprocessor on data bits 15 through 8 due to the dynamic bus sizing nature of the 68340.

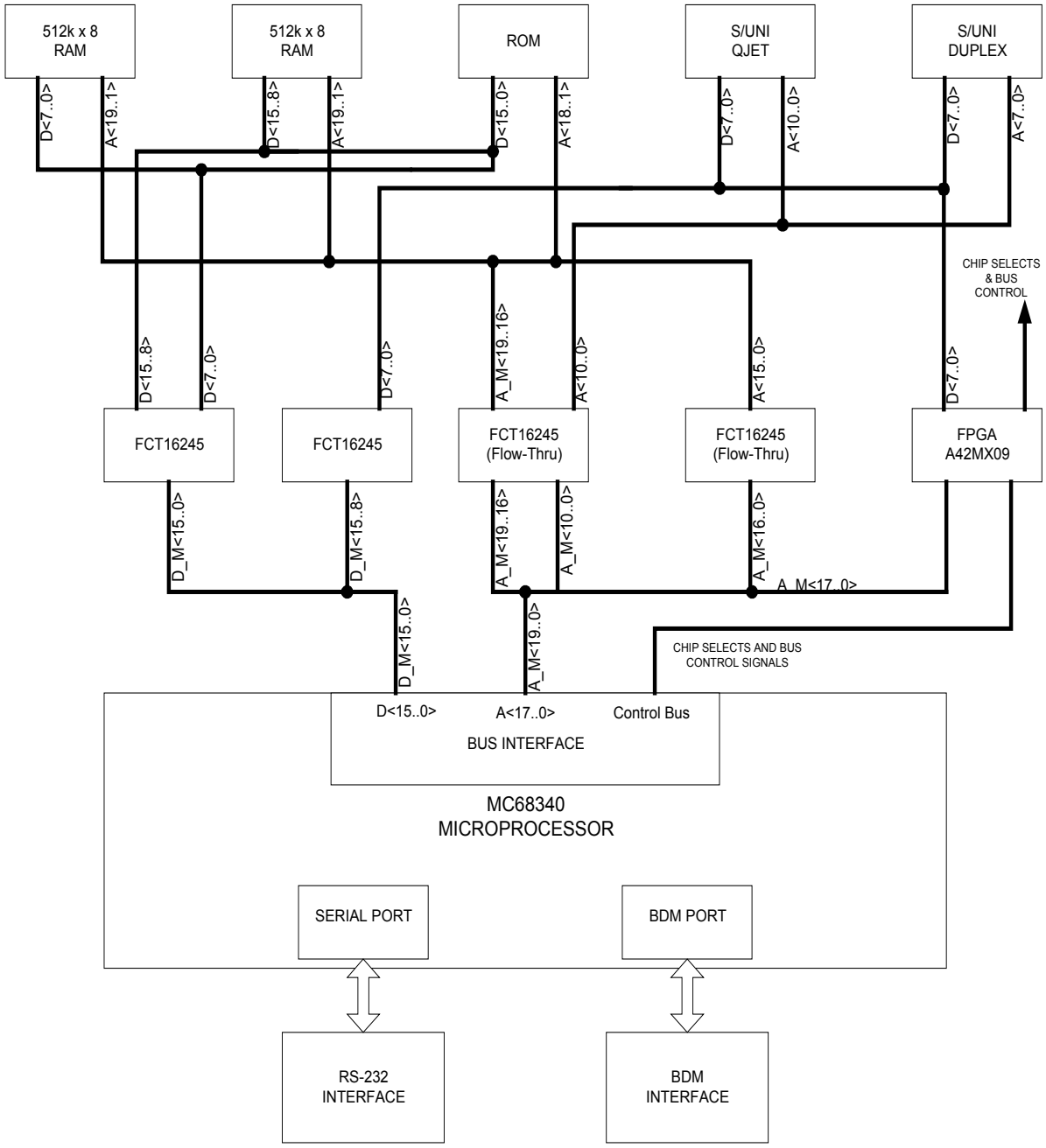


Figure 2. Microprocessor with Memory System

4.4 Clock Distribution Block

4.4.1 Oscillators

The S/UNI-DUPLEX requires one jitter-free clock input for REFCLK. It is used as the reference clock by both clock recovery and clock synthesis circuits. The high-speed serial interface bit rate is eight times the REFCLK frequency. Therefore, for a bit rate of 200Mbps, REFCLK must be 25 MHz. This clock signal is provided by a 25 MHz oscillator.

The Microprocessor Block requires two oscillators. A 25 MHz clock is needed for the processing core. The microprocessor block also requires a 3.6864 MHz clock for the serial interface.

Note the use of two different 25 MHz clock oscillators (for the microprocessor and the S/UNI-DUPLEX). This is so that the 25 MHz REFCLK signal to the S/UNI-DUPLEX can be varied for testing and demonstration purposes (by using an oscillator of a different frequency) without affecting the clock signal to the microprocessor block. By varying the REFCLK frequency, different bit rates are generated over the LVDS interface.

The UTOPIA bus may be timed using either a 25 MHz or 50 MHz oscillator. For this reference design, a 25 MHz UTOPIA bus was selected. The UTOPIA bus clock signals are buffered prior to the S/UNI-DUPLEX and S/UNI-QJET because the S/UNI-QJET does not have 5V tolerant RFCLK and TFCLK pins.

The FPGA is used to implement and control the multiplexing of both 8kHz reference clocks as well as 44.736MHz references. (See Figure 3)

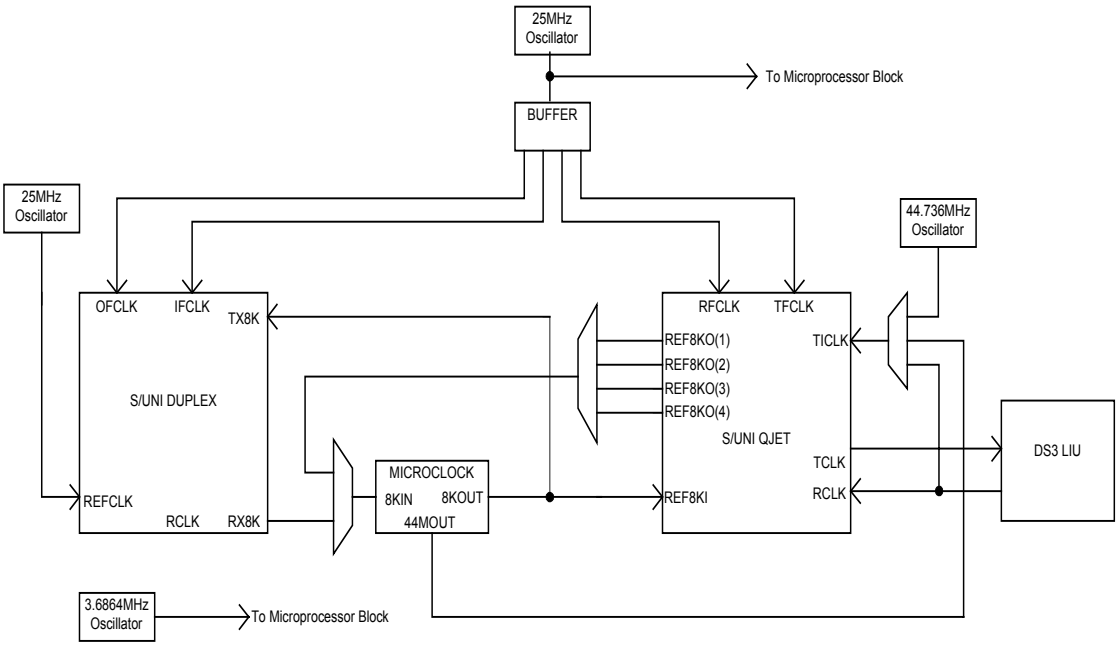


Figure 3. Timing Distribution on the WAN Card

4.4.2 8kHz multiplexing

The SUNI-DUPLEX provides an input pin and output pin, which can be used to distribute low speed reference clocks between cards. In communications equipment this is typically an 8 kHz clock used for timing PCM voice circuitry. The reference clock's rising edge is encoded and carried through each of the serial links in the system overhead. A simple byte marker is included in the system prepend byte in each cell carried over the serial link. This marker identifies the nearest byte boundary that aligns with the most recent rising clock edge. The receiving device pulses its corresponding clock output pin at the appropriate byte boundary.

This approach allows the reference clock to be an arbitrary frequency and yet be carried in-band independent of the serial link's bit rate. However it has limitations that must be accounted for. For example, timing jitter will occur due to the edge encoding scheme. For systems with protection switching, the reference clock on the line card will experience a temporary perturbation as the S/UNI-DUPLEX switches active links. Also, although they will be very rare, cell errors over the serial link could cause a clock edge to be missed. Hence for most applications

the designer will want to consider using an external PLL to clean up the reference clock.

The MK2049 is a PLL based clock synthesizer that generates T1, E1, DS-3, E3, and OC3 frequencies on receipt of an 8 kHz signal. The MK2049 also provides an ideally jitter free 8 kHz clock output. The input signal to the MK2049 can come from two possible sources (depending on the setting of a multiplexer):

1. The 8 kHz output reference of the S/UNI-DUPLEX
2. One of four 8 kHz output references from the S/UNI-QJET

An additional multiplexer selects which 8 kHz reference output from the S/UNI-QJET is provided to the aforementioned multiplexer. This signal can be selected from four possible sources:

1. The REF8KO<1> output of the S/UNI-QJET
2. The REF8KO<2> output of the S/UNI-QJET
3. The REF8KO<3> output of the S/UNI-QJET
4. The REF8KO<4> output of the S/UNI-QJET

This allows the 8 kHz timing reference to be synchronized to the network (via the S/UNI-QJET 8 kHz signals), or from timing distributed from the Core Card via the S/UNI-DUPLEX.

4.4.3 44.736MHz Multiplexing

The TICLK input to the S/UNI-QJET is used to provide a timing source for the TCLK output. There are 4 TICLK inputs to the QJET; one for each channel. The TICLK inputs to the S/UNI-QJET can independantly be fed from 3 possible sources:

1. Looped RCLK signal from the DS-3 LIU. The RCLK option allows the S/UNI-QJET timing to be synchronized to the DS-3 network.
2. The 44.736 MHz output from the MK2049 used to dejitter the 8kHz reference clock.
3. A 44.736 MHz on-board oscillator to provide for a local timing option.

4.5 Field Programmable Gate Array (FPGA)

As mentioned previously, the FPGA will be used to generate chip selects for the various devices on the micro bus, including the two SRAMs, PROM, the S/UNI-DUPLEX, and the S/UNI-QJET. In addition, the FPGA will play a critical role in the clock source and selection process.

The FPGA will contain the multiplexers indicated in Figure 3. The selection control signals for the multiplexers will be implemented via registers within the FPGA. The registers will be set via the on board microprocessor, allowing source selection to be made under the following situations (if implemented in software):

- Through control information transmitted from the Core Card via the embedded inter-device communications channel of the S/UNI-DUPLEX.
- Through the front panel serial interface.
- Through clock selection algorithms within the software of the 68340 microprocessor.

To accomplish this functionality, the microprocessor data, address, and control bus must interface to the FPGA. The FPGA, on receipt of the signals from the microprocessor listed in Table 1, will provide the signals listed in Table 2

Table 2. Signals generated by the FPGA.

Signal	Name	Description
DEB_MEM	Active Low Memory Device Enable	DEB_MEM will be generated by the FPGA to allow access to the PROM or SRAMs
RDB	Active Low Read Enable	Read Enable signal required by the S/UNI-QJET and S/UNI-DUPLEX
WRB	Active Low Write Enable	Write Enable signal required by the S/UNI-DUPLEX and S/UNI-QJET.
CSB_QJET	Active Low Chip Select	Chip Select signal for the S/UNI-QJET. The signal is low when A_M<17..15> are 010.
CSB_DUPLEX	Active Low Chip Select	Chip Select signal for the S/UNI-DUPLEX. The signal is low when A_M<17..15> are 100.
UWEB	Upper SRAM Write Enable	Active Low Write Enable signal for the most significant byte SRAM.
LWEB	Lower SRAM Write Enable	Active Low Write Enable signal for the least significant byte SRAM
OEB	Active Low	Output Enable signal for the SRAM devices.

Signal	Name	Description
	Output Enable	

Figure 4 presents a block diagram of the circuitry within the FPGA. VHDL code for the FPGA can be found in Appendix D.

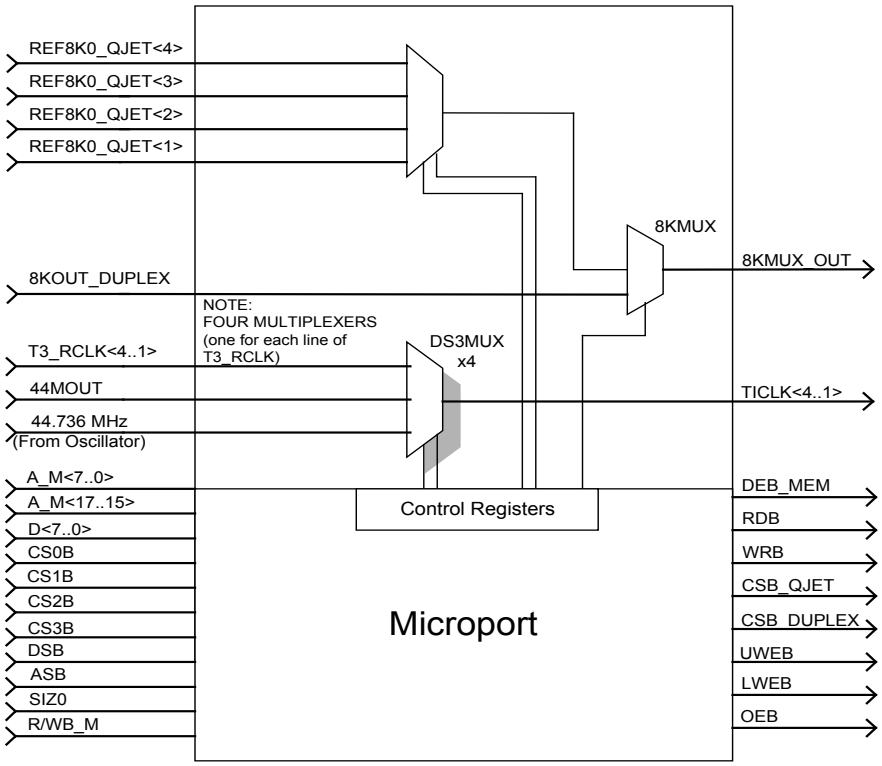


Figure 4. Block Diagram of the FPGA.

The FPGA will support the following clock selection registers:

Table 3. TICLK Selection Register (0x00h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Line4_B	Line4_A	Line3_B	Line3_A	Line2_B	Line2_A	Line1_B	Line1_A

LineX_B and LineX_A together determine the source of the clock signal output on the TICLK pin for LineX. The following table (Table 4) lists the possible choices:

Table 4. Clock Selection options for the TICLK register.

LineX_B	LineX_A	CLOCK SOURCE SELECTED
0	0	Looped T3_RCLK signal (44.736 MHz)
0	1	44MOUT signal from PLL
1	0	44.736 MHz from onboard oscillator.
1	1	No clock selected. TICLK is held high impedance.

The following register determines the distribution of the 8 kHz clock throughout the WAN Card.

Table 5. 8 kHz Selection Register (0x01h).

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
8KMUX	X	X	X	X	X	REF8K_B	REF8K_A

Where X is a don't care. The REF8K_X bits determine which of the S/UNI-QJET 8 kHz reference signals is passed to the 8KMUX multiplexer. The 8KMUX bit determines which 8 kHz reference signal is passed to the MK2049 PLL.

Table 6. REF8K0 Clock Selection Options.

REF8K_B	REF8K_A	REF8KO 8 KHZ CLOCK SOURCE SELECTED
0	0	REF8K0_QJET<1>
0	1	REF8K0_QJET<2>
1	0	REF8K0_QJET<3>
1	1	REF8K0_QJET<4>

Table 7. 8KMUX Clock Selection Options.

8KMUX	8 KHZ CLOCK SOURCE SELECTED
0	Chosen 8 kHz output reference from the S/UNI-QJET (based on bits REF8K_A & REF8K_B)
1	8 kHz output reference from the S/UNI-DUPLEX

4.6 Power Block

The WAN Card Reference Design will require both +5V and +3.3V voltage supplies. The system back plane will provide the +5V to the board, while the +3.3V will be derived from the +5V supply through the use of the LT1528 Low Dropout Voltage Regulator. The LT1528 is capable of supplying a current of up to 3A. The S/UNI-QJET, and S/UNI-DUPLEX will reside on the +3.3V power supply, while the MC68340 and the majority of the glue logic will be powered from the +5V supply.

When a board is plugged into a backplane, large transient currents can be drawn to charge up the bypass capacitors on the board. This can cause the voltage from the power supply to dip. The dip in voltage levels can cause other boards in the system to reset. Also, the connector pins may be damaged because they are not able to handle the large currents.

The solution is to use an N-channel pass transistor to ramp up the supply voltage in a controlled manner. A hot swap controller, the LTC1422 in this design, is used to control the gate of the N-channel transistor. By ramping the voltage at a controlled rate, the transient surge current

$$I = C * \frac{dV}{dt}$$

is controlled and limited to a safe value when the board makes connection.

The LTC1422 also has the capability to reset devices if the voltage dips below a certain programmed value. This reset is used to control the voltage regulator.

4.7 UTOPIA Bus Interface

The S/UNI-QJET interfaces with the S/UNI-DUPLEX via the UTOPIA bus. The connections are as illustrated in Figure 5. In this configuration, the S/UNI-DUPLEX is the UTOPIA bus master, and is configured for SCI-PHY operation. To accomplish this, the xMASTER, and SCIANY pins are connected to VCC, while the xANYPHY is connected to GND. Since the S/UNI-QJET only supports a UTOPIA L2 interface, the signals OSX and XAVALID of the S/UNI-DUPLEX are left unconnected, and ISX is connected to GND.

The DSLAM WAN Card will support a 25 MHz UTOPIA bus. One consideration in the UTOPIA bus interface is whether to use an 8 or 16 bit UTOPIA data bus. In this reference design, the UTOPIA bus is configured for 8 bit transfers at 25 MHz, by connecting the appropriate pins to VCC. This provides a UTOPIA bus with a bandwidth of 200 MB/s, equal to the maximum bandwidth of the LVDS interface.

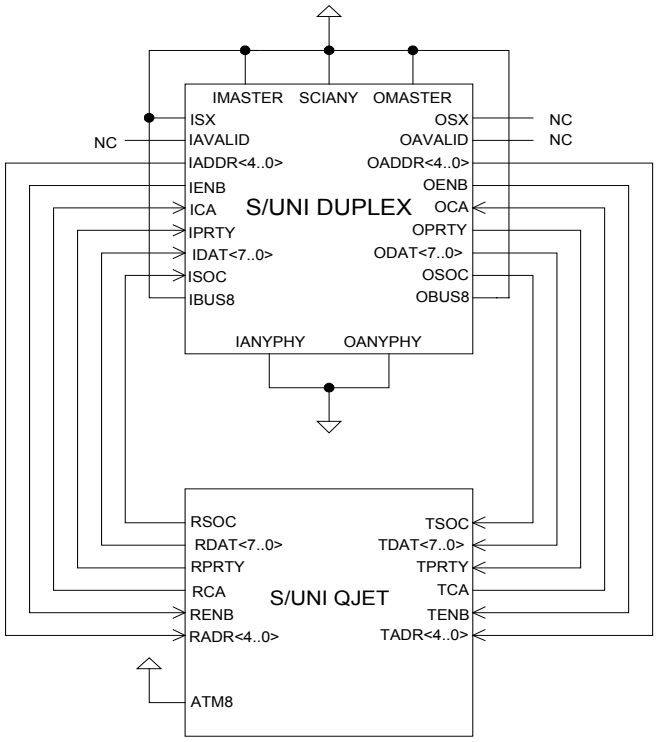


Figure 5. UTOPIA Bus Interface on the WAN Card.

4.8 DS-3 Line Interface

To connect to the WAN via a DS-3 interface, the TDK 78P7200 DS-3/E3/STS-1 Line Interface Unit is required. The connections between the S/UNI-QJET and the LIU are as illustrated in Figure 6.

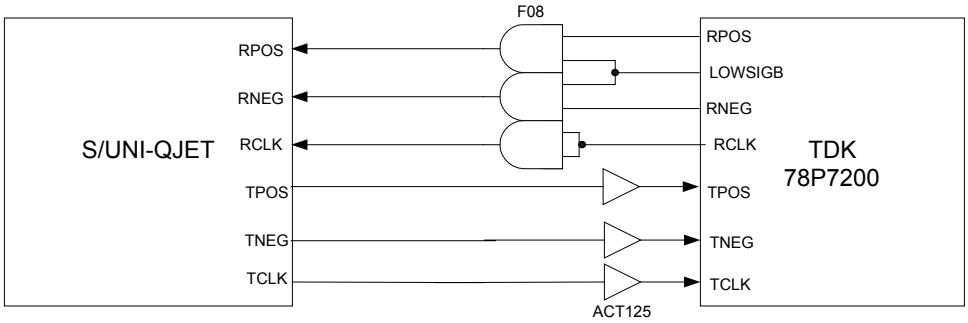


Figure 6. S/UNI-QJET to LIU Interface

The ACT125 buffers are required in order to produce the guaranteed 3.5V V_{IH} required by the DS-3 LIU.

In the receive direction (from the network), 74F08 gates are used to increase the slew rate of signals output from the LIU. For further discussion of this issue, please refer to [8] PMC-1950946, "Interfacing the D3MX to the SSI 78P7200 DS-3 LIU". Figure 6 above also indicates that the output signals from the LIU are ANDed (using the 74F08 gates) with the LIU signal LOWSIGB. LOWSIGB is an active low signal that is low when the input signal to the LIU (from the network) is less than a threshold value. Therefore, when the input signal to the LIU is too low, LOWSIGB is low, resulting in the outputs to the S/UNI-QJET being held low. The RCLK signal is also routed through a 74F08 gate so that it will be delayed by the same amount of time as the RPOS & RNEG signals.

Table 8 indicates how to configure the 78P7200 to operate in its various modes.

Table 8. Configuring the LIU

SPEED	CABLE	OPT1B	LBO
DS-3	< 225'	HIGH	HIGH
DS-3	> 225'	HIGH	LOW
E3	ALL	LOW	LOW

For long lines (cable length longer than 225') LBO should be set low, while for short lines it should be set high. This is accomplished through an on board jumper.

In addition to the above, the signal OPT2B should be set high for normal operation. When OPT2B is low, the LIU is in a low power, standby mode.

The physical interface to the DS-3 line will be via SMB connectors on the front panel.

4.9 Compact PCI Interface

The WAN card will be inserted into a Compact PCI shelf. Connector J1 will plug into P1 of the Compact PCI shelf, while connector J5 will plug into the custom DSLAM backplane that resides in the CompactPCI shelf. Although the DSLAM WAN card interconnects with the standard CompactPCI P1 connector, it does not communicate with the host CPU. The WAN card simply draws power (+5V) from this connector. Control of the S/UNI-DUPLEX and S/UNI-QJET is via an on board microprocessor (see Section 4.3).

As mentioned previously, the WAN card also interfaces with the CompactPCI shelf via the custom DSLAM backplane. It is through this backplane that intra-shelf LVDS signals are transported. Communication among the various DSLAM cards is facilitated through the embedded inter-device communication channel. For further information, please refer to [2], PMC-1981025, “S/UNI-VORTEX and S/UNI-DUPLEX Technical Overview”.

4.10 Front Panel Interface

The front panel interface for the WAN card will have the following components:

1. Eight SMB connectors for the four DS-3 lines, rather than the traditional BNC connectors due to the height restrictions of the CompactPCI card.

2. Two Firewire connectors to allow for connection of external LVDS links. Firewire connectors are chosen due to their ability to handle the expected data rate.

3. LEDs to provide status information.

4. An RJ-45 connector for the RS-232 interface to allow for programming and debugging.

For additional information regarding the front panel interface, please refer to PMC-1990357, “DSLAM Reference Design: System Design”, [5].

5 SOFTWARE CONFIGURATION

5.1 S/UNI-DUPLEX

After a reset has been performed, a software reset is recommended to bring the S/UNI-DUPLEX into its default operating state. As well, the following configuration changes should be made on the S/UNI-DUPLEX.

Table 9. S/UNI-DUPLEX Software Initialization Sequence

REGISTER	ADDRESS	VALUE	FUNCTION
Master Reset	0x00h	0x80h	Set the software reset bit
Master Reset	0x00h	0x00h	Remove the software reset

Table 10. Recommended S/UNI-DUPLEX Configuration

REGISTER	ADDRESS	VALUE	FUNCTION
Master Configuration	01h	0x06	Sets the MINTE bit high, enabling interrupts to appear on the INTB pin.
SCI-PHY/Any-PHY Input Configuration 2	0Dh	0x23	Sets the polling range of the SCI-PHY/Any-PHY input port to be four devices
SCI-PHY/Any-PHY Output Polling Range	15h	0x03	Sets the polling range of the SCI-PHY/Any-PHY output port to be four devices

5.2 S/UNI-QJET

A software reset should also be performed to bring the S/UNI-QJET into its default state. If C bit parity is to be used, the following registers must be set after resetting the device.

Table 11. S/UNI-QJET Software Initialization Sequence

REGISTER	ADDRESS	VALUE	FUNCTION
Master Reset	0x006h	0x80h	Sets the software reset bit
Master Reset	0x006h	0x00h	Removes the software reset

Table 12. C-bit Parity S/UNI-QJET Configuration

REGISTER	ADDRESS	VALUE	FUNCTION
DS3 FRMR Configuration	0xX30	83	Enables C bit parity mode
DS3 TRAN Configuration	0xX34	01	Enables C bit parity

Note: The 'X' in the address field for Table 12 should be replaced by the channel number in question. (0, 1, 2, or 3).

6 DESIGN CONSIDERATIONS

6.1 S/UNI-DUPLEX Power Supply

During power-up, the BIAS pin must be equal to or greater than the voltage on the VDD pins. This is accomplished by the voltage regulator. The voltage on the BIAS pin is also the same one that is regulated to the VDD voltage. Therefore, the worst case is that the regulator malfunctions and shorts which still leaves the BIAS pin equal to VDD. Also, an extra protection diode can be used to limit the VDD to a maximum of 0.5V above the BIAS voltage.

Analog power pins QAVD, CAVD, RAVD and TAVD must be applied after VDD or, must be current limited to the maximum latch-up current of 100mA. A simple solution is to use a small filtering network between the VDD and AVD planes to delay the power to the AVD plane, which will delay power to each AVD pin. Each network is a single R-C network, with the resistor between the AVD plane and the AVD pin, and the capacitor from the AVD pin to the ground plane.

The differential voltage measured between AVD supplies and VDD must be less than 0.5V. A Schottky diode with a 0.5V drop should be placed in parallel with the filter network between VDD and AVD. This is accomplished using a Shottky diode placed between 5V and 3.3V. This same diode also functions as the extra protection diodes for the S/UNI-DUPLEX and S/UNI-QJET.

6.2 S/UNI-QJET Power Supply

The S/UNI-QJET requires that the BIAS pin be equal to or greater than the voltage on the VDD pins. This can be accomplished as above with the voltage regulator, and for additional safety, the protection diode.

Each of the VDD pins must connect to a common 3.3V power plane, while each of the VSS pins must connect to a common ground plane.

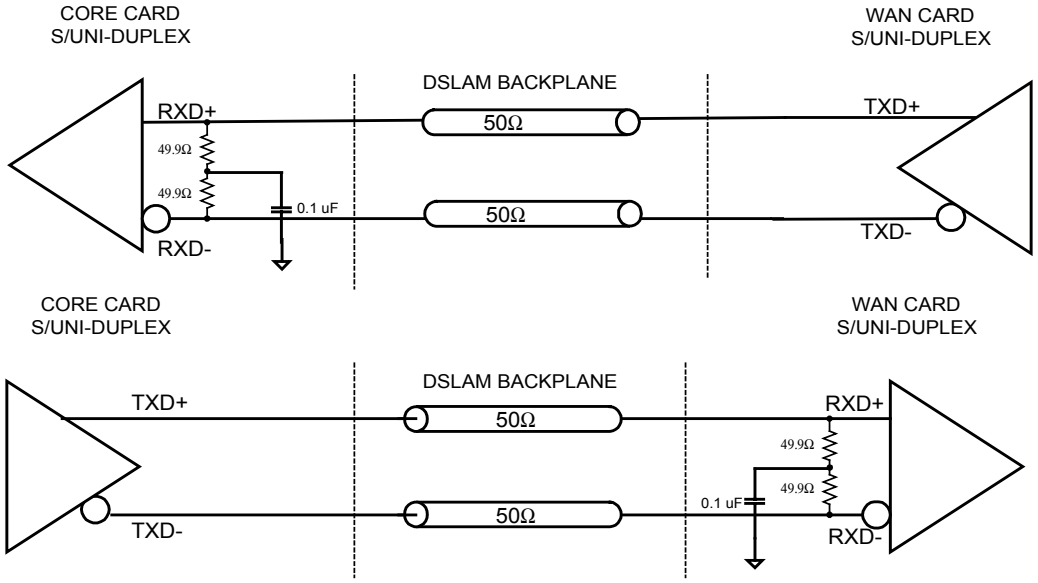
0.1μF bulk capacitors should be placed on alternating power pins along with 0.01μF decoupling capacitors.

6.3 LVDS Design Notes

The low voltage differential signals should be routed together. The two traces that form a differential TX/RX path should have equal trace lengths from the chip to the connector. This is so that any coupling that occurs on the TX/RX path is common-mode and not differential.

Traces for the LVDS signals should have controlled impedances. The two 49.9Ω differential receive termination resistors should be located as physically close to the chip as possible.

There are two methods of termination for the LVDS signals, selectable through onboard jumpers. The first method, depicted in Figure 7, is used for LVDS lines that interface to the DSLAM backplane.



Backplane Termination

Figure 7. LVDS Backplane Termination Scheme

The second method, depicted in Figure 8 on the next page, is used for LVDS lines that interface to the front panel. Two additional termination methods are possible for front panel LVDS signals:

1. Capacitive Coupling
2. Transformer Coupling

Capacitive coupling, as indicated by the dashed lines offers a low cost, low board space alternative for LVDS signals that originate from shelves on the same ground system. To use the capacitive coupling option, do not install the transformers. Install the 0.22μF and 1MΩ resistors instead.

For shelf to shelf termination where the shelves are on different ground systems, we recommend using transformers to provide proper isolation. Common mode chokes are

also used to reduce the amount of radiated and received electromagnetic interference (EMI). Only one end of the connection requires transformers. These transformers are not used on the Core cord due to the large number of transformers that would be required to interface to both the Line and WAN Cards.

To use the transformer coupling option, do not install the 0.22 µF or 1MΩ resistors. Install the transformer instead.

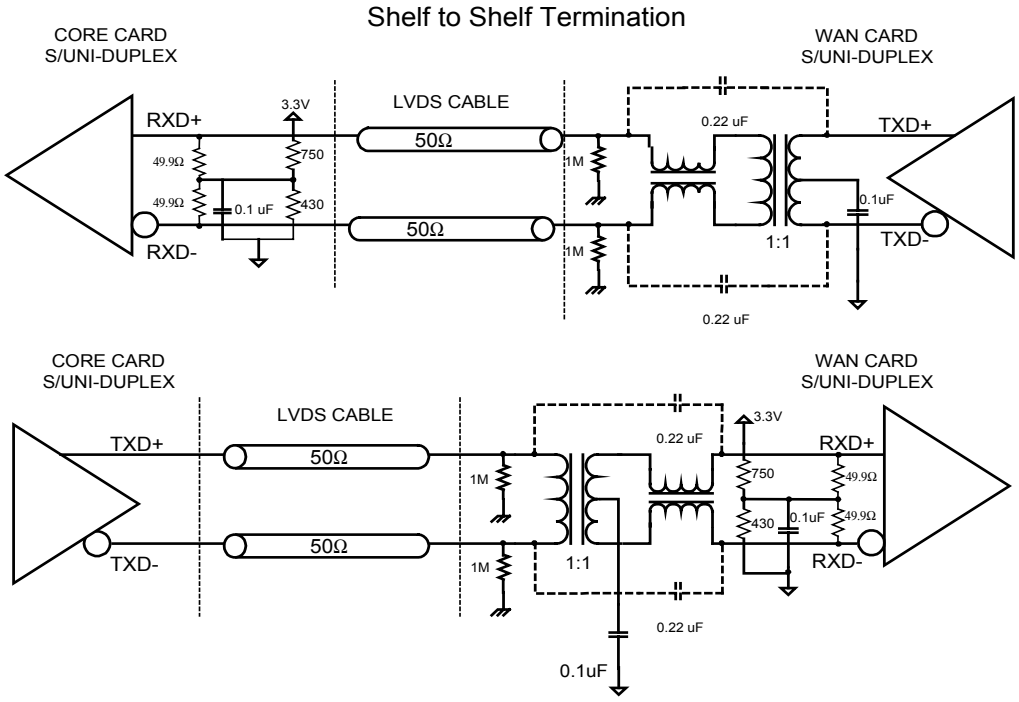


Figure 8. LVDS Front Panel Termination Scheme

In all termination methods, the LVDS receive signals are terminated by two 49.9Ω resistors and a 0.1uF capacitor as shown in Figure 7. This termination network should be placed as physically close to the S/UNI-DUPLEX as possible.

7 IMPLEMENTATION DESCRIPTION

7.1 Root Drawing, Sheet 1

This sheet provides an overview of the major functional blocks of the DSLAM WAN card reference design. This sheet includes how the various blocks connect together.

7.2 S/UNI-DUPLEX Block, Sheets 2 and 3

These sheets show how to connect the S/UNI-DUPLEX into the WAN Card reference design.

- Two 25 MHz oscillators are shown on page 2. Y4 is used to clock the UTOPIA bus, as well as the microprocessor. Y5 is used to drive the REFCLK pin of the S/UNI-DUPLEX. Two oscillators are used so that the bit rate of the LVDS interface may be changed without affecting the clock signal of the microprocessor.

- 8 jumpers are indicated on page 3. These jumpers select either the front panel or backplane LVDS interface. To select the front panel mode, for LVDS port 1, all 4 jumpers for port 1 should be placed in the FP position. If LVDS over the backplane is desired, they should be placed in the BP position.

7.3 S/UNI-QJET Block, Sheet 4

This sheet shows how to connect the S/UNI-QJET into the WAN Card reference design.

7.4 DS3 LIU Block, Sheets 5 and 6

These sheets show how the TDK 78P7200 is connected in the WAN Card reference design. Note that SMB connectors are used rather than BNC connectors. Each SMB connector is connected to chassis ground via a 1M resistor. A jumper is available per LIU, for selection of line length.

7.5 Micro Block, Sheets 7,8, and 9

These three sheets show the integration of the MC68340 microprocessor into the WAN Card reference design.

- Sheet 7 shows the connections to the MC68340, with U1 used to provide the serial interface. In addition, J24 is used to provide access to background debug mode functions.

- Sheet 8 shows the interface between the microprocessor and the system RAM (U11 and U12) and ROM (U13) via 16 bit bus transceivers (U19 and U16). U19 is used in "flow through" mode, allowing address signals to pass straight through the device to the RAM and ROM.

- Sheet 9 shows the connections to the ACTEL 42MX09 FPGA (U21). Jumper J27 selects either ROM (jumper not installed) or BDM (jumper installed) mode of operation.

7.6 Compact PCI Interface Block, Sheets 10 and 11

These sheets show how the board is connected into the CompactPCI shelf.

- Sheet 10 shows the connections of the board to Compact PCI connector J1. Note that only power is derived from J1. Included in the implementation is a hot swap controller (U25) and a 3A linear regulator (U26). U26 provides the necessary 3.3V power, derived from the +5V supply of the CompactPCI shelf. An additional feature is the ESD strip, which is included in the draft proposal for Compact PCI Hot Swap compatibility.

- Sheet 11 shows the connections of the board to the DSLAM system backplane. The DSLAM system backplane is used to transmit LVDS signals between boards in the same CompactPCI shelf.

8 ERRATA

The following section details bugs found in the testing phase of this reference design. In order for this design to behave as specified, the following corrections are necessary.

Problem: The 4 transformers interfacing to the line output pins of the LIUs need to have their center tap pins tied to VCC (+5V).

Solution: Connect pin 2 of T3, T4, T7, T8 to +5V.

Problem: With regards to oscillators Y4 & Y5, the layout has provided for either half-size (8 pin) or full-size (14 pin) oscillators to be used. However a layout error is present on Y5. The pad for the output pins of the 8-pin & 14-pin devices should be tied together. In the case of Y5, the output pad for the 8-pin device is connected to GND.

Solution: Only a full-size (14-pin) oscillator may be used for Y5.

Note: 8-pin & 14-pin are simply designators used to indicate the size of the oscillator. The oscillators themselves have only 4 pins each.

Note: This error is not contained in the schematics. It only occurred during layout of the board.

Problem: The LT1528 Voltage Regulator (U26) has its shutdown pin (pin 4) driven by the reset pin of the LT1422 Hot Swap Regulator (U25). This was added as an extra safety precaution to ensure that the 5V supply is supplied to the board before the 3.3V supply. This precaution has been deemed unnecessary as the design only requires the 5V supply rail to be greater than the 3.3V supply rail at all times. The LT1528 guarantees this regardless of how the shutdown pin is used.

Solution: Leave pin 4 of the LT1528 (U26) unconnected.

9 GLOSSARY

ADSL	Asymmetric Digital Subscriber Line
ANY-PHY	PMC-Sierra extension to the UTOPIA L2 specification allowing any number of PHY devices on the same UTOPIA bus.
ATM	Asynchronous Transfer Mode
CO	Central Office
DS-3	Digital Services 3. A hierarchical structure consisting of 28 DS-1's at an aggregate line rate of 44.736 MB/s.
DSLAM	Digital Subscriber Line Access Multiplexer
LAN	Local Area Network
LVDS	Low Voltage Differential Signal
POTS	Plain Old Telephone Service
PSTN	Public Switched Telephone Network
SCI-PHY	PMC-Sierra extension to the UTOPIA L2 specification allowing 32 rather than 31 PHY devices on the same UTOPIA bus.
S/UNI	SATURN User Network Interface
S/UNI-DUPLEX	PMC-Sierra's mnemonic for the PM7350 Dual Port Serialized UTOPIA Multiplexer (DUPLEX).
S/UNI-QJET	PMC-Sierra's mnemonic for the PM7346 Saturn Quad User Network Interface for J2/E3/T3
UTOPIA	The Universal Test and Operations PHY Interface for ATM (UTOPIA) specification deals with the interface between the PHY and ATM layer in the ATM protocol stack.
WAN	Wide Area Network

10 APPENDIX A: SCHEMATICS

DSLAM REFERENCE DESIGN: WAN CARD

PMC-SIERRA, INC. ISSUE 2

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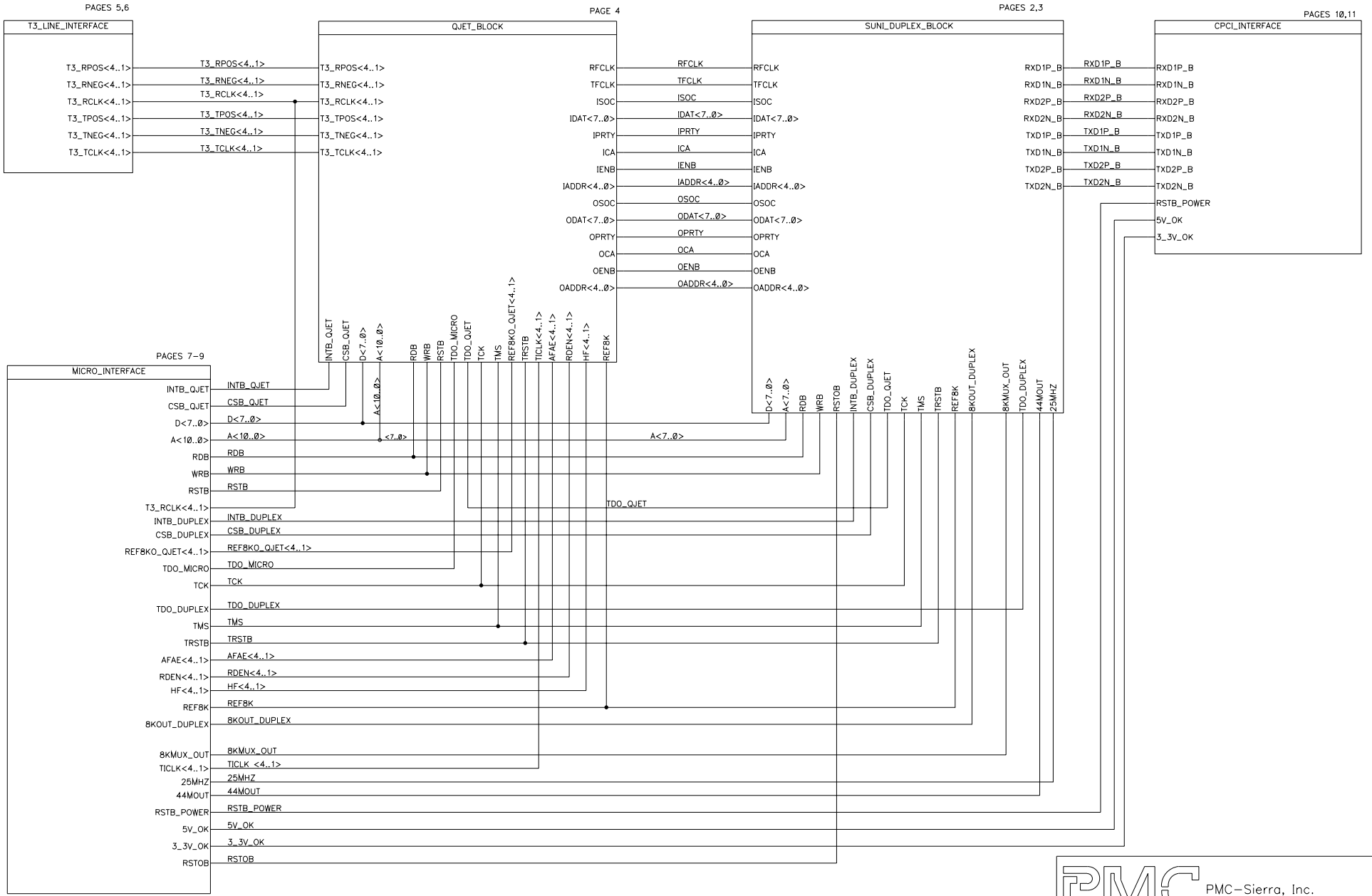

NOTE: ALL TRACES 75 OHM UNLESS OTHERWISE NOTED.

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PMC-Sierra, Inc.

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ENGINEER: PMC-SIERRA (MG)	PAGE: 1 OF 11

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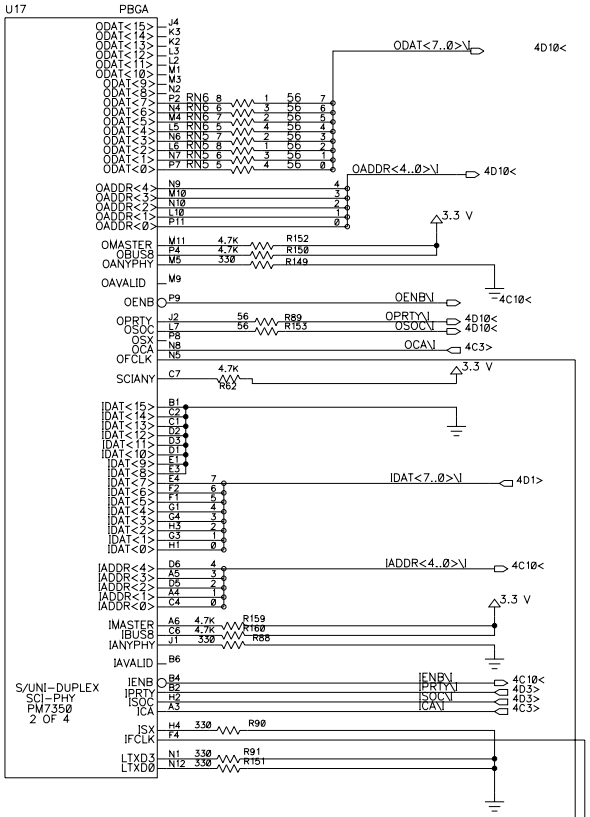
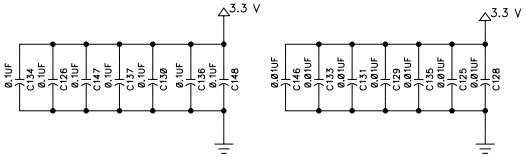
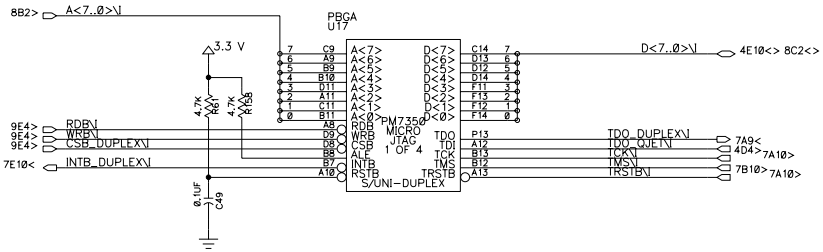
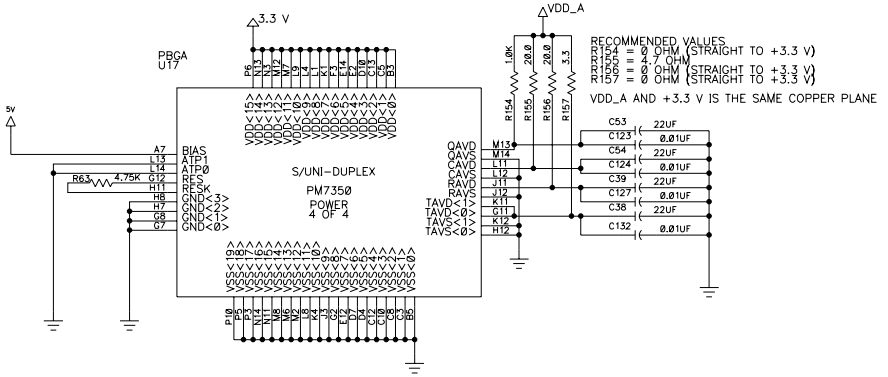
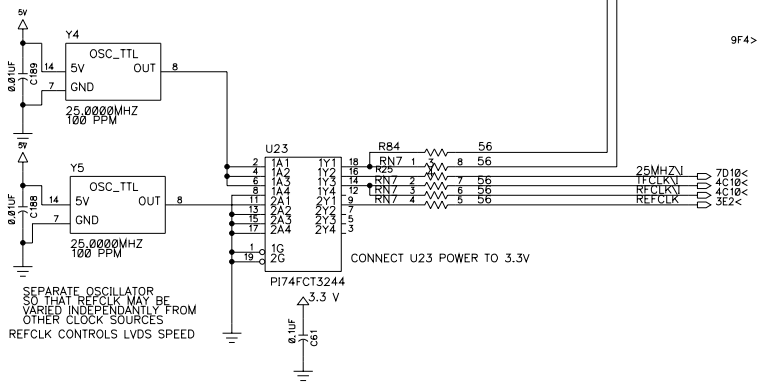


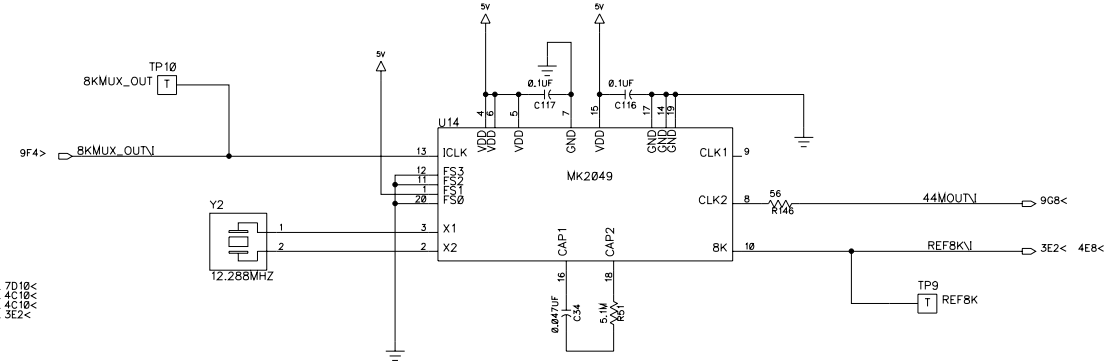




NOTE: PLACE FILTER NETWORKS AS PHYSICALLY CLOSE TO THE DEVICE AS POSSIBLE.







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ENGINEER: PMC-SIERRA, INC. (MG)	PAGE: 2 OF 11

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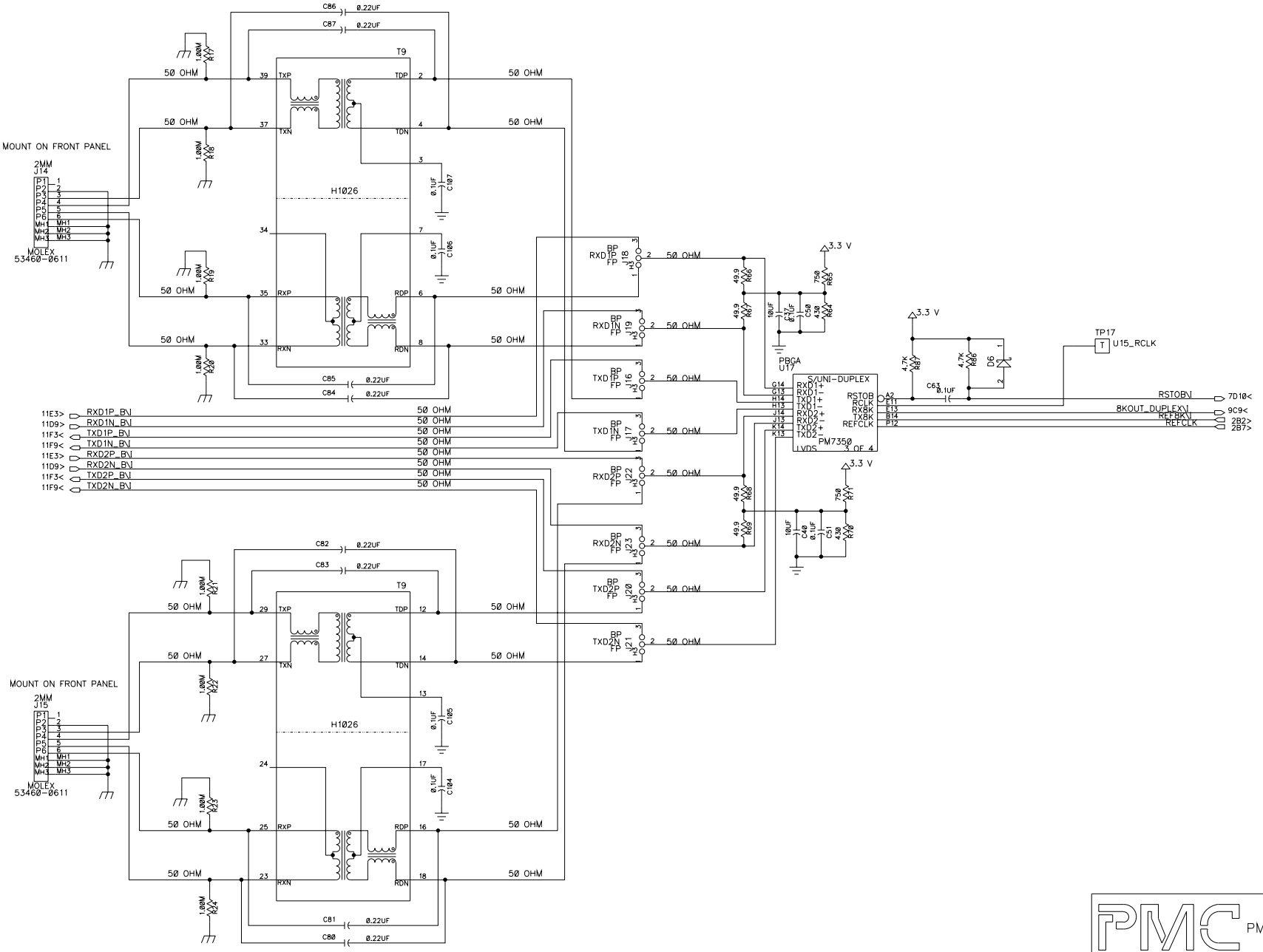
NOTE: IF NOT USING TRANSFORMER COUPLING, DO NOT INSTALL T9.



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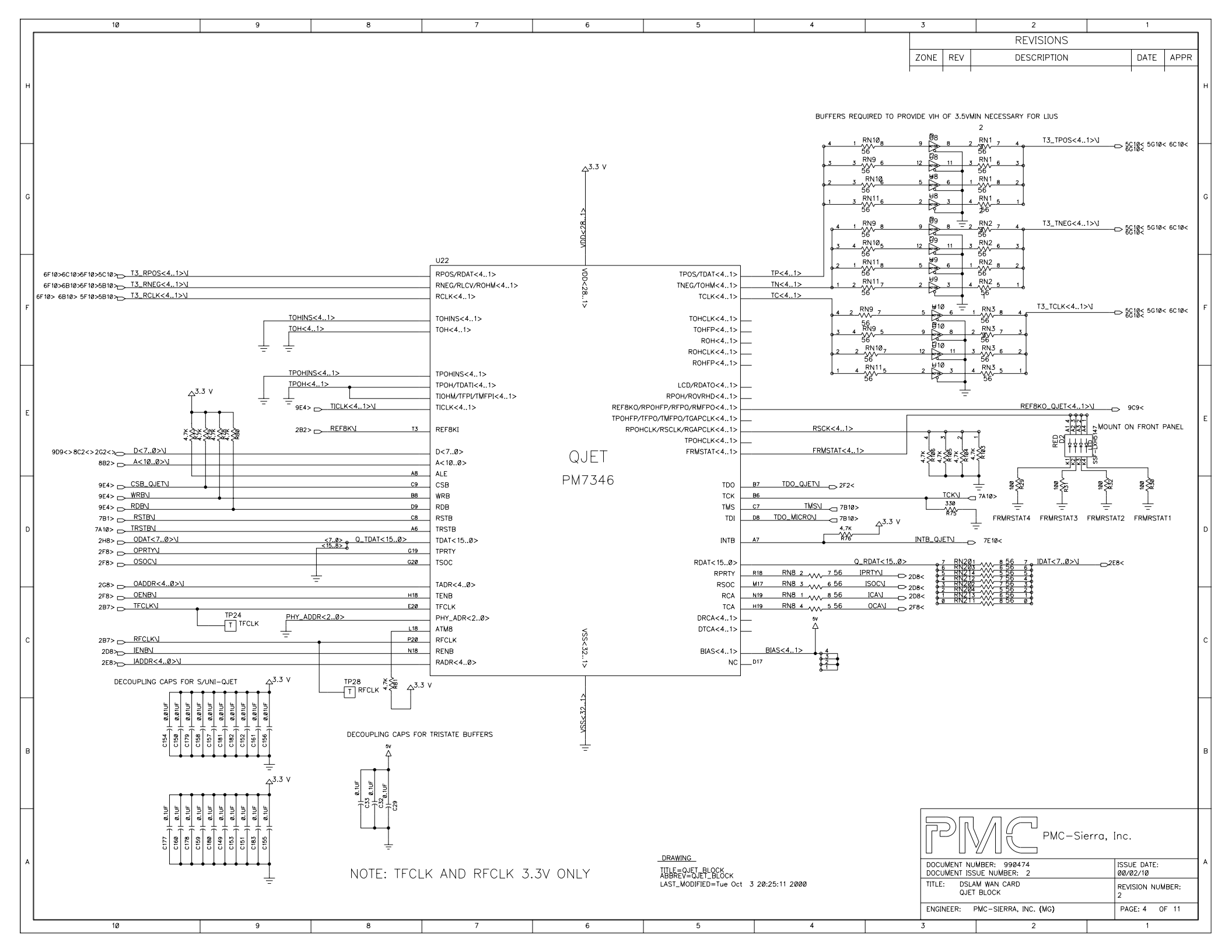
BUFFERS REQUIRED TO PROVIDE VIH OF 3.5VMIN NECESSARY FOR LIUS



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DS-3 LINE INTERFACE

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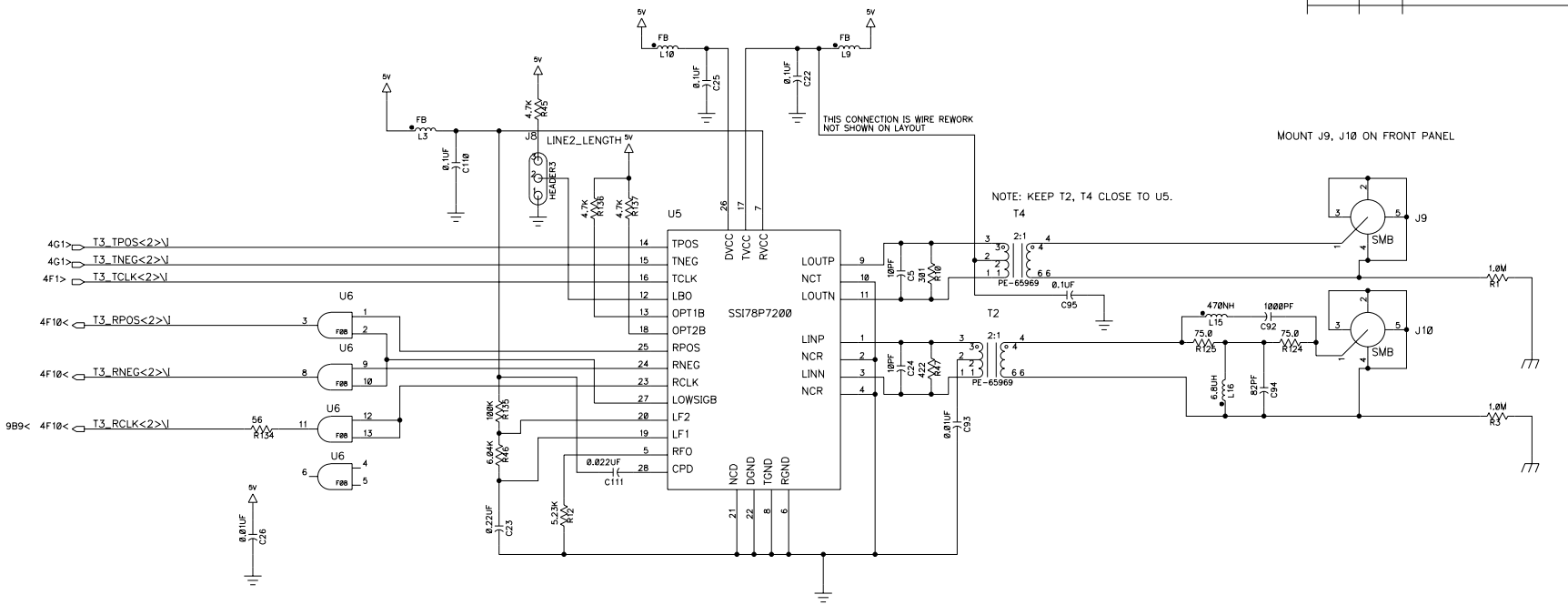

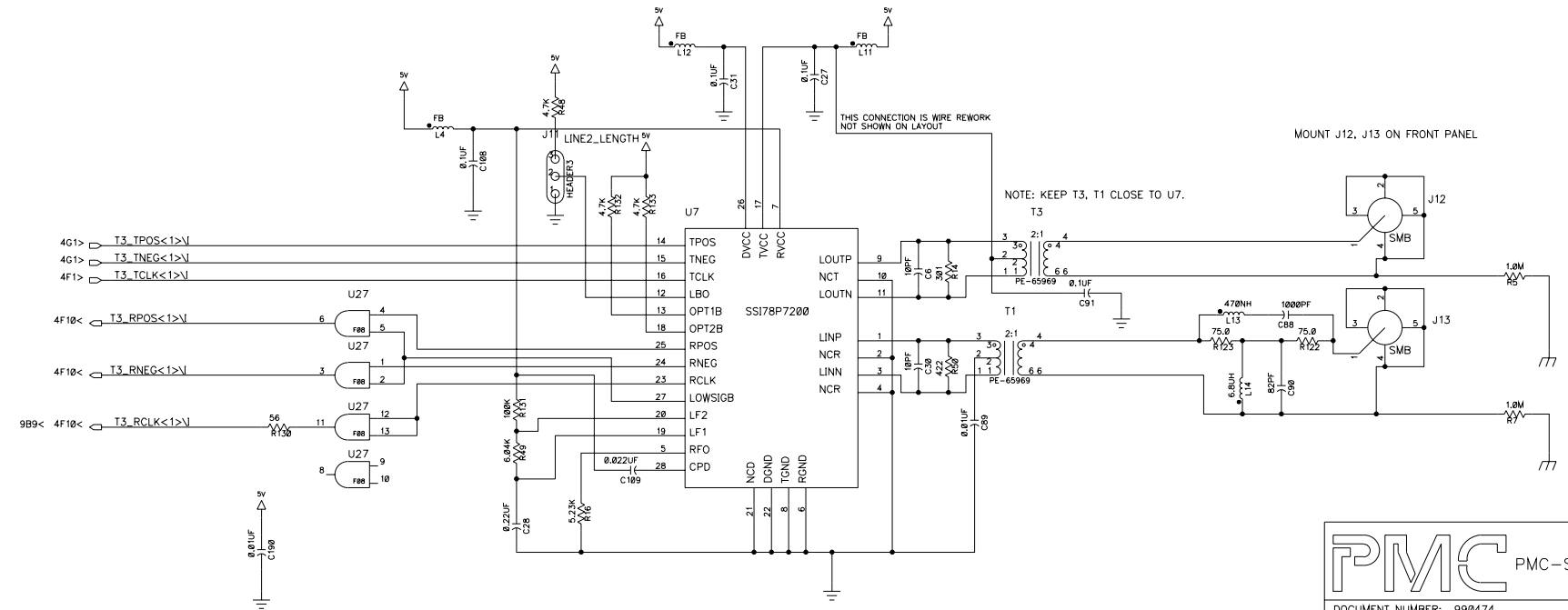

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DS-3 LINE INTERFACE

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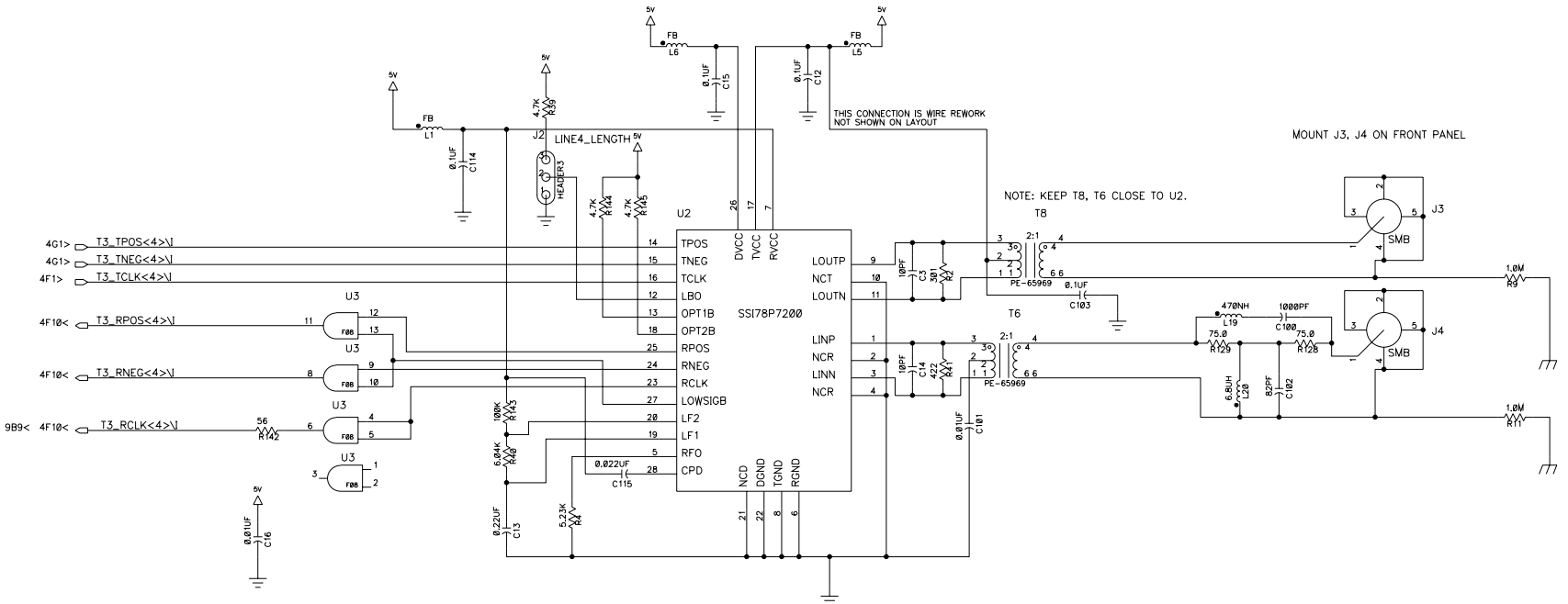

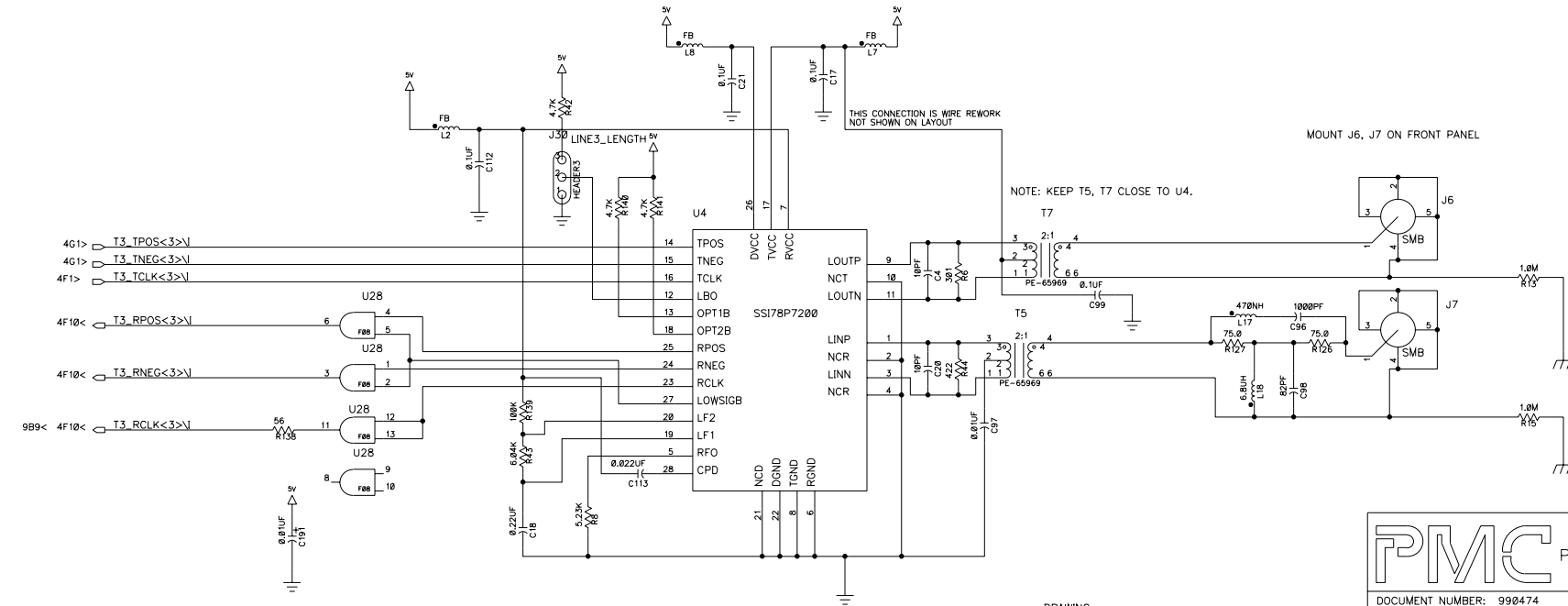

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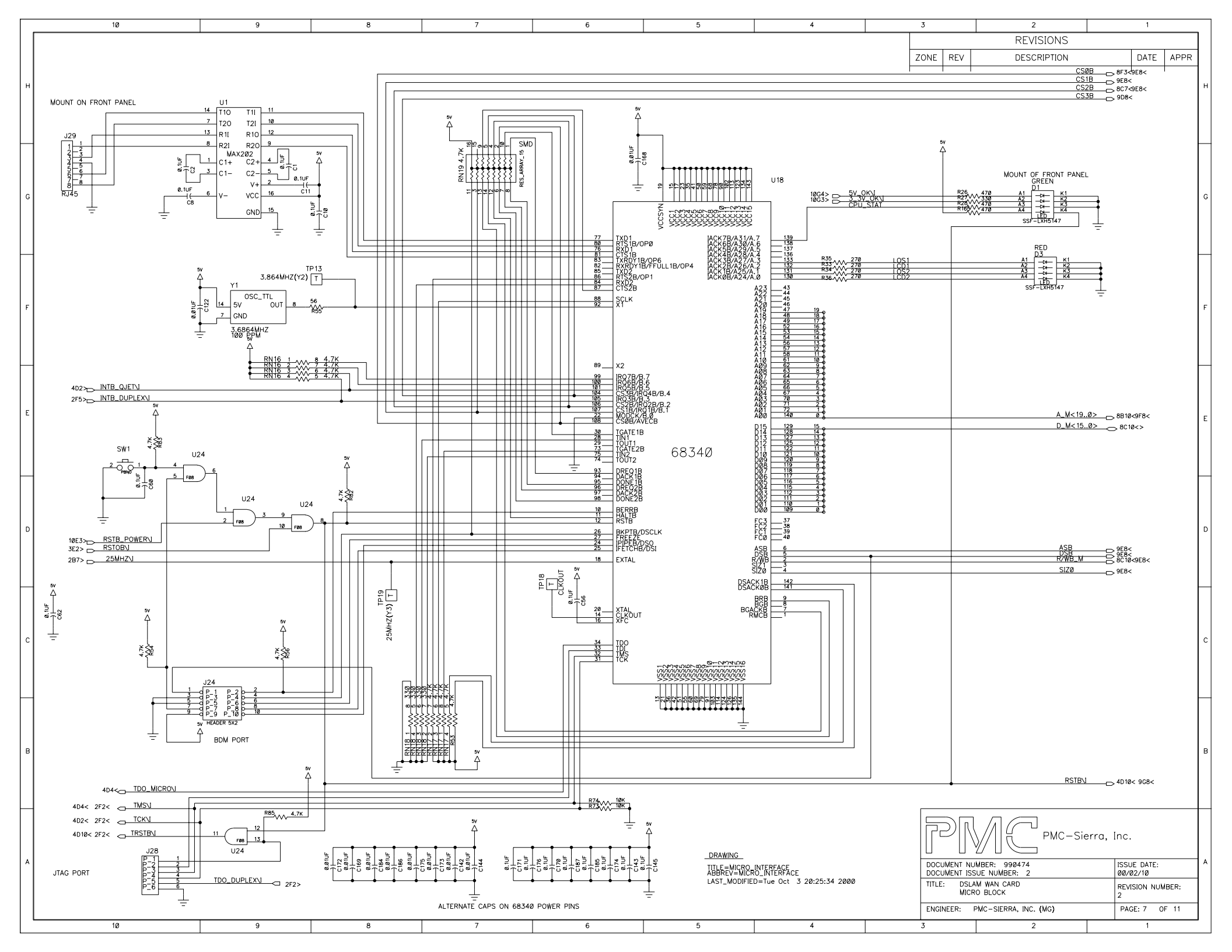
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J29
RJ45
U18
68340
MOUNT OF FRONT PANEL
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SSF-LXH5147
RED
D3
SSF-LXH5147
SW1
U24
J24
HEADER 5X2
BDM PORT
JTAG PORT
J28
TP13
3.864MHZ(Y2)
TP19
25MHZ(Y3)
TP18
CLKOUT
Y1
OSC_TTL
3.6864MHZ
100 PPM
5V
RN19 4.7K
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DSB
R/WB_M
SIZ0
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INTB_DUPLEXV
RSTB_POWERV
RSTOBV
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TDO_MICROV
TMSV
TCKV
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5V_OKV
3_3V_OKV
CPU_STAT
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LOS2
LCD1
LCD2
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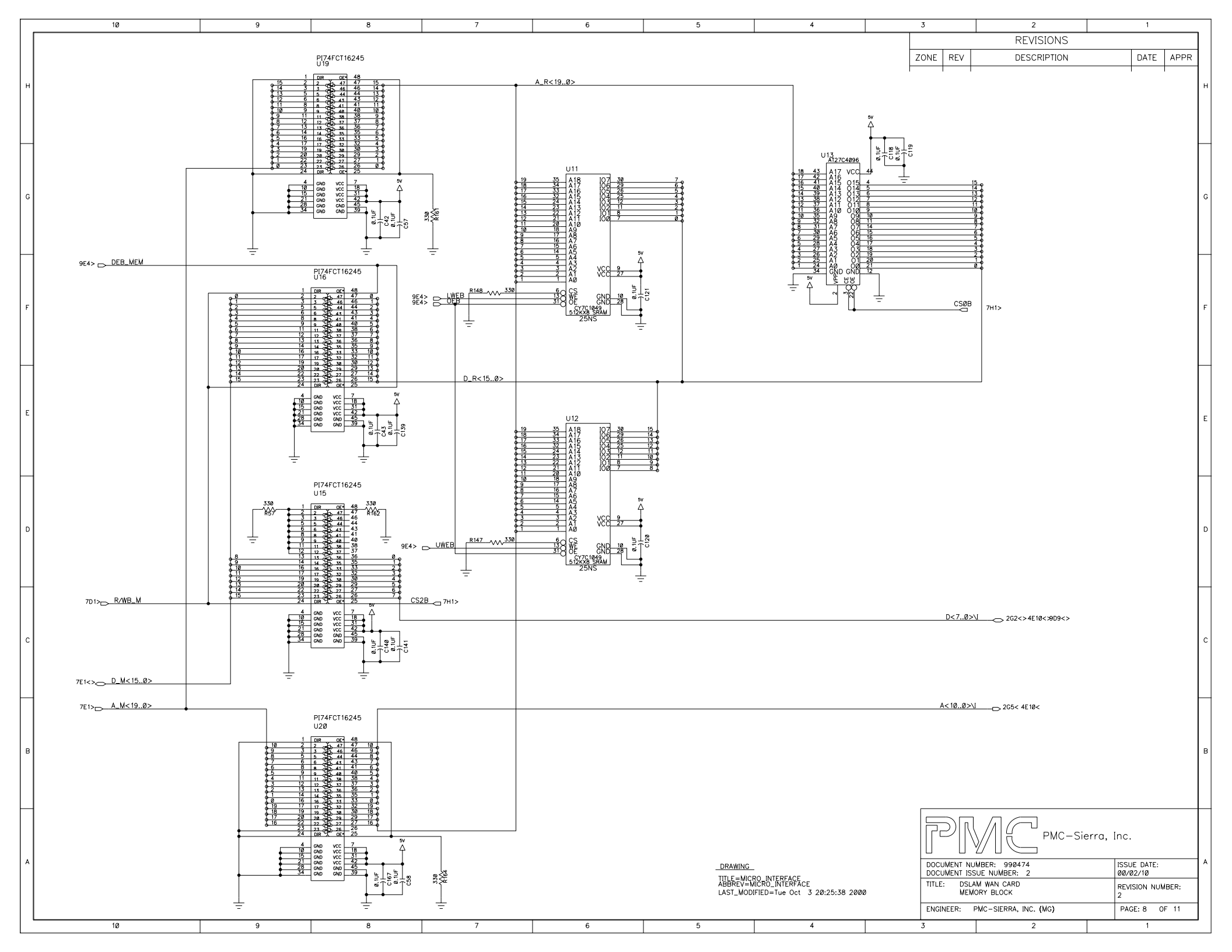
DOCUMENT ISSUE NUMBER: 2
ISSUE DATE: 00/02/10
TITLE: DSLAM WAN CARD MICRO BLOCK
REVISION NUMBER: 2
ENGINEER: PMC-SIERRA, INC. (MG)
PAGE: 7 OF 11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TITLE: DSLAM WAN CARD MEMORY BLOCK
REVISION NUMBER: 2
ENGINEER: PMC-SIERRA, INC. (MG)
PAGE: 8 OF 11

REVISIONS				
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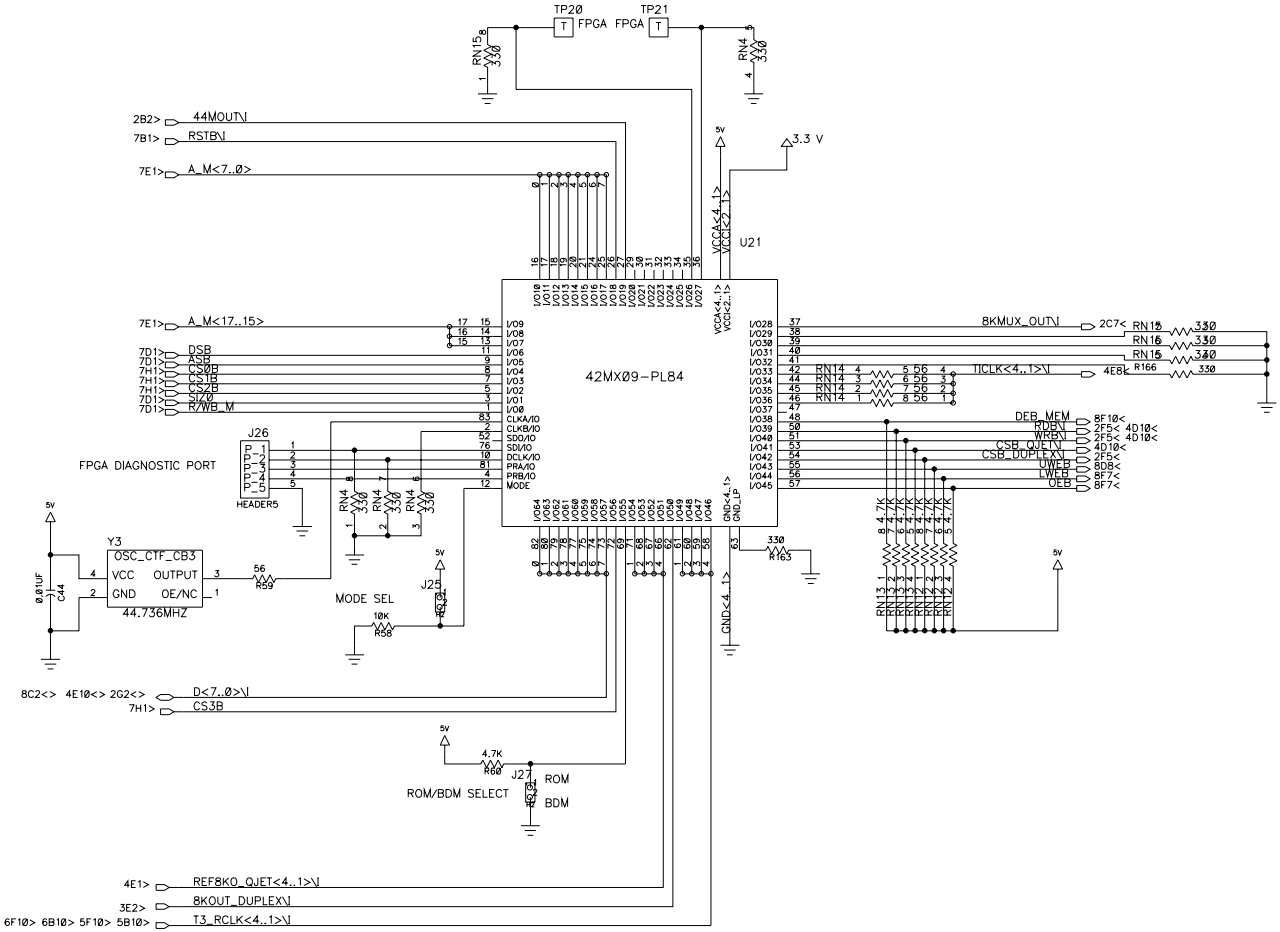
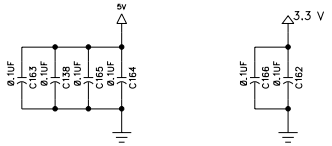


PLACE ONE CAP ON EACH POWER PIN



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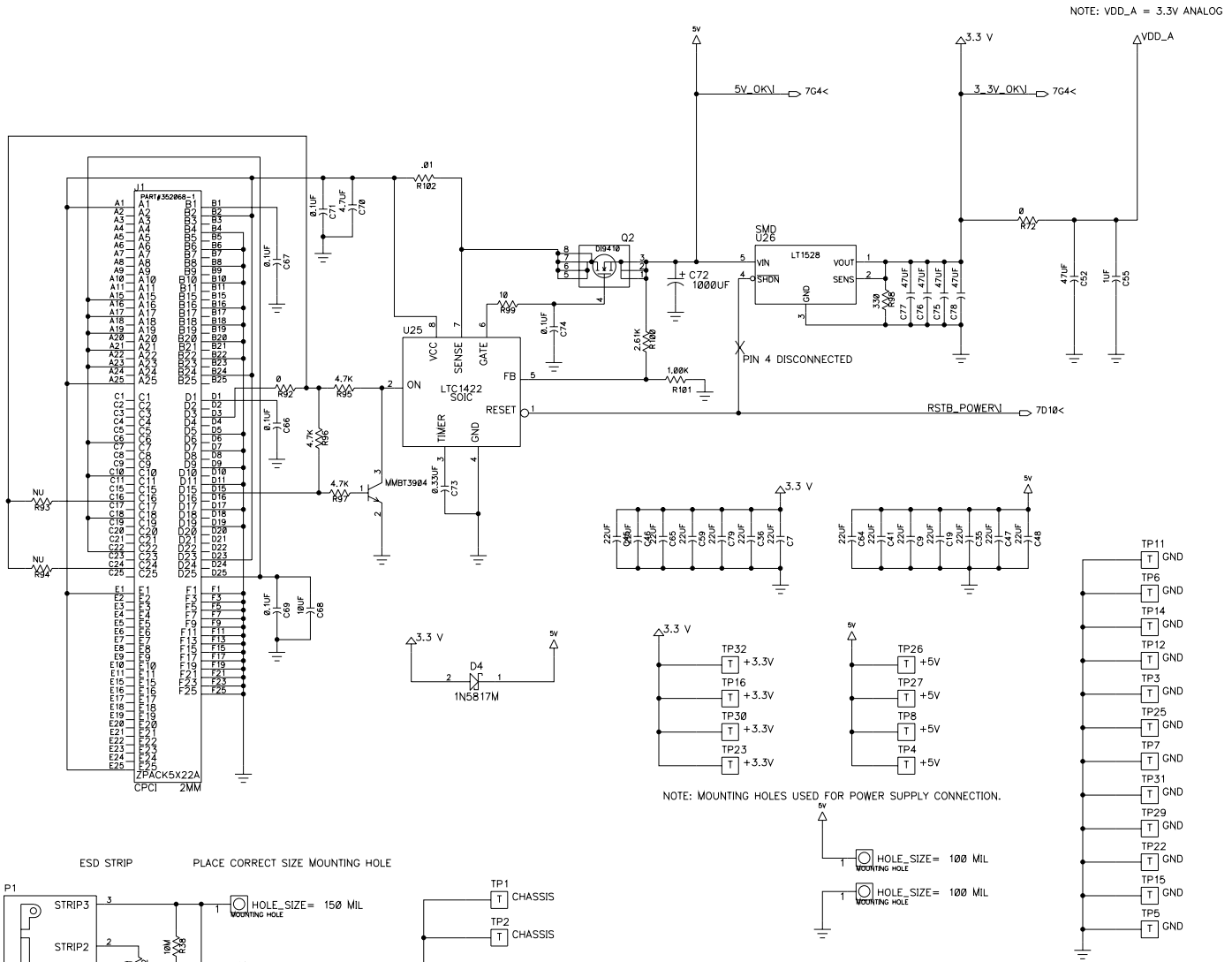
TITLE: DSLAM WAN CARD FPGA BLOCK	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA, INC. (MG)	PAGE: 9 OF 11

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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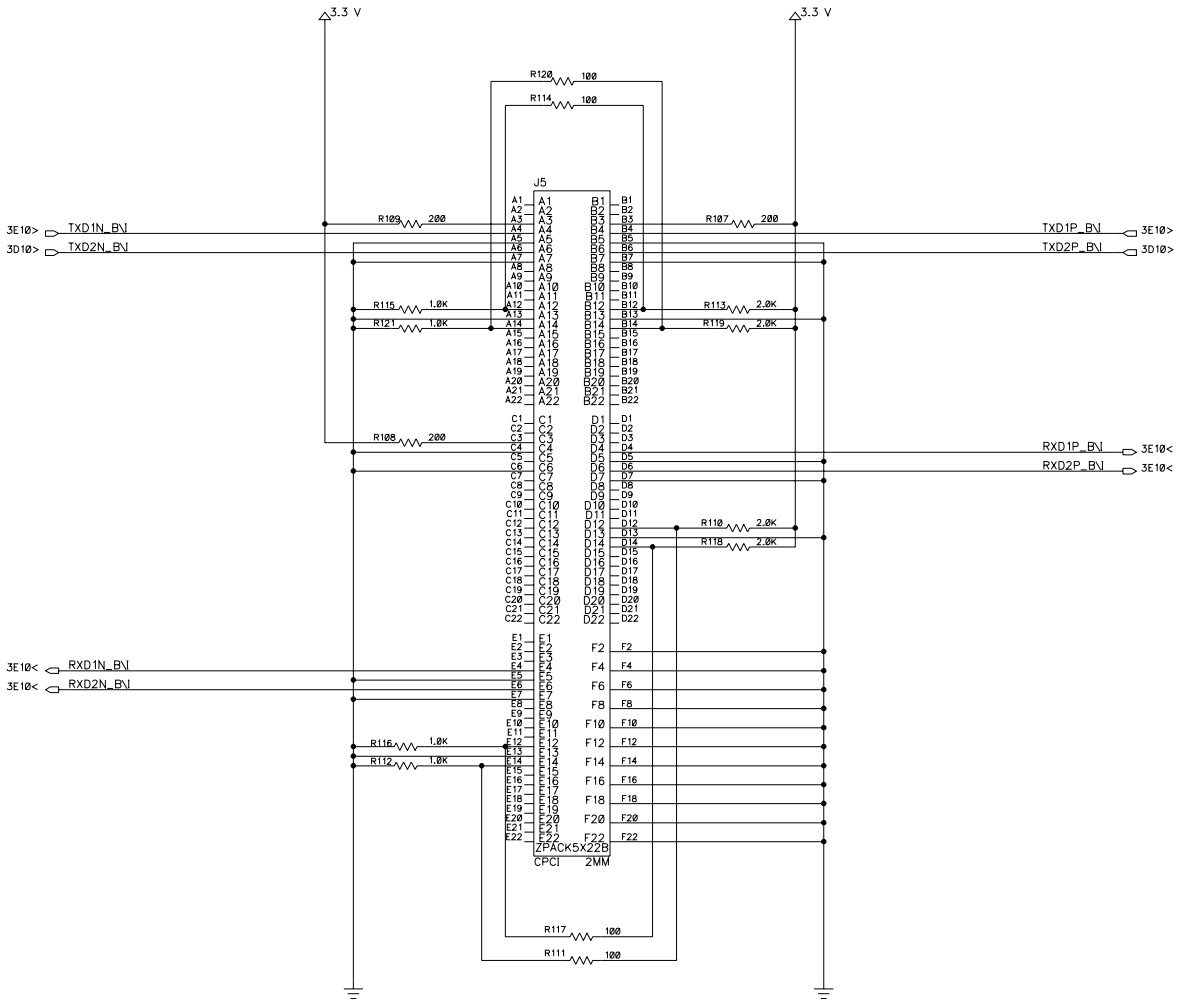
TITLE: DSLAM WAN CARD CPCI INTERFACE	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA, INC. (MG)	PAGE: 10 OF 11

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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TITLE: DSLAM WAN CARD LVDS INTERFACE	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA, INC. (MG)	PAGE: 11 OF 11

11 APPENDIX B: BILL OF MATERIALS

Table 13. Bill of Materials

NO.	Part Name - Value	Part Number	Ref Des	Qty
1	1N5817_-1N5817M	1N5817M	D4	1
2	42MX09_PL84_PLCC_SOCKET-BASE	42MX09_PL84	U21	1
3	74ACT125_SOIC-BASE-VCC=5V	74ACT125SC	U8-U10	3
4	74F08_SOIC-VCC=5V	74F08SC	U27	1
5	74F08_SOIC-VCC=5V	74F08SC	U28 U3,U6,U24,	4
6	74FCT16245_1_SSOP48-BASE	PI74FCT16245ATV	U15,U16, U19,U20	4
7	74FCT3244_SOIC-BASE-VCC=3_3V	PI74FCT3244S	U23	1
8	78P7200_PLCC-BASE	TSC78P7200	U2,U4,U5, U7	4
9	AT27C4096_PLCC-90NS	AT27C4096-90JI	U13	1
10	CAPACITOR-0.01UF, 50V,X7R_603	DIGIKEY PCC103BVCT-ND	C16,C26, C44,C89, C93,C97, C101, C122-C125, C127-C129, C131-C133, C135,C142, C144,C146, C150,C152, C154, C156-C158, C161,C168, C169,C172, C173,C175, C179,C181, C182,C184, C186, C188-C191	42
11	CAPACITOR-0.022UF, 25V,X7R_603	DIGI-KEY -- PCC1767CT-ND	C109,C111, C113,C115	4
12	CAPACITOR-0.047UF, 25V,X7R_0603	NEWARK -- 85F219	C34	1

NO.	Part Name - Value	Part Number	Ref Des	Qty
13	CAPACITOR-0.1UF,16V, X7R_603	PANASONIC -- ECJ-1VB1C104K	C1,C2,C8, C10-C12, C15,C17, C21,C22, C25,C27, C29, C31-C33, C42,C43, C49-C51, C56-C58, C60-C63, C66,C67, C69,C71, C74,C91, C95,C99, C103-C108, C110,C112, C114, C116-C121, C126,C130, C134, C136-C141, C143,C145, C147-C149, C151,C153, C155,C159, C160, C162-C167, C170,C171, C174, C176-C178, C180,C183, C185,C187	86
14	CAPACITOR-0.22UF, 10V,X7R_603	DIGI-KEY -- PCC1749CT-ND	C80-C87	8
15	CAPACITOR-0.22UF, 35V,TANT TEH	DIGI-KEY -- PCT6224CT-ND	C13,C18, C23,C28	4
16	CAPACITOR-0.33UF, 35V,TANT TEH	DIGI-KEY -- PCT6334CT-ND	C73	1
17	CAPACITOR-1000PF, 50V,X7R_0603	DIGI-KEY -- PCC102BNCT-NE	C88,C92, C96,C100	4
18	CAPACITOR-1000UF, 10V,ELECTRO_SA	DIGI-KEY -- PCE3178CT-ND	C72	1
19	CAPACITOR-10PF,50V, NPO_603	DIGI-KEY -- PCC100CVCT-ND	C3-C6,C14, C20,C24, C30	8
20	CAPACITOR-10UF,16V, TANT TEH	DIGI-KEY -- PCT3106CT-ND	C37,C40, C68	3
21	CAPACITOR-1UF,16V, TANT TEH	DIGI-KEY -- PCT3105CT-ND	C55	1
22	CAPACITOR-22UF,16V, TANT TEH	DIGI-KEY -- PCT3226CT-ND	C7,C9,C19, C35,C36, C41, C45-C48, C59,C64,C65, C79	14

NO.	Part Name - Value	Part Number	Ref Des	Qty
23	CAPACITOR-22UF,6.3V, TANT TEH	DIGI-KEY -- PCT1226CT-ND	C38,C39, C53,C54	4
24	CAPACITOR-4.7UF,16V, TANT TEH	DIGI-KEY -- PCT3475CT-ND	C70	1
25	CAPACITOR-47UF,10V, TANT TEH	DIGI-KEY -- PCT2476CT-ND	C52, C75-C78	5
26	CAPACITOR-82PF,50V, NPO_603	DIGI-KEY -- PCC820ACVCT-ND	C90,C94, C98,C102	4
27	CPCI_ESD_STRIP_BOTTOM_EDGE-BASE	PART OF PCB	P1	1
28	CRYSTAL_HC49-12.288MHZ,30PPM	ECX-4735-12.288M	Y2	1
29	CY7C1049-25NS	CY7C1049L-25VC	U11,U12	2
30	DI9410_SOIC-BASE	DI9410	Q2	1
31	DIODE_SCHOTTKY_SMB_2-2A,20V	DIGI-KEY -- B220DICT-ND	D6	1
32	H1026_SMD-BASE	H1026	T9	1
33	HEADER2_100MIL-BASE	PZC36SAAN	J25,J27	2
34	HEADER3S_100MIL-BASE	PZC36SAAN	J16-J23	8
35	HEADER3_100MIL-BASE	PZC36SAAN	J2,J8,J11, J30	4
36	HEADER5X2_100MIL-BASE	PTC36DAAN	J24	1
37	HEADER5_100MIL-BASE	PZC36SAAN	J26	1
38	HEADER6_100MIL-BASE	PZC36SAAN	J28	1
39	INDUCTOR-470NH,, PANASONIC	ELJ-NCR47JF	L13,L15, L17,L19	4
40	INDUCTOR-6.8UH,, PANASONIC	ELJ-FC6R8JF	L14,L16, L18,L20	4
41	INDUCTOR-FB,50, FAIR RITE	FAIR RITE -- 2743019447	L1-L12	12
42	LT1528_SMD-BASE	LINEAR TECHNOLOGY -- LT1528CQ	U26	1
43	LTC1422_SOIC-BASE	LTC1422CS8	U25	1
44	MAX202_1_SOIC16-BASE	MAX202CSA	U1	1
45	MC68340-BASE	MC68340	U18	1
46	MK2049_SOIC-BASE	MK2049-01S	U14	1
47	MMBT3904_SOT23-BASE	MMBT3904LT1	Q1	1
48	MOLEX53460_0611_2MM-BASE	53460-0611	J14,J15	2
49	MOUNTING_HOLE_100MIL-BASE	MOUNTING HOLE	M2,M3	2
50	MOUNTING_HOLE_150MIL-BASE	MOUNTING HOLE	M1	1
51	OSC_CTS_CB3-44.736MHZ,5V,50PPM	CB3-3C-44.7360-T	Y3	1
52	OSC_TTL_DIP-25.0000MHZ,100 PPMA	DIGI-KEY -- CTX171-ND	Y4,Y5	2
53	OSC_TTL_DIP-3.6864MHZ,100 PPM,A	DIGI-KEY -- CTX154-ND	Y1	1
54	PBNO_VERT_6MM-BASE	DIGIKEY -- P8009S-ND	SW1	1
55	PE65969-BASE	PE65969	T1-T8	8

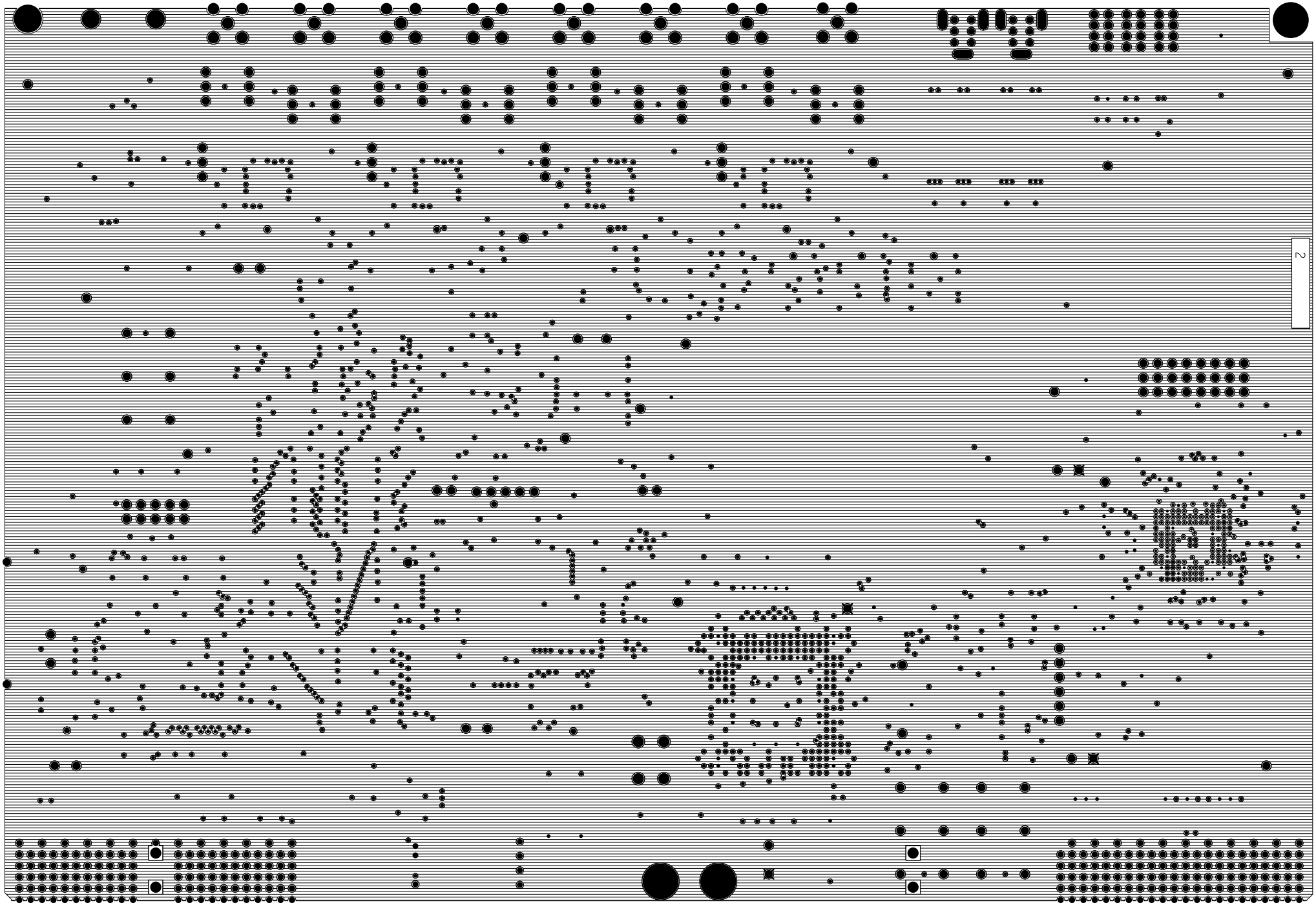
NO.	Part Name - Value	Part Number	Ref Des	Qty
56	RESISTOR-.01,1%,1206	IRC-TT LRC-LR1206-01-R010-F	R102	1
57	RESISTOR-0,5%,603	ERJ-3GSY0R00V	R92-R94	3
58	RESISTOR-0,5%,805	DIGI-KEY -- P<VALUE>ACT-ND	R72	1
59	RESISTOR-1.00K,1%, 805	DIGI-KEY -- P<VALUE>CCT-ND	R101	1
60	RESISTOR-1.00M,1%, 603	DIGI-KEY -- P<VALUE>MHCT-ND	R17-R24	8
61	RESISTOR-1.0K,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R112,R115, R116,R121, R154	5
62	RESISTOR-1.0M,5%,805	DIGI-KEY -- P<VALUE>ACT-ND	R1,R3,R5, R7,R9,R11, R13,R15	8
63	RESISTOR-10,5%,603	DIGI-KEY -- P10GCT-ND	R99	1
64	RESISTOR-100,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R29-R32, R111,R114, R117,R120	8
65	RESISTOR-100K,5%,603	DIGI-KEY -- P100KGCT-ND	R131,R135, R139,R143	4
66	RESISTOR-10K,1%,603	DIGI-KEY -- P<VALUE>GCT-ND	R58,R73, R74	3
67	RESISTOR-10M,5%,1206	DIGI-KEY -- P<VALUE>ECT-ND	R37,R38, R52	3
68	RESISTOR-2.0K,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R110,R113, R118,R119	4
69	RESISTOR-2.61K,1%, 805	DIGI-KEY -- P<VALUE>CCT-ND	R100	1
70	RESISTOR-20.0,1%,603	DIGI-KEY -- P20.0HCT-ND	R155,R156	2
71	RESISTOR-200,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R107-R109	3
72	RESISTOR-270,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R33-R36	4
73	RESISTOR-3.3,1%,805	DIGI-KEY -- P<VALUE>DCT-ND	R157	1
74	RESISTOR-301,1%,603	DIGI-KEY -- P301HCT-ND	R2,R6,R10, R14	4
75	RESISTOR-330,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R27,R57, R75,R88, R90,R91, R98, R147-R149, R151, R161-R164, R166-R169	19
76	RESISTOR-4.75K,1%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R63	1

NO.	Part Name - Value	Part Number	Ref Des	Qty
77	RESISTOR-4.7K,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R39,R42, R45,R48, R53,R54, R56, R60-R62, R76-R83, R85-R87, R95-R97, R103-R106, R132,R133, R136,R137, R140,R141, R144,R145, R150,R152, R158-R160	41
78	RESISTOR-422,1%,603	DIGI-KEY -- P<VALUE>HCT-ND	R41,R44, R47,R50	4
79	RESISTOR-430,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R64,R70	2
80	RESISTOR-470,5%,603	ERJ-3GSYJ471V	R26,R28, R165	3
81	RESISTOR-49.9,1%,603	ERJ-3EKF49R9V	R66-R69	4
82	RESISTOR-5.1M,5%, 1206	DIGI-KEY -- P<VALUE>ECT-ND	R51	1
83	RESISTOR-5.23K,1%, 603	DIGI-KEY -- P<VALUE>HCT-ND	R4,R8,R12, R16	4
84	RESISTOR-56,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R25,R55, R59,R84, R89,R130, R134,R138, R142,R146, R153	11
85	RESISTOR-6.04K,1%, 603	DIGI-KEY -- P6.04KHCT-ND	R40,R43, R46,R49	4
87	RESISTOR-750,5%,603	DIGI-KEY -- P<VALUE>GCT-ND	R65,R71	2
88	RES_ARRAY_15_SMD-4.7K	DIGI-KEY -- 766-161-R<VALUE>-ND	RN19	1
89	RES_ARRAY_4_SMD-330	DIGI-KEY -- Y4<VALUE CODE>-ND	RN4,RN15, RN18	3
90	RES_ARRAY_4_SMD-4.7K	DIGI-KEY -- Y4<VALUE CODE>-ND	RN12,RN13, RN16,RN17	4
91	RES_ARRAY_4_SMD-56	DIGI-KEY -- Y4<VALUE CODE>-ND	RN1-RN3, RN5-RN11, RN14,RN20, RN21	13
92	RJ45-BASE	555078-1	J29	1
93	SMB_RIGHT_ANGLE-BASE	131-3701-341	J3,J4,J6, J7,J9,J10, J12,J13	8
94	SSF_LXH5147-LGD	SSF-LXH5147LGD	D1	1
95	SSF_LXH5147-LID	SSF-LXH5147LID	D2,D3	2
96	SUNIDUPLEX_SCIPHY_2_ PBGA-BASE	PM7350-BI	U17	1

NO.	Part Name - Value	Part Number	Ref Des	Qty
97	SUNI_QJET_SBGA-BASE	PM7346	U22	1
98	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP16,TP23, TP30,TP32	4
99	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP4,TP8, TP26,TP27	4
100	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP19	1
101	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP13	1
102	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP10	1
103	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP1,TP2	2
104	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP18	1
105	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP20,TP21	2
106	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP3, TP5-TP7, TP11,TP12, TP14,TP15, TP22,TP25, TP29,TP31	12
107	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP9	1
108	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP28	1
109	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP24	1
110	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP17	1
111	ZPACK5X22FH_ASCPCI_2MM	352068-1	J1	1
112	ZPACK5X22FH_BSCPI_2MM	352152-1	J5	1

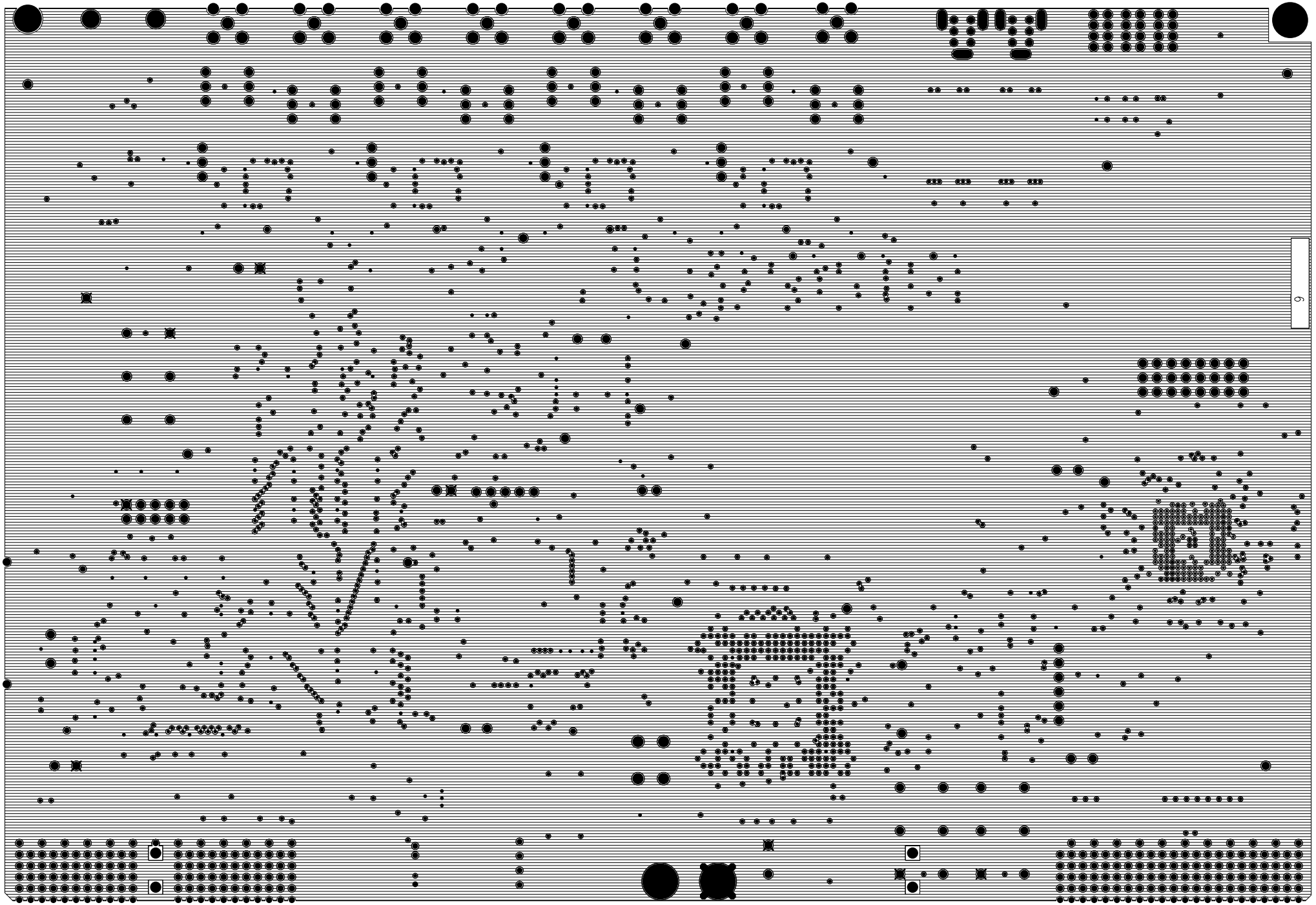
12 APPENDIX C: LAYOUT

3V3 PLANE



PMC-SIERRA DSLAM_WAN REV 2.0 2000

5V PLANE



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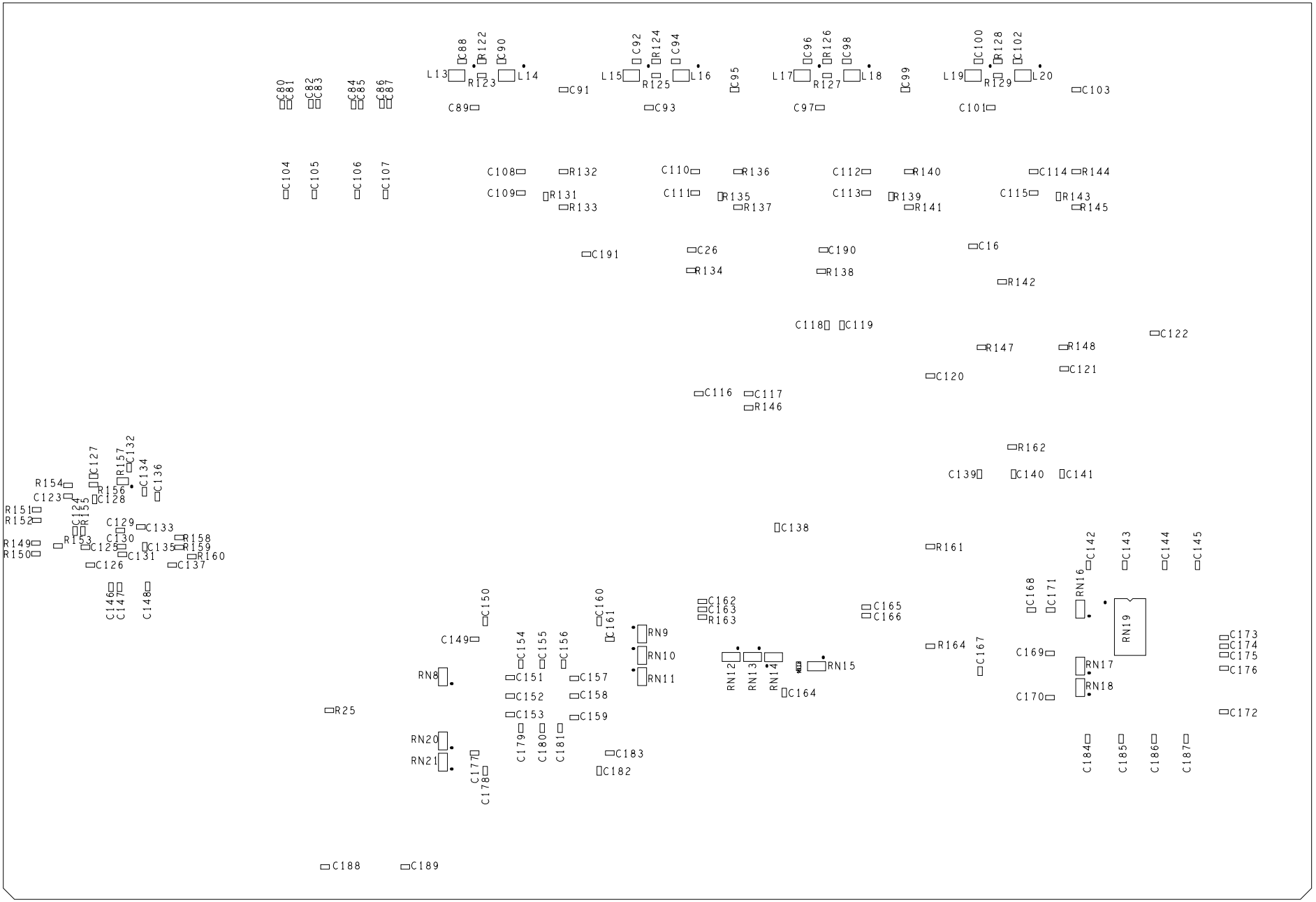
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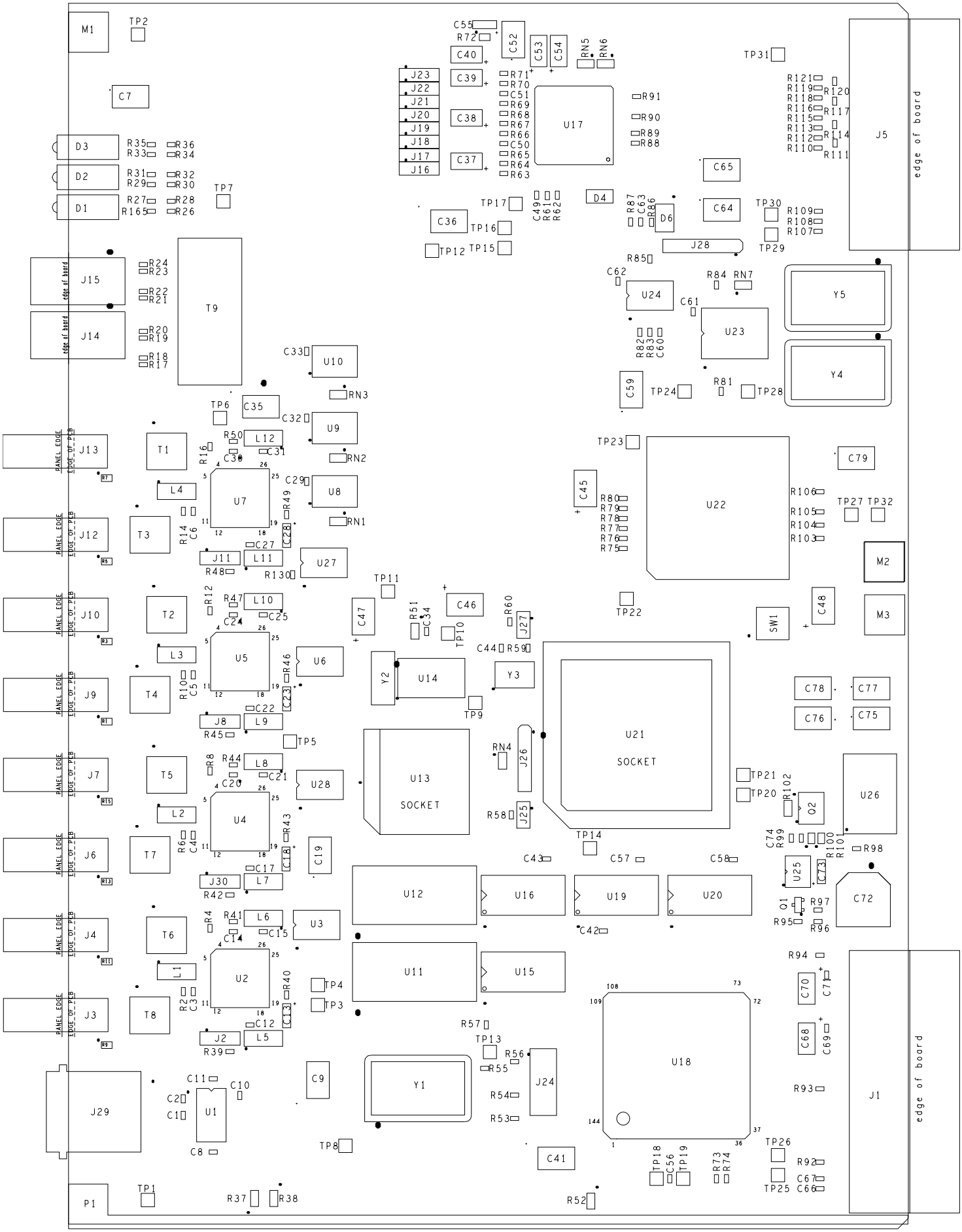
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D3
D2
D1
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R33
R36
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R31
R29
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R165
R28
R26
TP7
J15
J14
edge of board
R24
R23
R22
R21
R20
R19
R18
R17
T9
C33
U10
RN3
TP6
C35
C32
U9
RN2
C29
U8
RN1
J13
J12
J11
J10
J9
J7
J6
J4
J3
J2
PANEL EDGE
EDGE OF PCB
T1
T3
T2
T4
T5
T7
T6
T8
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L3
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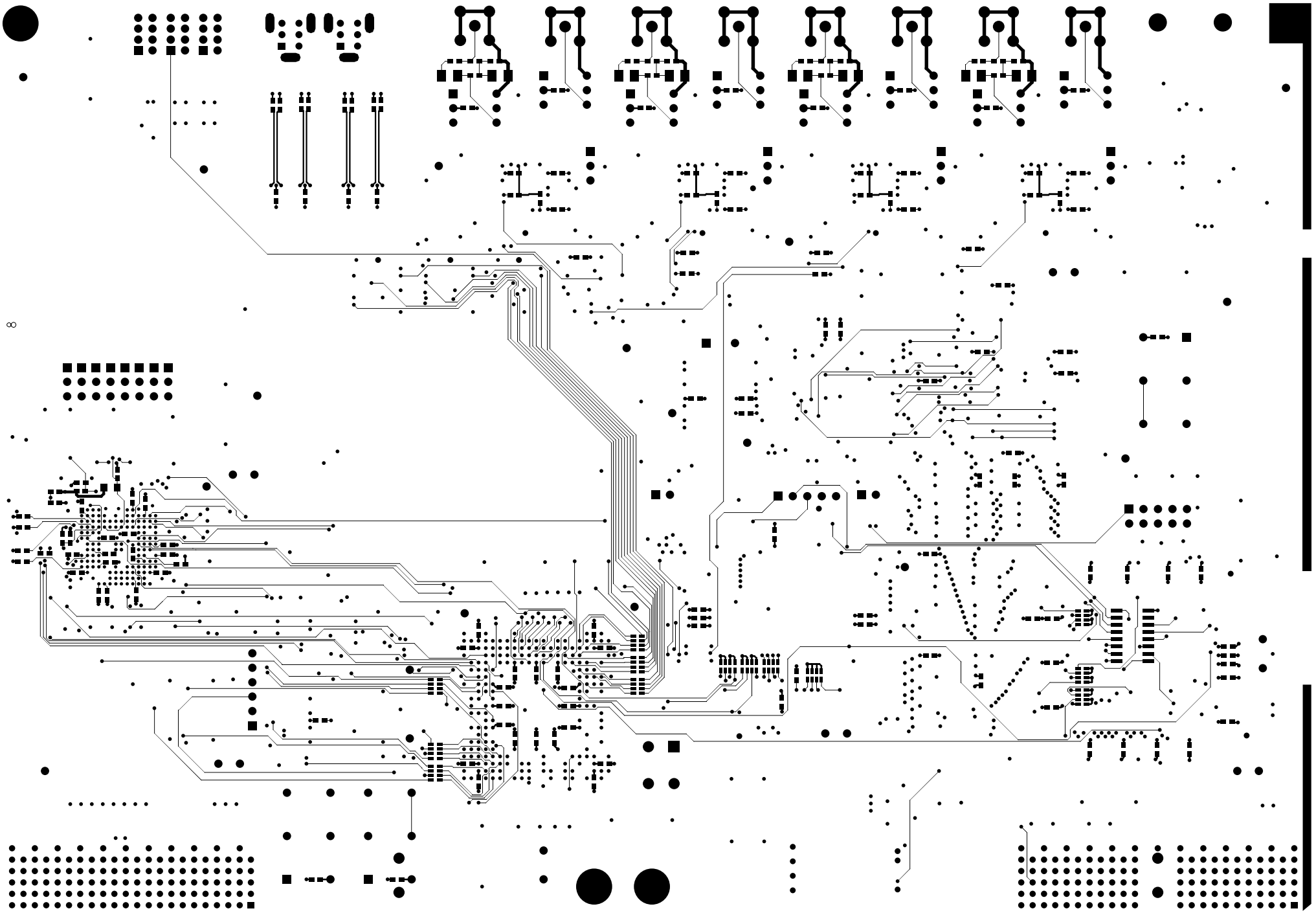
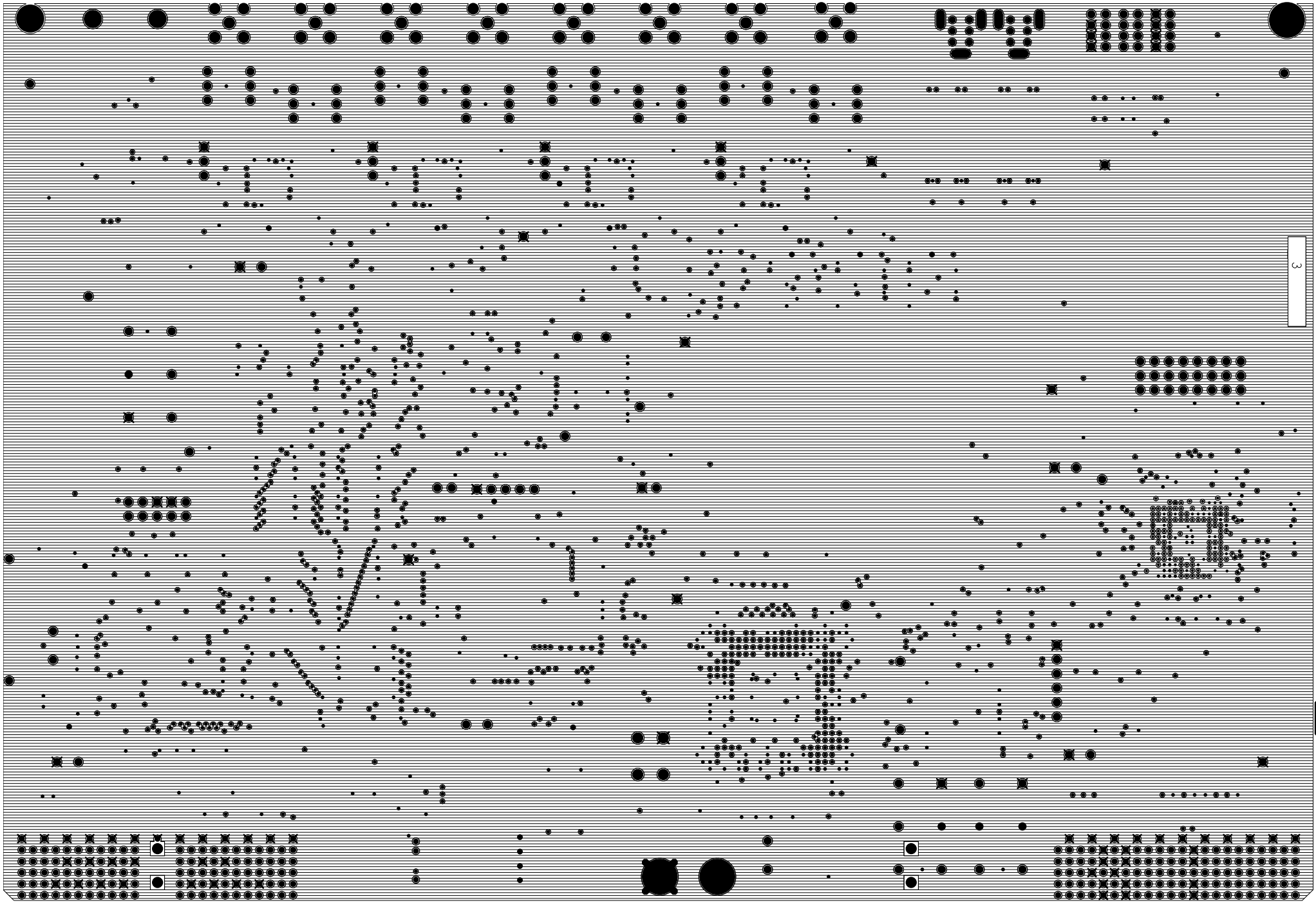
R90
R89
R88
TP31
R121
R119
R118
R116
R115
R113
R112
R110
R120
R117
R114
R111
J5
C65
C64
TP30
R109
R108
R107
TP29
J28
TP17
C49
R61
R62
D4
R87
C63
R86
D6
C36
TP16
TP12
TP15
R85
C62
U24
R84
RN7
Y5
C61
U23
Y4
R82
R83
C60
C59
TP24
R81
TP28
TP23
C79
C45
U22
R80
R79
R78
R77
R76
R75
R106
R105
R104
R103
TP27
TP32
M2
M3
TP22
SW1
C48
TP11
C47
R51
C34
C46
R60
J27
TP10
C44
R59
Y2
U14
Y3
TP9
U21
SOCKET
C78
C77
C76
C75
U13
SOCKET
RN4
J26
J25
R58
TP14
TP21
TP20
R102
Q2
U26
C74
R99
R100
R101
R98
C43
C57
C58
U25
C73
Q1
R97
R95
R96
C72
U12
U16
U19
U20
C42
U11
U15
R94
C70
C71
C68
C69
R57
TP13
R56
R55
R54
R53
J24
Y1
U18
R93
J1
edge of board
TP8
C41
TP18
C56
TP19
R73
R74
TP26
R92
TP25
C67
C66
R52



GND PLANE



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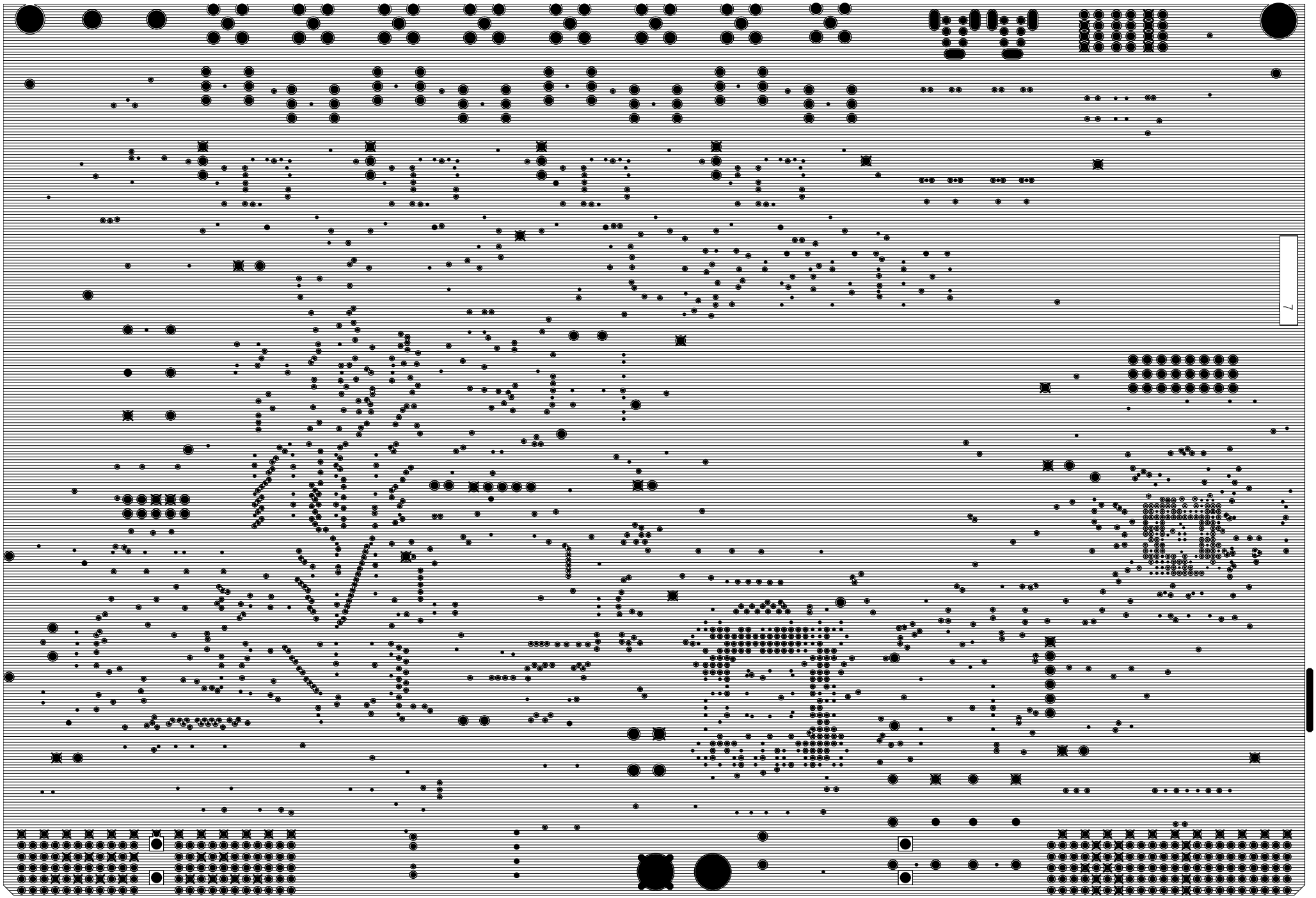
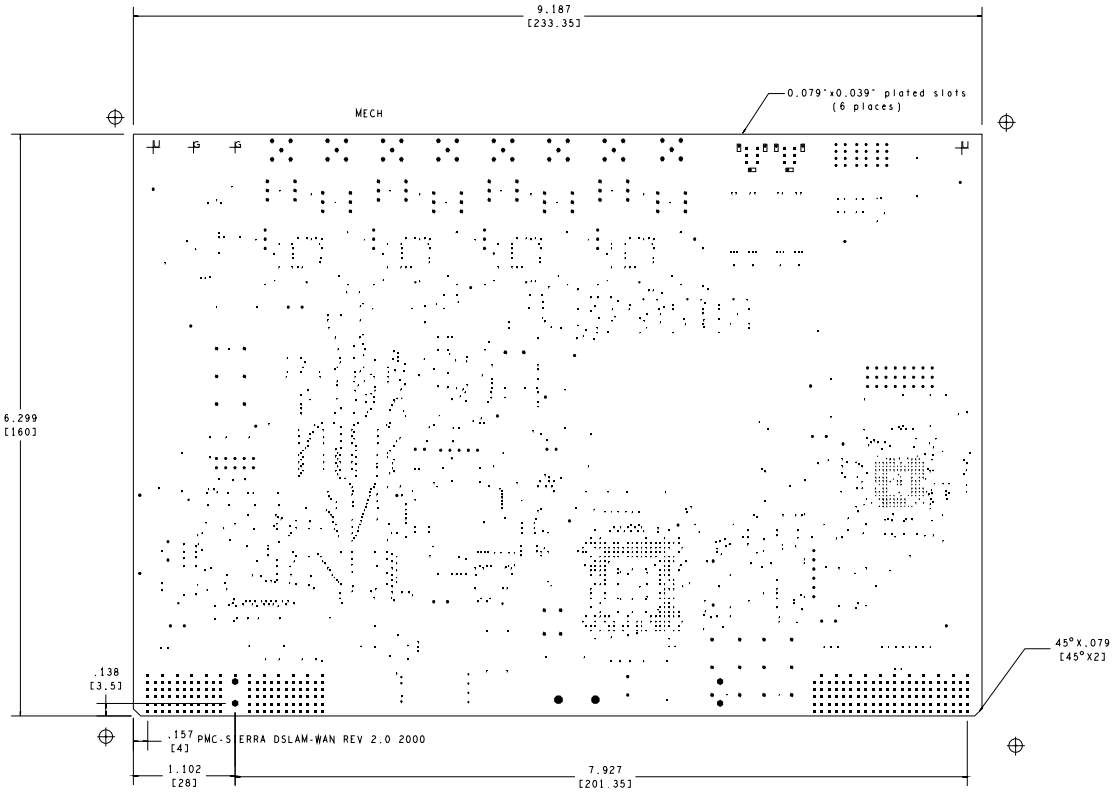


PMC-SIERRA DSLAM_WAN REV 2.0 2000

REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED



ARTWORK FILM
TOP LAYER
GROUND PLANE
3V3 PLANE
SIG1 LAYER
SIG2 LAYER
5V PLANE
GNDD PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
SOLDER PASTE TOP
SOLDER PASTE BOTTOM
MECH DRAWING
ASSY TOP
ASSY BOTTOM

FINISHED HOLES SIZE			
All Units are in mils			
FIGURE	SIZE	PLATED	QTY
·	12.0	PLATED	159
·	13.0	PLATED	1300
·	25.0	PLATED	19
·	26.0	PLATED	244
·	32.0	PLATED	12
·	36.0	PLATED	117
·	39.0	PLATED	6
·	39.37	PLATED	2
·	42.0	PLATED	72
·	52.0	PLATED	40
●	100.0	PLATED	2
⊕	149.606	PLATED	1
⊕	150.0	PLATED	1
●	78.74	NOT PLATED	4
⊕	128.0	NOT PLATED	2

Note: All 5 mils traces are 75 Ohms controlled inpedance.
All 11 mils are 50 Ohms controlled impedance.

Notes:

1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers.
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are spedified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
FR-4	DIELECTRIC	-------	-------	6 mil	4.5
COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	3.0 mil	4.5
COPPER	CONDUCTOR	3V3 PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	8 mil	4.5
COPPER	CONDUCTOR	SIG1	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	18 mil	4.5
COPPER	CONDUCTOR	SIG2	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	8 mil	4.5
COPPER	CONDUCTOR	5V_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	3 mil	4.5
COPPER	CONDUCTOR	GNDA PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	6 mil	4.5
COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------

UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN			
TOLERANCES ON:				
2 PL DECIMALS ±	CHECKED			
3 PL DECIMALS ±	ENGRG			
ANGLES ±	ISSUED			
FRACTIONS ±				
DOC# PMC-990474				
DOC ISSUE# 2				
REV # 2.0				
DATE:FEB 2000				

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Canada, V5A 4V7

Tel: 604 415-6000 Fax: 604 415-6200

SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF

DRAWING SUMMARY REPORT

W:\projects\dslam_wan_r2\pcb\dslam_wan.brd

Thu Feb 24 08:51:04 2000

Drawing Extents XL -5850.000 YL -6710.000 XU 16150.000 YU 10290.000
Dimensions in mils with 3 decimal places

Package Symbols: 514 Total 180 Mirrored 2736 Pins

Mechanical Symbols: 10 Total 6 Pins

Format Symbols: 1

DRC: 0 Errors

Padstacks: 66 Definitions

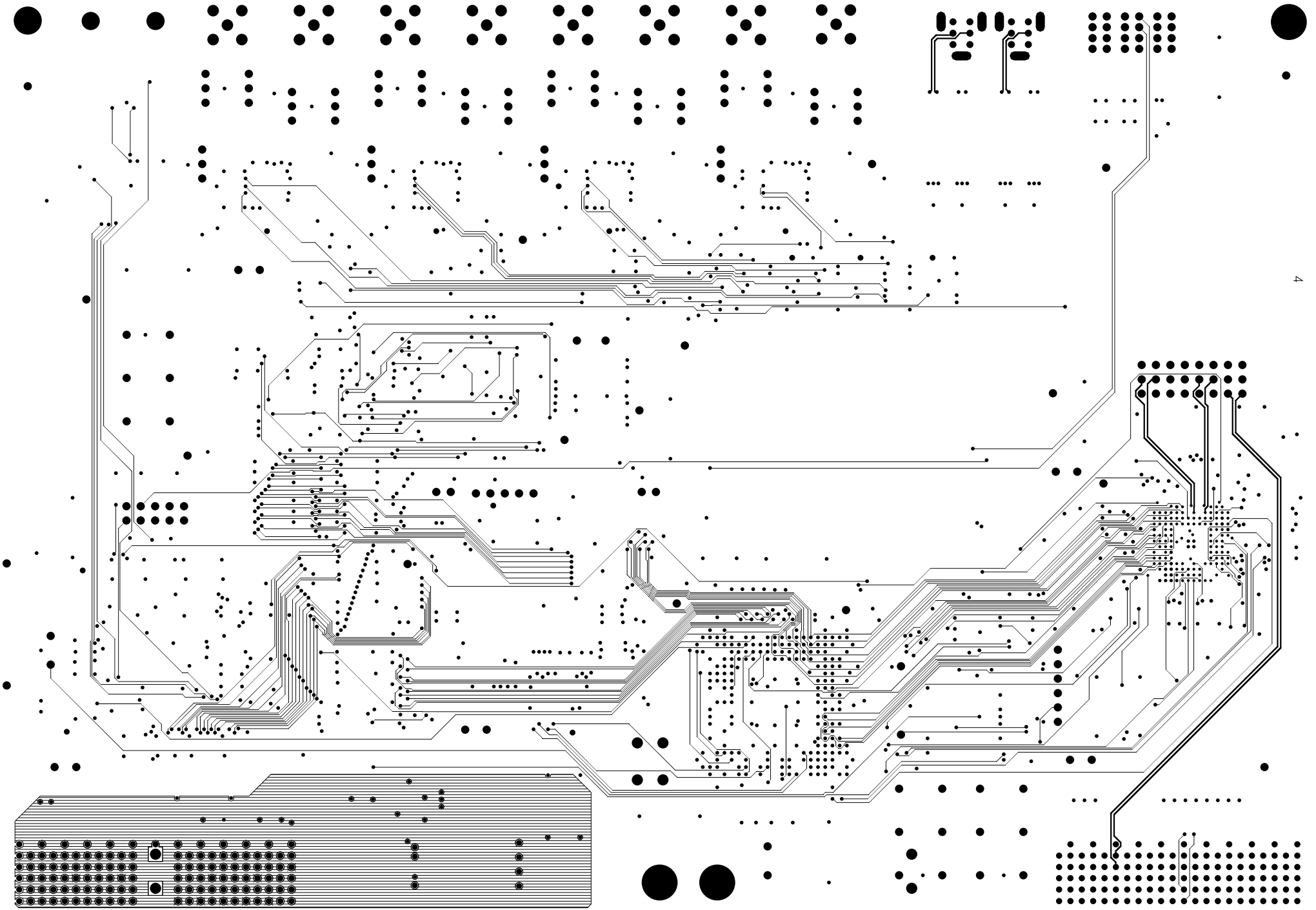
Functions: Assigned 603 Unassigned 0 Total 603

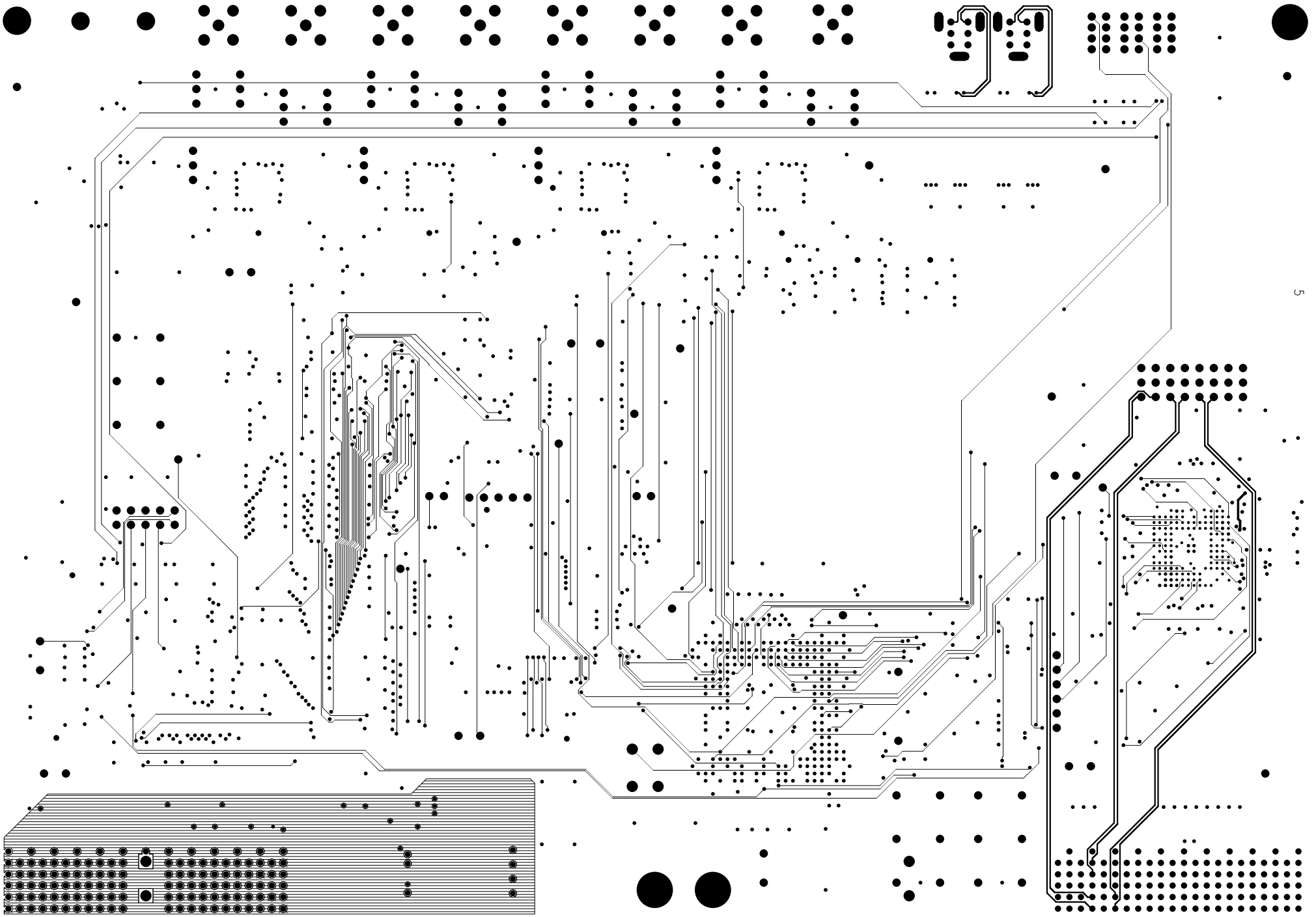
Layout Statistics:

Components: Placed 514 Unplaced 0 Total 514
Nets: W/Rats 578 No/Rats 3 Total 581
Pins: W/Rats 1578 No/Rats 845 Unused 313 Unplaced 0 Total 2736
Equivalent ICs (1 pin = 1/14 EIC) 195
RatTs 0

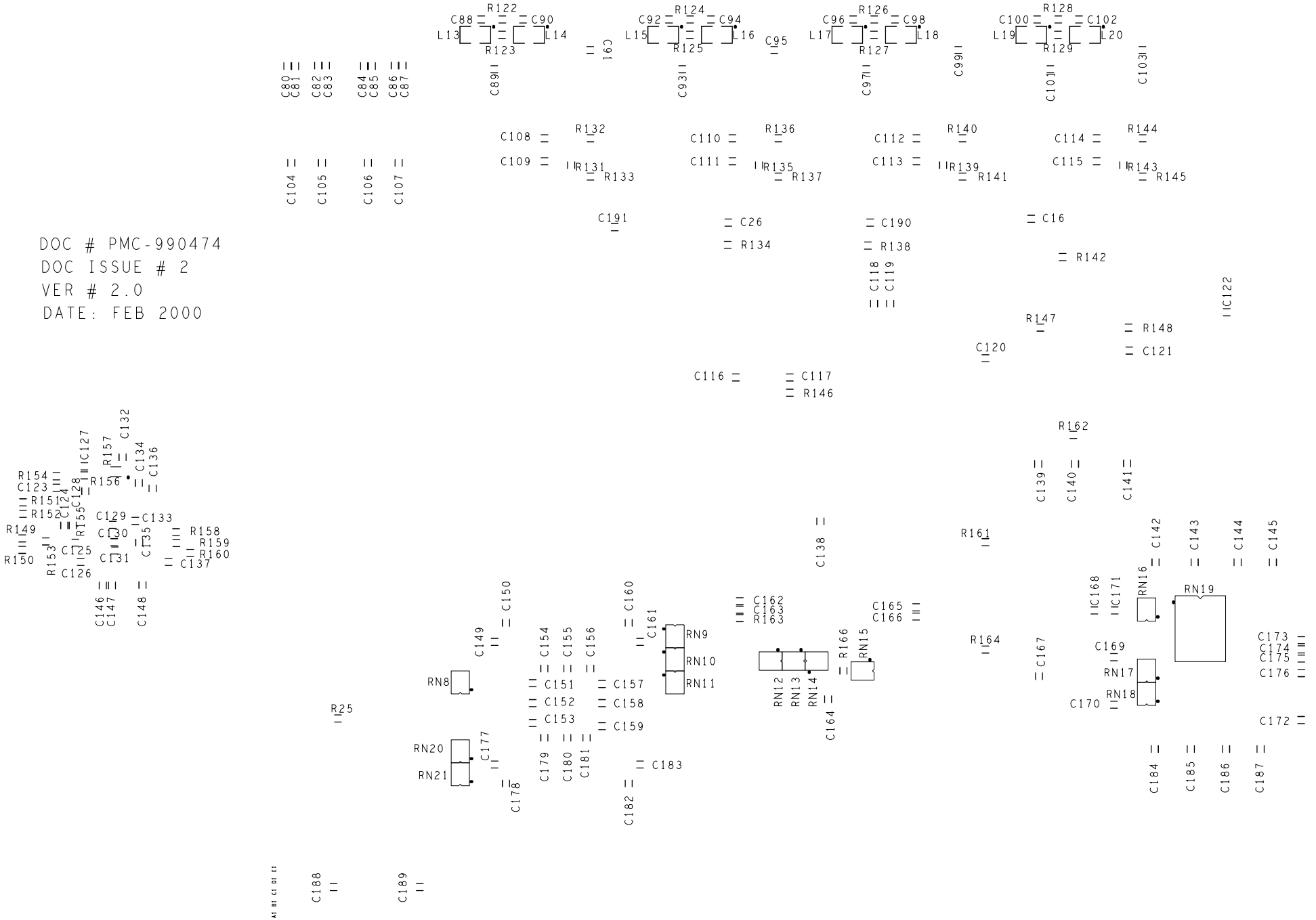
Connection Statistics:	W/Rats	No/Rats	Total
Connections	1000	842	1842
Already Connected	1000	842	1842
Missing Connections	0	0	0
Dangling Connections (See logfile)			1
Connection Completion	100.00%	100.00%	100.00%
Manh Distance (inches)	1094.75		
Etch Length (inches)	1101.49	73.30	1174.80
Number of vias	856	628	1484
Vias per Connection	0.86	0.75	0.81
Smd pins with attached clines			2096

Etch:	#connect lines/arcs	#shapes (voids)	#rect-angles	#non-connect lines/arcs	#text
TOP	1686	5(16)	0	1	3
GND_PLANE	338	1(1441)	0	1	3
3_3V_PLANE	16	1(1701)	0	1	3
SIG1	256	1(144)	0	1	3
SIG2	200	1(142)	0	1	3
5V_PLANE	40	1(1666)	0	1	3
GNDD_PLANE	338	1(1441)	0	1	3
BOTTOM	583	0(0)	0	1	3
etch totals	3457	11(6551)	0	8	24

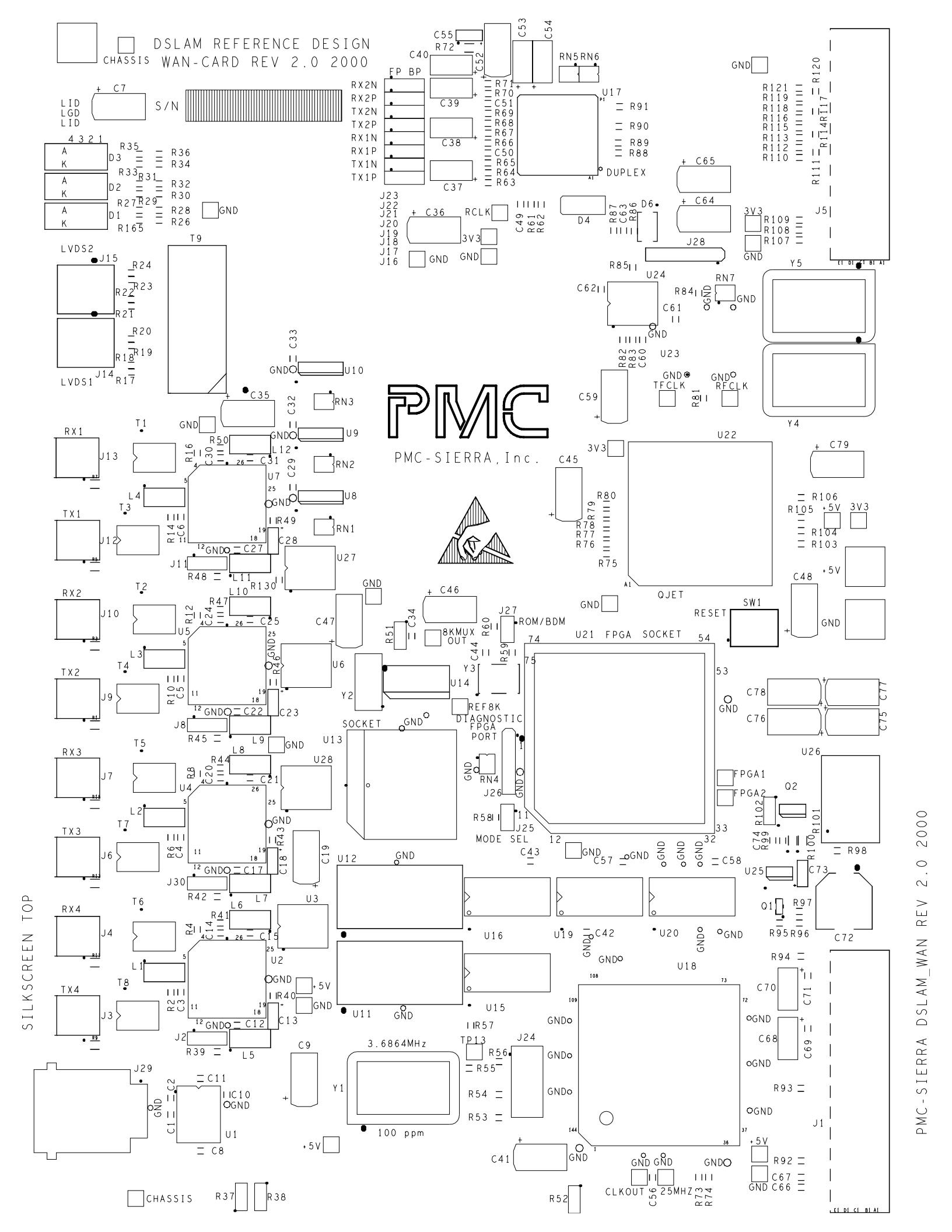




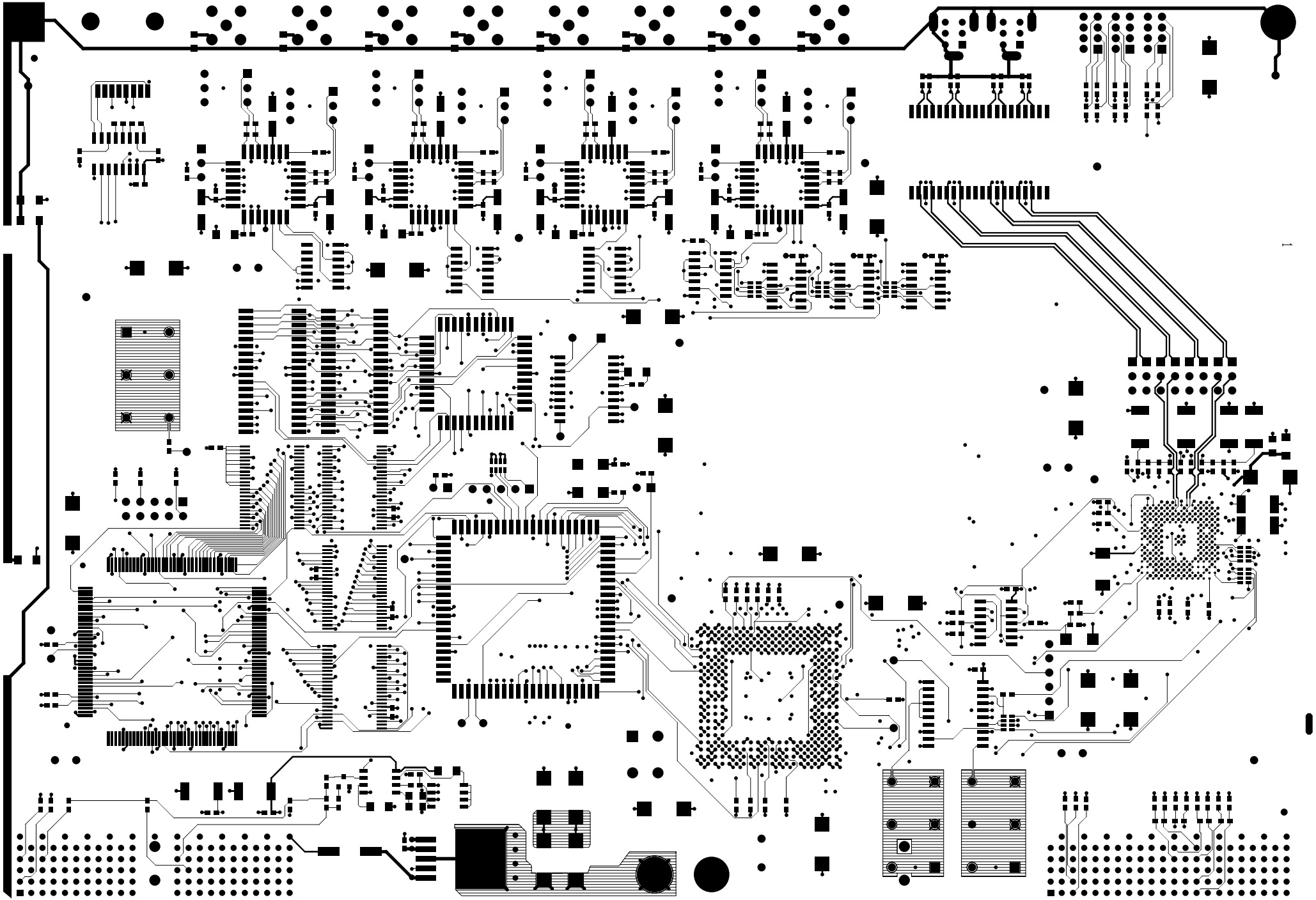
SILKSCREEN BOTTOM



DOC # PMC-990474
DOC ISSUE # 2
VER # 2.0
DATE: FEB 2000


DSLAM REFERENCE DESIGN
CHASSIS WAN-CARD REV 2.0 2000
PMC
PMC-SIERRA, Inc.
SILKSCREEN TOP
PMC-SIERRA DSLAM_WAN REV 2.0 2000
QJET
DUPLEX
FPGA SOCKET
SOCKET
DIAGNOSTIC
MODE SEL
RESET
ROM/BDM
8KMUX
REF8K
FPGA PORT
FP BP
LVDS1
LVDS2
CLKOUT 25MHZ
3.6864MHz
100 ppm
TFCLK
RFCLK
RCLK
GND
3V3
+5V

TOP LAYER



PMC-SIERRA DSLAM_WAN REV 2.0 2000

DRAWING SUMMARY REPORT

W:\projects\dslam_wan_r2\pcb\dslam_wan.brd

Thu Feb 24 08:51:04 2000

End Summary Report

13 APPENDIX D: VHDL CODE FOR FPGA

```
-- ------------------------------------------------------------------------
-- ------------------------------------------------------------------------
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--
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-- PMC-Sierra, Inc.
-- 105 - 8555 Baxter Place
-- Burnaby, B.C.
-- Canada   V5A 4V7
-- Tel: 604-415-6000
-- Fax: 604-415-6206
-- email: apps@pmc-sierra.com
-- ------------------------------------------------------------------------
-- Project          : PMC-1990474
-- File Name        : dslam_wan_top.vhd
-- Path             :
-- Designer         : XX
--
-- Revision History
-- Issue     Date         Initials     Description
-- 1         08/17/99     XX           Initial Release
--
-- 2         11/16/99     XX           Update
--
-- 3         07/04/00     XX           Final Release
--
-- Function
-- This is the top level of the VHDL code required for the DSLAM WAN
-- reference design.  The code provides for microprocessor bus logic
-- and creates various multiplexers.
-------------------------------------------------------------------------

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

library a42mx;
use a42mx.all;

ENTITY dslam_wan_top IS
  port (
    resetb : IN STD_LOGIC;
    ref8k0_qjet : IN STD_LOGIC_VECTOR (3 downto 0);
    lfkout_duplex : IN STD_LOGIC;
    t3_rclk : IN STD_LOGIC_VECTOR (3 downto 0);
    ds3mout : IN STD_LOGIC;
    sys_clk : IN STD_LOGIC;
    a_ml : IN STD_LOGIC_VECTOR(7 downto 0);
    a_mu : IN STD_LOGIC_VECTOR(17 downto 15);
```

```
    d : IN STD_LOGIC_VECTOR(7 downto 0);
    cs0b : IN STD_LOGIC;
    cs1b : IN STD_LOGIC;
    cs2b : IN STD_LOGIC;
    cs3b : IN STD_LOGIC;
    dsb : IN STD_LOGIC;
    asb : IN STD_LOGIC;
    siz0 : IN STD_LOGIC;
    rwb_m : IN STD_LOGIC;
    mode : IN STD_LOGIC;

    test_point1 : OUT STD_LOGIC;
    test_point2 : OUT STD_LOGIC;

    lfmux_out : OUT STD_LOGIC;
    qjet_ticlk : OUT STD_LOGIC_VECTOR (3 downto 0);
    deb_mem : OUT STD_LOGIC;
    rdb : OUT STD_LOGIC;
    wrb : OUT STD_LOGIC;
    csb_qjet : OUT STD_LOGIC;
    csb_duplex : OUT STD_LOGIC;
    uweb : OUT STD_LOGIC;
    lweb : OUT STD_LOGIC;
    oeb : OUT STD_LOGIC
      );
end dslam_wan_top;

ARCHITECTURE dslam_wan_top_arch OF dslam_wan_top IS

CONSTANT lfREG : INTEGER := 1;
CONSTANT ds3REG : INTEGER := 0;

TYPE regtype IS array (0 to 1) OF STD_LOGIC_VECTOR(7 downto 0);

SIGNAL fpga: regtype;
SIGNAL write : STD_LOGIC;
SIGNAL read : STD_LOGIC;

SIGNAL lf_mux_int : STD_LOGIC;

begin


-- This process is used to write to the FPGA's internal registers.  Data is
-- written into the FPGA on the falling edge of dsb, coming from the
-- microprocessor. The dsb signal indicates that stable data is present
-- on the data bus.


process (resetb, dsb)
  begin
    IF resetb = '0' THEN
       fpga(ds3REG) <= "00000000";
       fpga(lfREG) <= "00000000";
    ELSIF (dsb = '0') AND (cs2b = '0') AND (a_mu(17 DOWNTO 15) = "110") AND
(rwb_m = '0') THEN
      IF a_ml = "00000000" THEN
        fpga(ds3REG) <= d;
      ELSIF a_ml = "00000001" THEN
        fpga(lfREG) <= d;
      END IF;
    END IF;
  end process;

-- Optional - For FPGA register debugging purposes
test_point1 <= fpga(ds3REG)(7);
test_point2 <= fpga(lfREG)(7);
```

```
-- Lower 8 bit ram write enable
lweb <= NOT (((NOT siz0) OR (a_ml(0))) AND (NOT cs1b) AND (NOT rwb_m)) WHEN mode = '1'
       ELSE NOT (((NOT siz0) OR(a_ml(0))) AND (NOT (cs1b AND cs0b)) AND (NOT rwb_m));

-- Upper 8 bit ram write enable
uweb <= NOT ((NOT rwb_m) AND (NOT a_ml(0)) AND (NOT cs1b)) WHEN mode = '1'
       ELSE NOT ((NOT rwb_m) AND (NOT a_ml(0)) AND (NOT (cs1b AND cs0b)));

-- Ram output enable
oeb <= NOT (rwb_m AND (NOT cs1b)) WHEN mode = '1'
       ELSE NOT (rwb_m AND (NOT (cs1b AND cs0b)));

-- Duplex & Qjet write
wrb <= rwb_m;

-- Duplex & Qjet read
rdb <= not rwb_m;

-- Active for all memory operations
deb_mem <= cs0b AND cs1b;

-- QJET chip select
csb_qjet <= NOT ((NOT cs2b) AND (NOT a_mu(15)) AND (a_mu(16)) AND (NOT a_mu(17)));

-- DUPLEX chip select
csb_duplex <= NOT ((not cs2b) AND (NOT a_mu(15)) AND (NOT a_mu(16)) AND (a_mu(17)));

-- 8kHz multiplexor intermediate signal
lf_mux_int <= ref8k0_qjet(0) WHEN ( (fpga(lfREG)(0) = '0') AND (fpga(lfREG)(1) = '0'))
      ELSE ref8k0_qjet(1) WHEN ((fpga(lfREG)(0) = '1') AND (fpga(lfREG)(1) = '0'))
      ELSE ref8k0_qjet(2) WHEN ((fpga(lfREG)(0) = '0') AND (fpga(lfREG)(1) = '1'))
      ELSE ref8k0_qjet(3);

-- 8kHz multiplexor output
lfmux_out <= lfkout_duplex WHEN fpga(lfREG)(7) = '1'
             ELSE lf_mux_int;

-- 44.736 MHz multiplexor outputs
qjet_ticlk(3) <= t3_rclk(3) WHEN ((fpga(ds3REG)(7) = '0') AND (fpga(ds3REG)(6) = '0'))
              ELSE ds3mOUT WHEN ((fpga(ds3REG)(7) = '0') AND (fpga(ds3REG)(6) = '1'))
              ELSE sys_clk WHEN ((fpga(ds3REG)(7) = '1') AND (fpga(ds3REG)(6) = '0'))
              ELSE 'Z';

qjet_ticlk(2) <= t3_rclk(2) WHEN ((fpga(ds3REG)(5) = '0') AND (fpga(ds3REG)(4) = '0'))
              ELSE ds3mOUT WHEN ((fpga(ds3REG)(5) = '0') AND (fpga(ds3REG)(4) = '1'))
              ELSE sys_clk WHEN ((fpga(ds3REG)(5) = '1') AND (fpga(ds3REG)(4) = '0'))
              ELSE 'Z';

qjet_ticlk(1) <= t3_rclk(1) WHEN ((fpga(ds3REG)(3) = '0') AND (fpga(ds3REG)(2) = '0'))
              ELSE ds3mOUT WHEN ((fpga(ds3REG)(3) = '0') AND (fpga(ds3REG)(2) = '1'))
              ELSE sys_clk WHEN ((fpga(ds3REG)(3) = '1') AND (fpga(ds3REG)(2) = '0'))
              ELSE 'Z';

qjet_ticlk(0) <= t3_rclk(0) WHEN ((fpga(ds3REG)(1) = '0') AND (fpga(ds3REG)(0) = '0'))
              ELSE ds3mOUT WHEN ((fpga(ds3REG)(1) = '0') AND (fpga(ds3REG)(0) = '1'))
              ELSE sys_clk WHEN ((fpga(ds3REG)(1) = '1') AND (fpga(ds3REG)(0) = '0'))
              ELSE 'Z';

end dslam_wan_top_arch;
```

14 NOTES

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