PM5357

S/UNI-622-POS

SATURN USER NETWORK INTERFACE (622-POS)

REFERENCE DESIGN

PROPRIETARY AND CONFIDENTIAL

PRELIMINARY

ISSUE 2: FEBRUARY 2000

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
2	January 2000	Rev 2 to Rev 3 schematic change: Removed the analog 8KHz t o77.76MHz PLL. The reference designations on the Issue 3 schematics match those on the Rev 1 PCB. At this time, there are no plans to build a PCB to Issue 3 schematics.
1.5	August 2000	Rev 1 to Rev 2 schematic change to support uP cPCI: Removed WAN clocking, removed local uP in lieu of the cPCI I/F, analog 8KHz to 77.76MHz PLL was added for internal testing, replaced 5V to 3.3V Linear regulator filter for S/UNI-622-POS analog power pins with RC passive 3.3V filters, add programmable FPGA for drop side ATM/Packets. Rev 1 PCB was fabricated to Rev 2 schematics. Issue 1.5 document was never issued.
1	Nov 1998	Document created with Rev 1 Schematics. No PCB made to Rev 1 Schematics. Only a paper design. Document posted on intranet.

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1 INTRODUCTION

The PM5356 S/UNI-622-MAX performs ATM processing and the PM5357 S/UNI-622-POS performs both ATM processing and Packet Over SONET (POS). Both these devices have the same footprint and they are pin for pin compatible. Even though only reference to the PM5357 is made, this document relates to both the devices

The PM5357 S/UNI-622-POS standard product is a SATURN User Network Interface with SONET/SDH processing, ATM and Packet mapping functions at the STS-12c (STM-4-4c) 622.08 Mbit/s rate. This chip also features an integral CRU and CSU for clock/data recovery and generation. The S/UNI-622-POS is intended for use in equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interface (UNI), ATM Network-Network Interfaces (NNI), and Packet Over SONET/SDH (POS) interfaces. The POS interface can be used to support several packet based protocols, including the Point-to-Point Protocol (PPP). The S/UNI-622-POS may find application at either end of switch-to-switch links or switch-to-terminal links, both in public network (WAN) and private network (LAN) situations.

This S/UNI-622-POS reference design provides a physical interface implementation of a SONET/SDH line card for both ATM and POS applications. It provides one single-mode or multi-mode optical interface, 5V or 3.3 V, at OC-12c rate and a UTOPIA Level 2, 50MHz, 16-bit wide bus system side synchronous interface. The onboard programmable FPGA provides a simple means to manipulate ATM cells and POS packets.

The PM5357 S/UNI-622-POS features two drop side synchronous interfaces. For ATM applications, standard 50 MHz, 16 bit UTOPIA Level 2 and 100MHz, 8-bit UTOPIA Level 3 interfaces are provided. For POS (Packet over SONET) designs, a SATURN compliant POS-PHY Level 2 and Level 3 interface is used. More on this interface is explained later in this document.

This POS Reference board implements a subset of the full capabilities of the S/UNI-622-POS and this board does not support APS.

Both the PM5357 and the PM5356 are packaged in a 304 pin Super Ball Grid Array (SBGA) as shown below.

For detailed information on these devices please refer to their respective data sheets. The terms cPCI and CompactPCI™ will be used interchangeably.

Figure 1: S/UNI-622POS Chip

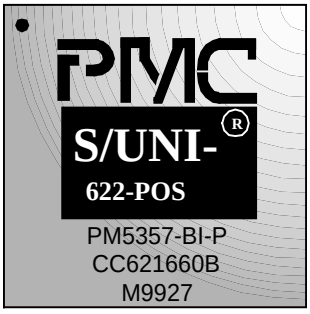
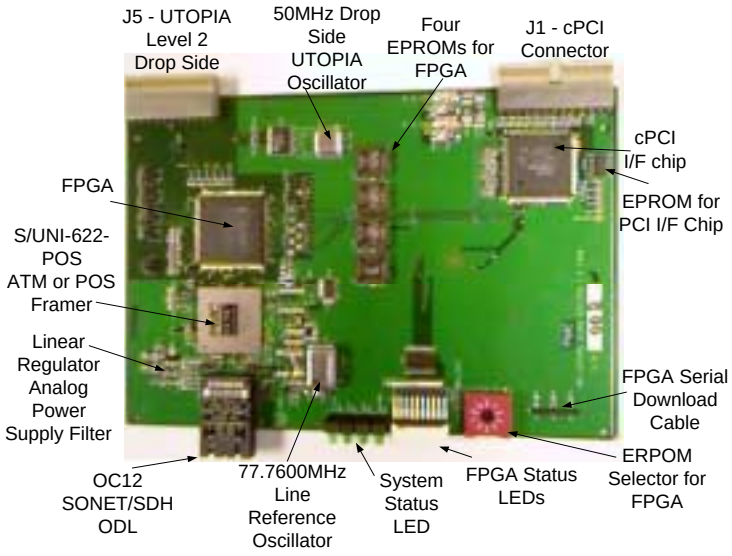


Figure 2: Picture of S/UNI-622-POS Reference Design PCB



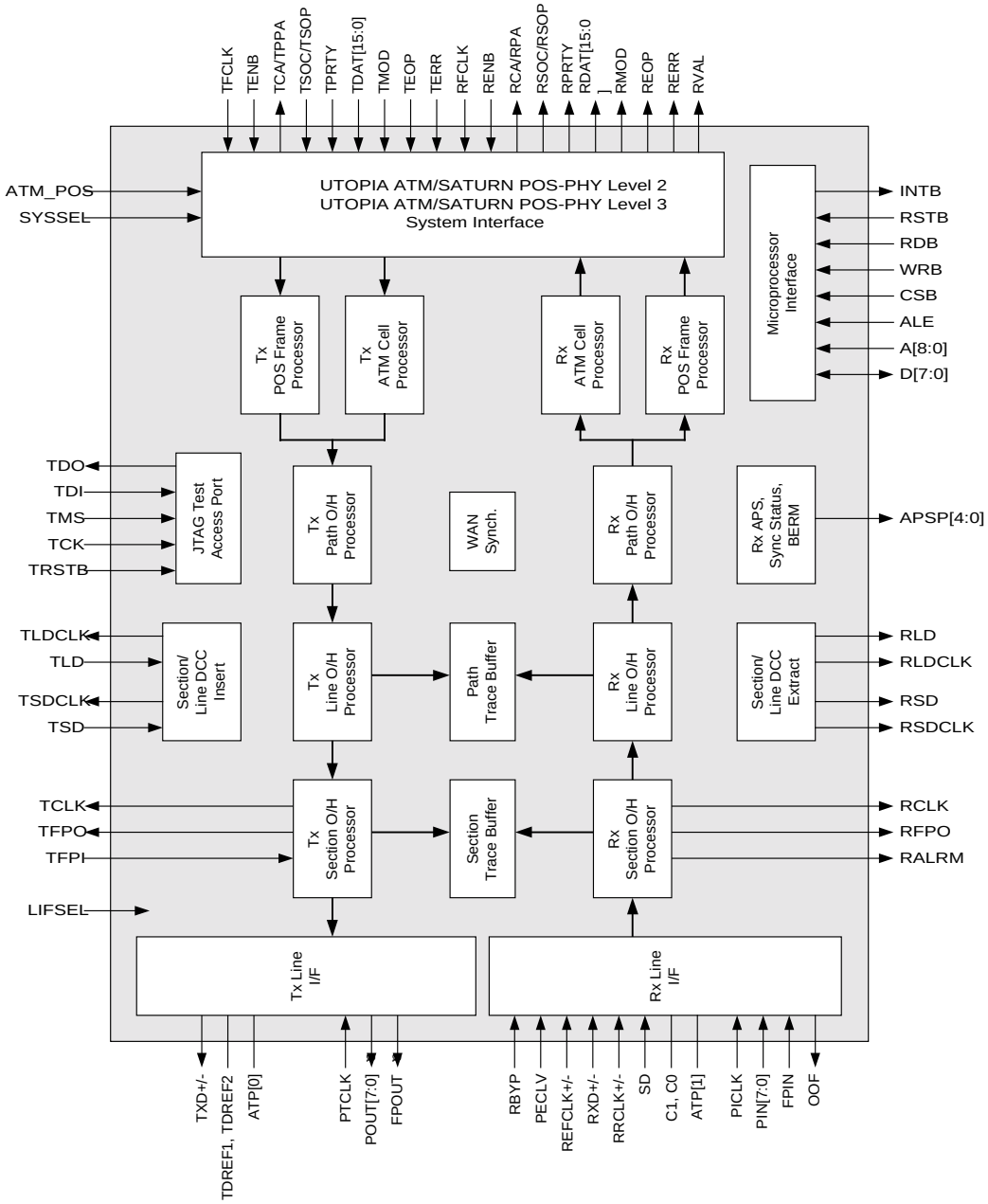
- Provides one single-mode or multi-mode OC-12c rate 622.08 Mbit/s SONET/SDH Physical Layer Port

- Provides a Utopia Level 2, 50 MHz, 16-bit ATM Single-PHY System Interface to the FPGA or cPCI J5.

- Provides a POS-PHY Level 2, 50 MHz, 16-bit Packet Over SONET/SDH Single-PHY System Interface to the FPGA or cPCI bus J5 connector.

2 S/UNI-622-POS BLOCK DIAGRAM

Figure 3: S/UNI-622-POS Block Diagram



3 APPLICATIONS

The S/UNI-622-POS reference design demonstrates the physical interface implementation for both ATM and POS applications. The list below shows the networking equipment that can incorporate the S/UNI-622-POS device:

- WAN and Edge ATM switches physical interfaces
- LAN switches and hubs physical interfaces
- Packet switches and hubs physical interfaces

The POS Reference Board can be used in four modes:

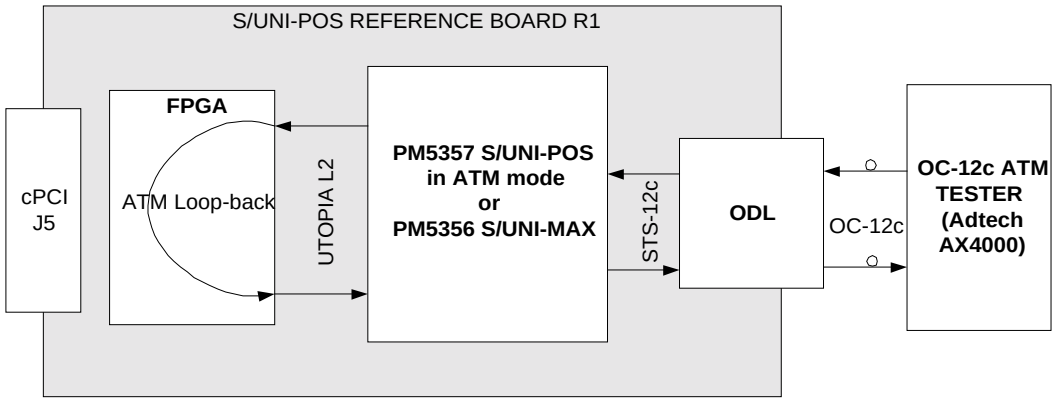
- Drop Side ATM Loop-Back
- ATM Transparent
- POS Generation/Receiving
- POS Transparent.

This S/UNI-622-POS reference PCB can be configured to demonstrate ATM drop side loopback, ATM transparent to the backplane, POS generation/receiving, and POS transparent to the backplane as described in more detail below.

3.1 ATM Drop Side Loop-Back

In an ATM application, the S/UNI-622-POS reference design interfaces to one OC-12c rate SONET/SDH signal on the line side. On the drop side, the S/UNI-622-POS interfaces directly to an FPGA that can be programmed to do drop side loop-back as shown in figure 1 below. An external ATM/SONET tester must generate ATM cells within SONET OC-12c frames. The POS device must be programmed for ATM mode by strapping the POS_ATMB pin (Y21) low. In addition, register 0x48, Transmit Path Signal Label, the SONET C2 byte, defaulted to 0x01, must be set to 0x13 to identify the payload to be ATM cells. The FPGA must be configured from the ATM Loop-back EPROM by selecting the correct EPROM via the dial up switch on the PCB before boot-up. The FPGA source VHDL code is enclosed in the Appendix at the end of this document.

Figure 4: ATM Drop Side Loop-Back

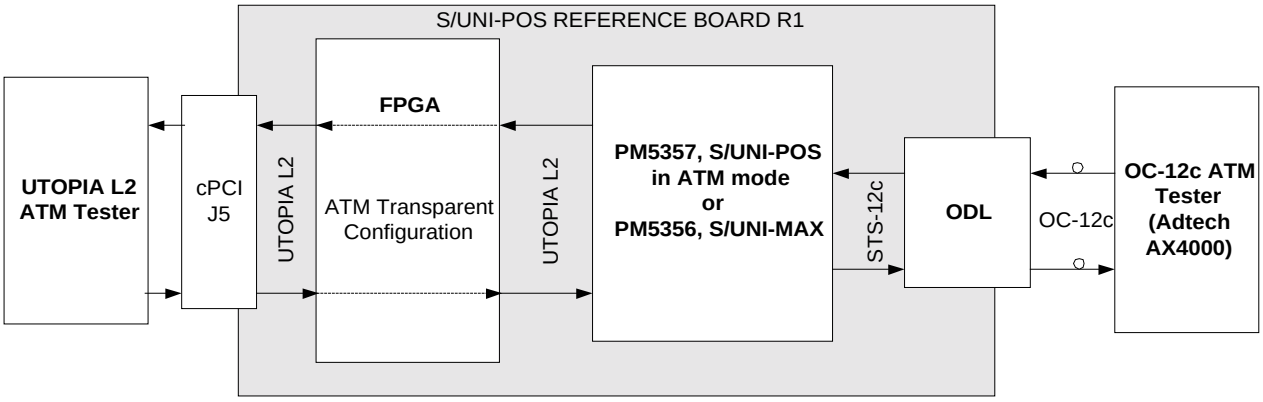


3.2 ATM Transparent

FPGA can also be configured to act like a transparent interface between the POS UTOPIA L2 and the cPCI J1 connector. The user can then connect a UTOPIA L2 compliant ATM Link layer device to the cPCI J1 connector and a SONET/ATM tester on the OC-12c side as shown in figure below.

Figure 5 below shows how the S/UNI-622-POS reference design can be used in a complete ATM switching design.

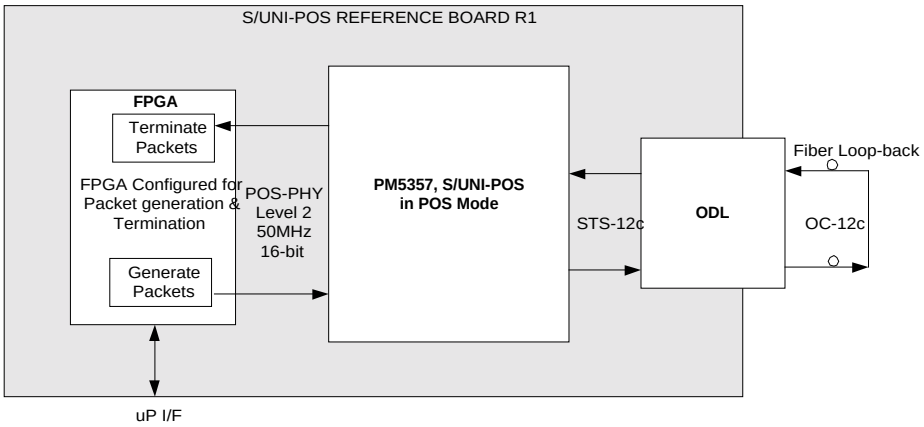
Figure 5: ATM Transparent



3.3 POS Source and Receive Packets

The FPGA can be configured to generate packets and compare these packets when they are looped back as shown below. In a Packet Over SONET/SDH application using the PPP protocol, the S/UNI-622-POS reference design interfaces to an OC-12c rate SONET/SDH signal on the line side. On the drop side, the S/UNI-622-POS reference design interfaces directly with an FPGA programmed to act as a link layer processor using a 256 byte synchronous FIFO SATURN POS-PHY Level 2 interface over which packets are transferred.

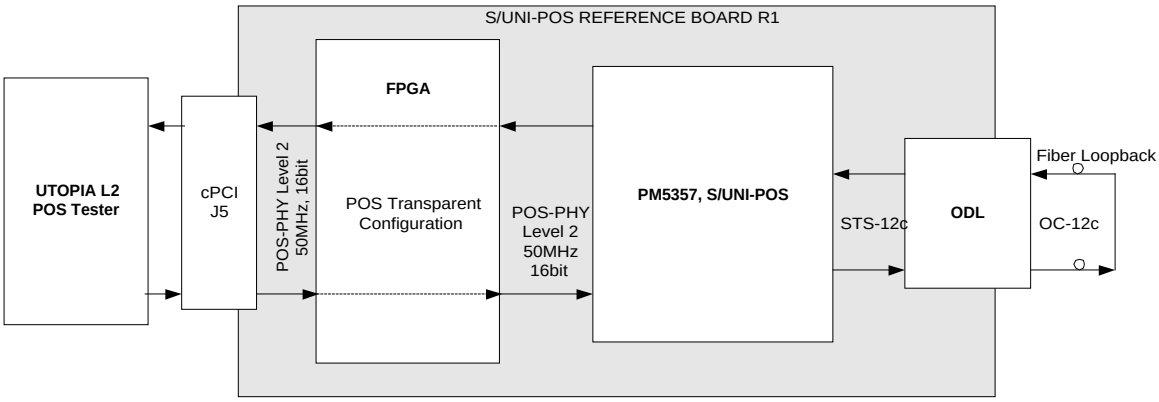
Figure 6: Packet generation and receiving using FPGA



3.4 POS Transparent

The FPGA can be configured to be packet transparent while connected to an external stand-alone SATURN compliant, POS-PHY tester or a POS link layer device.

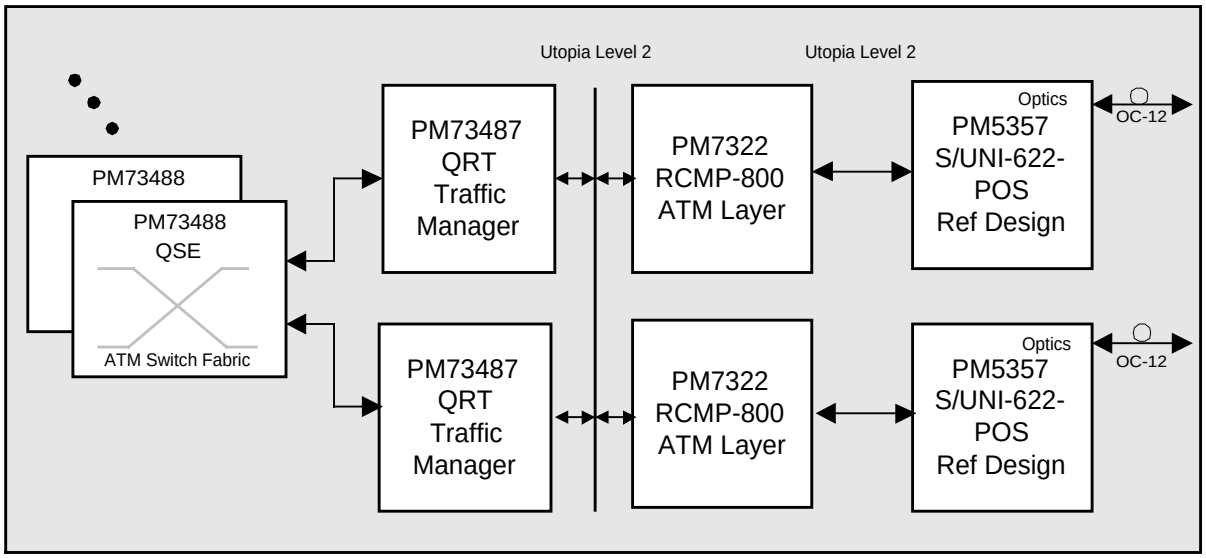
Figure 7: POS Transparent to backplane



3.5 Reference PCB with other PMC-Sierra ATM chips

This reference board can be potentially used within a larger system utilizing PMC-Sierra's ATM chip sets.

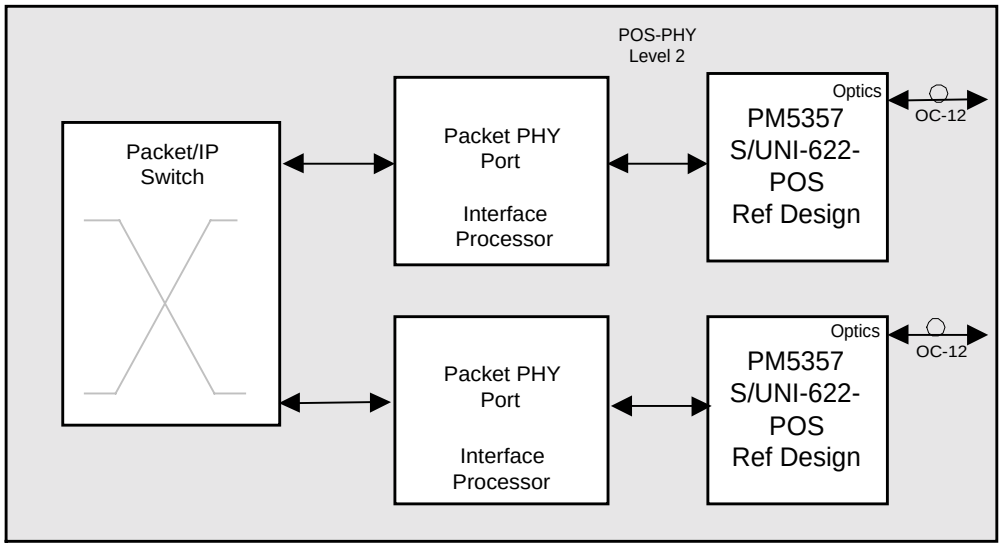
Figure 8: S/UNI-622-POS with PMC-Sierra ATM Chipsets



3.6 Using the Reference board with Packet Switch

This reference board can also be potentially used within a larger system utilizing packet switch and link layer processors as shown below.

Figure 9: S/UNI-622-POS Ref Design with POS Link Layer Device



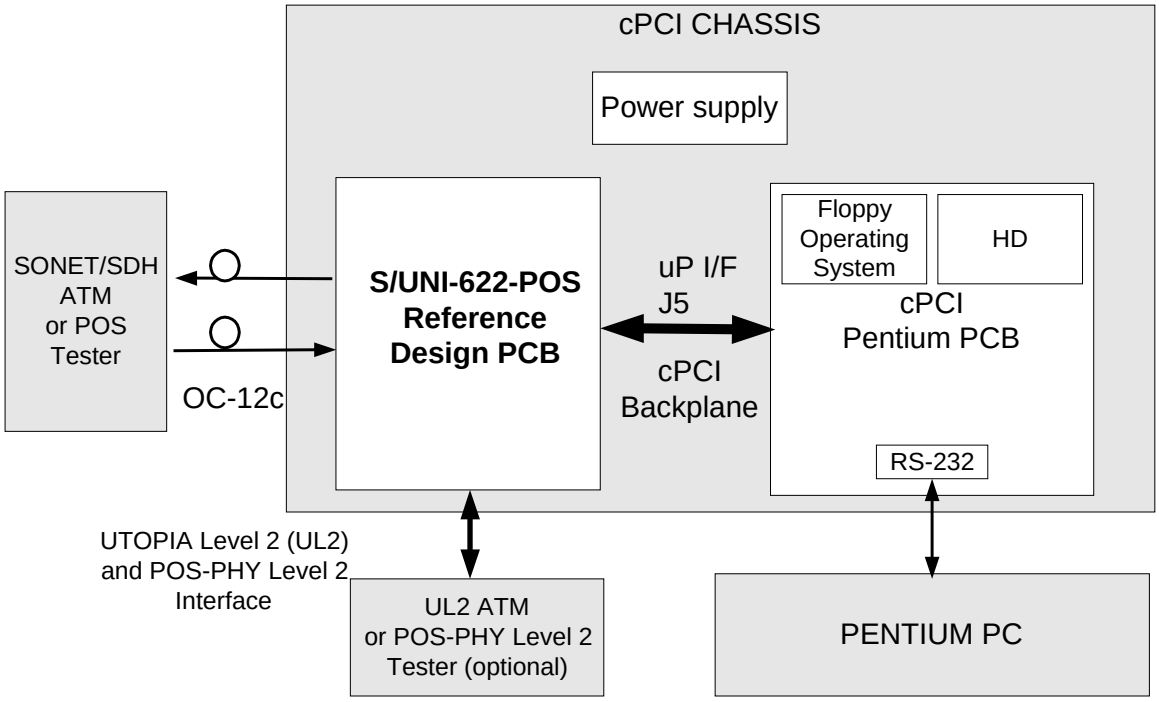
4 REFERENCES

- PMC-Sierra, Inc., PMC-980911 “PM5357 S/UNI-622-POS Data Sheet”, Issue 3, Jan. 15, 1999
- PMC-Sierra, Inc., PMC-980589 “PM5356 S/UNI-622-MAX Data Sheet”, Issue 4, Jan. 15, 1999
- Bell Communication Research – SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, December 1995
- CompactPCI™ specification, PICMG 2.0 R2.1, September 2, 1997.
- ATM Forum - AF-PHY-0039.00, “UTOPIA Level 2, Version 1.0”, June, 1995.
- ATM Forum - STR-PHY-UL3-01.00, “UTOPIA Level 3”, April, 1999
- PMC-Sierra’s web site for this device, the IBIS models, BSDL file, and drivers can be found on PMC-Sierra’s Internet Site.
- Digital High Speed Design, A Handbook of Black Magic, Prentice Hall PTR, by Howard W. Johnson, Martin Graham,

5 SYSTEM FUNCTIONAL DESCRIPTION

This Reference Design Board utilized a cPCI form factor hence it may only be tested within the cPCI environment. This system is composed of a cPCI chassis, the POS Reference PCB, Pentium PCI board with operating system SW, and an external Pentium PC with dumb terminal software. In addition an external SONET ATM and/or POS tester is required to generate and receive ATM or POS data to/from the S/UNI-622-POS framer.

Figure 10: SYSTEM LEVEL BLOCK Diagram

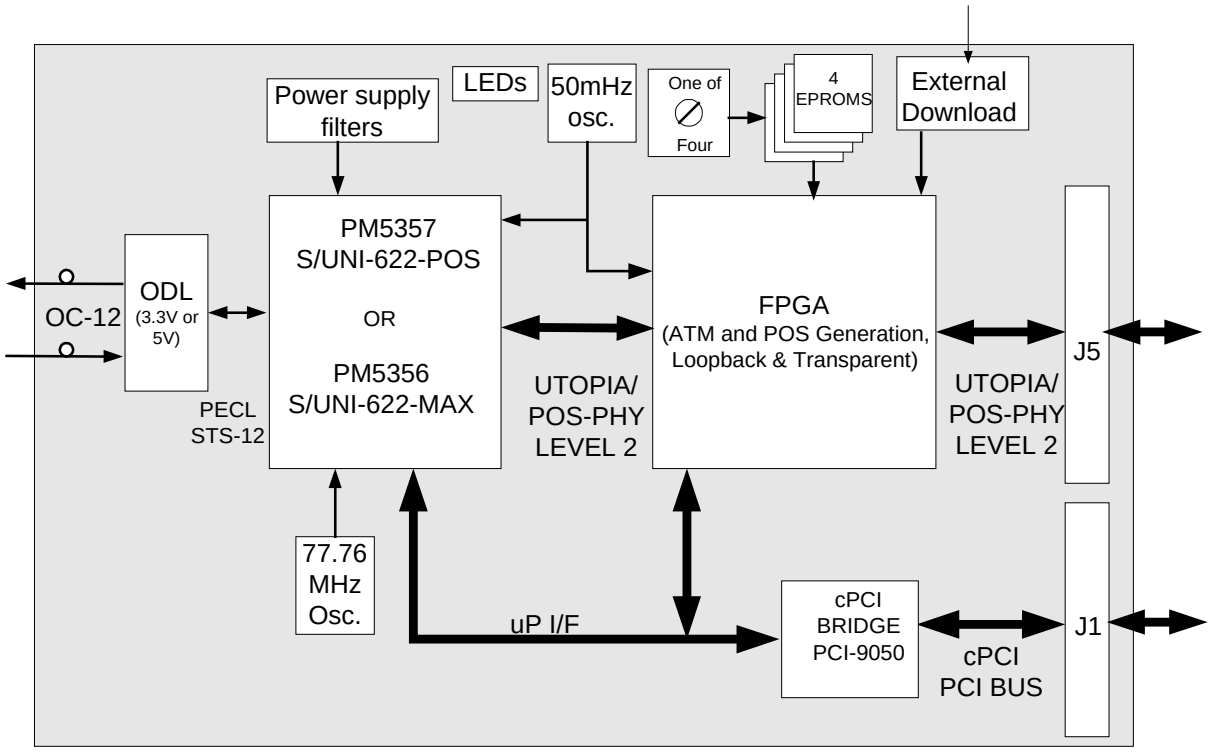


6 FUNCTIONAL DESCRIPTION

6.1 BLOCK DIAGRAM

The figure below shows the major components on the reference design.

Figure 11: Reference Design Block Diagram



6.2 S/UNI-622-POS

The PM5357 S/UNI-622-POS and the PM5356 S/UNI-622-MAX are very similar devices. The PM5356 implements ATM framing and the PM5357 implements ATM and POS framing. These SATURN User Network Interfaces are monolithic integrated circuits that implement SONET/SDH processing, ATM mapping and Packet Over SONET/SDH mapping functions at the STS-12c/STM-4-4c, 622.08 Mbit/s rate.

The S/UNI-622-POS receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section, line, and path overhead. The S/UNI-622-POS can also be configured for clock and data recovery and clock synthesis by-pass where it receives SONET/SDH frames via a byte-serial interface.

When used to implement an ATM UNI or NNI, the PM5357 S/UNI-622-POS and the PM5356 S/UNI-622-MAX frame to the ATM payload using cell delineation.

When used to implement packet transmission over a SONET/SDH link, the PM5357 S/UNI-622-POS, extracts Packet Over SONET/SDH (POS) frames from the SONET/SDH synchronous payload envelope.

The S/UNI-622-POS transmits SONET/SDH streams using a bit serial interface. This framer chip can also be configured for clock and data recovery and clock synthesis by-pass where it transmits the SONET/SDH frames via a byte-serial interface.

When used to implement an ATM UNI or NNI, ATM cells are written to an internal four cell FIFO using a 16-bit wide UTOPIA Level 2 (clocked up to 50 MHz) or an 8-bit wide Utopia Level 3 compatible (clocked up to 100 MHz) datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one complete cell.

When used to implement a Packet over SONET/SDH link, the S/UNI-622-POS inserts POS frames into the SONET/SDH synchronous payload envelope. Packets to be transmitted are written into a 256-byte FIFO through a 16-bit SATURN POS-PHY Level 2 or Level 3 system side interface.

No line rate clocks are required directly by these chips, as they synthesize the transmit clock and recover the receive clock using a 77.76 MHz reference clock. These framers output serial differential PECL line data (TXD+/-).

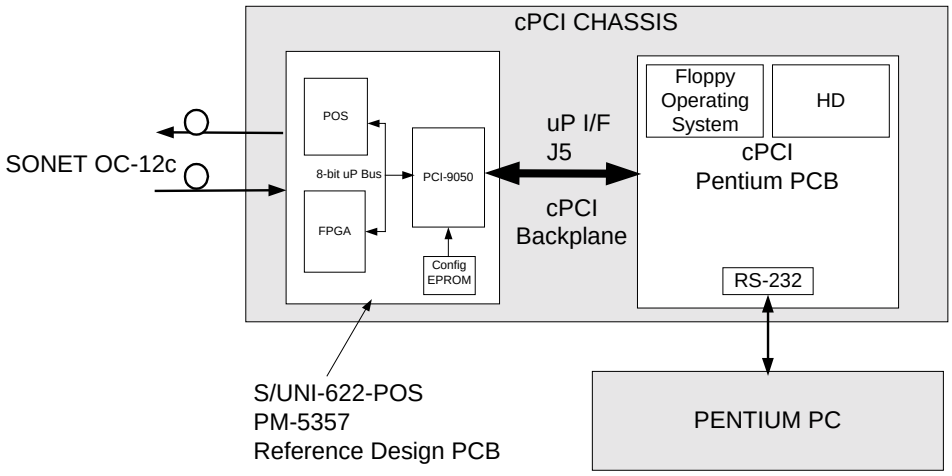
The S/UNI-622-POS is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. These devices also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

Both these devices are implemented in low power, +3.3 Volt, CMOS technology. They have TTL compatible digital inputs and TTL/CMOS compatible digital outputs. High speed inputs and outputs support 3.3V and 5.0V compatible pseudo-ECL (PECL). Detailed information about the PM5357 S/UNI-622-POS is available in the data sheet PMC-980911 and the PM5356 in data sheet PMC-980589.

6.3 Microprocessor Interface

The S/UNI-622-POS chip and rest of the reference board is controlled through the cPCI interface connector J1. All read and writes to the S/UNI-622-POS chip and the FPGA are executed through this cPCI bus.

Figure 12: Microprocessor Interface



At the physical level, the POS chip address and data bus is connected to the PLX chip (a PCI-9050 bus interface chip). The Address, A[10:2] and data bus, D[7:0], are multiplexed. The data bus is 8-bits wide (single byte) and the PLX chip must be programmed for this mode via it's external configuration EMPROM.

The local cPCI PCB µP should be running an operating system that allows the user to be able to access the PM5356/PM5357 registers.

6.4 External Connectors

The S/UNI-622-POS reference design contains two main back-plane connectors, J1 for the CompactPCI™ bus and J5 for the external UTOPIA/POS-PHY Level 2 drop-side.

J3, an 8-pin header is used to download the FPGA during code debugging from the PC to the reference board via a DLC4 Parallel Xchecker cable.

6.5 UTOPIA and POS-PHY drop side interface

For ATM applications, the PM5356/PM5357 and S/UNI-622-POS/MAX supports UTOPIA Level 2, Level 3 (UL2 and UL3) synchronous drop side interfaces.

For packet data (POS) applications the S/UNI-622-POS supports POS-PHY Level 2 and Level 3 bus interface.

On this PCB only the ATM Forum UTOPIA Level 2 (UL2) is supported at 50 MHz and 16 bits wide. The UL2 is used on many other PMC-Sierra ATM framers such as the S/UNI-LITE, S/UNI-ULTRA and S/UNI-622.

The UTOPIA Level 3 runs at 100MHz at 8-bits wide but is not supported on this PCB. For more information on these interfaces please consult the data sheets.

7 IMPLEMENTATION DESCRIPTION

In this document, the S/UNI-622-POS schematics refer to the schematics titled "S/UNI-622-POS reference design".

The S/UNI-622-POS reference design schematics were captured using Cadence software, Concept Schematics Capture Tool.

7.1 ROOT DRAWING, Sheet 1

This sheet provides an overview of the major functional blocks of the S/UNI-622-POS reference design. The schematic was designed in a hierarchical format. The interconnections between the OPTICS_BLOCK, POS_BLOCK, POS BLOCK POWER SUPPLY FILTERS, SYS_INTERFACE, FPGA, FPGA EPROMs and PCI BUS Interface are labeled with a xxx\I.

7.2 ODL and 77.76 MHz reference, Sheet 2

This page includes the OC-12, 622mHz Optical Interface and the 77.7600 MHz line side clock reference interface to the POS chip.

7.2.1 622 Mbit/s Optical Interface

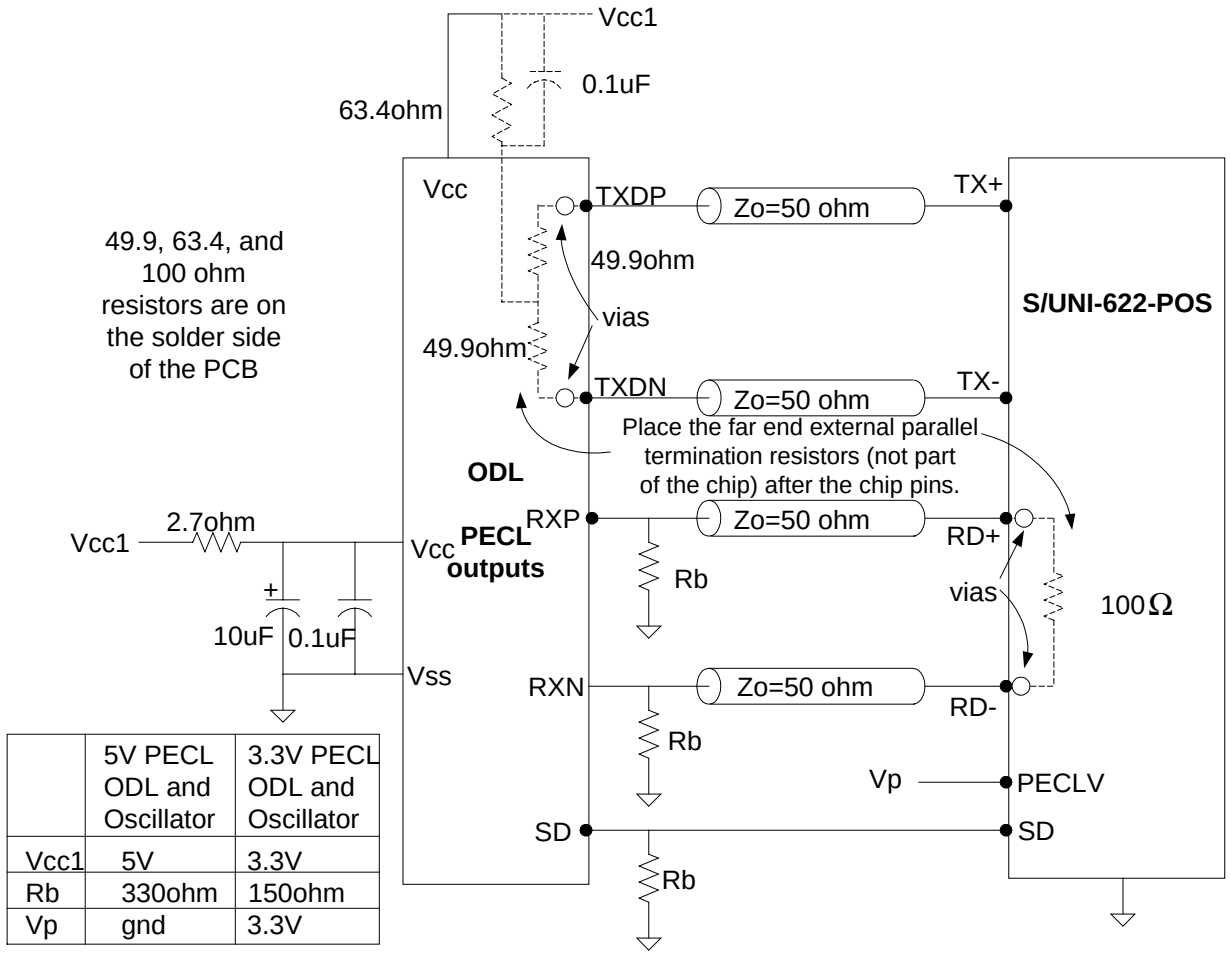
The ODL circuit consists of power supply filtering, ODL, TX and RX PECL terminations and SD connection.

The PECL signals run on 50 Ohm controlled impedance signal lines and are properly terminated at the ODL and at the S/UNI-622-POS device.

The S/UNI-622-POS device interfaces to one HP HFCT-5208 Single mode Fiber Transceivers. The HFCT-5208 transceivers are in a 1 x 9-pin package with a duplex SC receptacle. There are several manufacturers that market OC-12 ODL's including HP and Siemens in 5V and 3.3V options.

It's important that the oscillator is PECL and not the cheaper CMOS or TTL output type. Any jitter at the S/UNI-622-POS reference input may be seen at the TXD+/- data outputs and this translates into Optical output jitter. The 3.3V Connor Winfield EE14-541, 77.7600MHz Oscillator is specified at 10ps RMS output jitter and it's PECL outputs have rise/fall times of 550ps. The Connor Winfield 5V EH13-541 is specified at a much higher rise/fall times of 2.3ns max. Although no extensive tests were done with these two oscillators, no appreciable intrinsic jitter difference was noticed.

Figure 13: ODL Line Interface Terminations

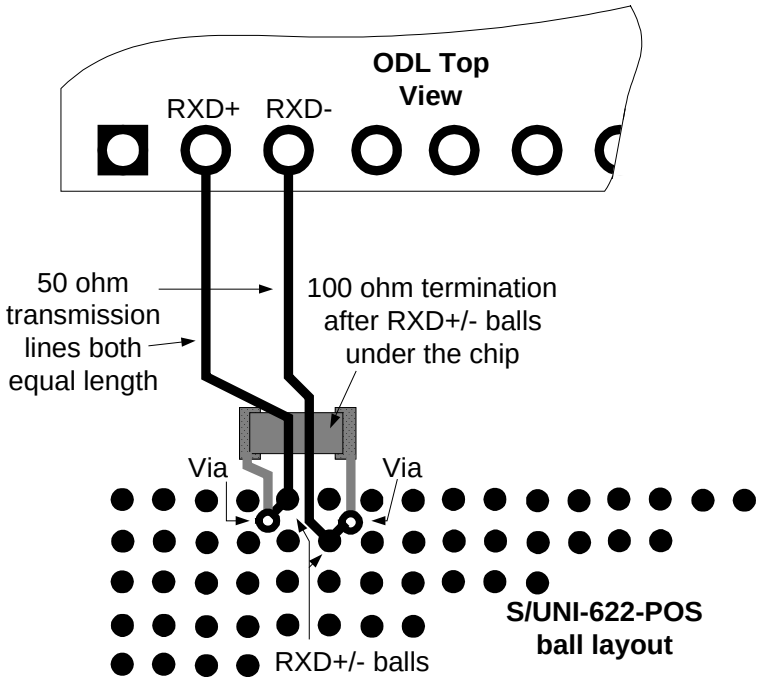


	5V PECL ODL and Oscillator	3.3V PECL ODL and Oscillator
Vcc1	5V	3.3V
Rb	330ohm	150ohm
Vp	gnd	3.3V

The S/UNI-622-POS reference design provides a single optical interface running at 622 Mbit/s OC-12c rate. The line interface consists of one single mode or multimode optical data link (ODL) and a termination scheme for the PECL signal into and out from the S/UNI-622-POS transmit, TXD+/- and receive, RXD+/- signal pairs. The suggested termination scheme for the PECL transmit and receive signals is shown in Figure 4 for 3.3V and 5V ODLs.

Notice in the schematic above, that the far end terminating resistors in dotted lines are placed after the chip (or ODL) pins so that transmission stubs are avoided and reflections are reduced. A suggested layout with the terminating 100 ohm resistor is shown below. Similarly the TXD+/- 49.9 ohm resistor termination circuit should be located on the solder side of the PCB and after the ODL pins.

Figure 14: RXD+/- PCB layout



In normal operation, the S/UNI-622-POS performs clock and data recovery on the incoming serial stream. As an option, internal clock and data recovery may be bypassed by setting the RBYP pin high and providing an externally recovered receive clock on the RRCLK+/- pins. In this mode RXD+/- is sampled on the rising edge of RRCLK+/-. This reference design is intended to use the PM5356/PM5357 internal clock and data recovery only and provides a footprint fitting the HFCT-5208 type ODL with a 1x9 pin duplex SC receptacle only.

Optionally, a footprint and function compatible, Siemens 3.3V ODL can be used, PN# V23826-H18-C363. Comparable jitter performance was observed with the 5V and the 3.3V ODL.

In loss of signal condition, indicated by the SD (signal degrade) pin or a lack of data transitions for 80 consecutive bit periods, the S/UNI-622-POS will squelch the receive data and the clock recovery unit will switch to the reference clock (77.76MHz) to keep the recovered clock in range. This technique guarantees that the S/UNI-622-POS will generate a LOS indication when the ODL loses incoming light.

The ODL power supplies are filtered as recommended by the manufacturer. The TX and RX supplies are filtered with a 1µH series coil, a 10µF bulk Tantalum and a ceramic 0.1µF ceramic cap. However, if the power supply is ‘noisy’, greater than 100mVp-p, additional filtering may be required.

7.2.2 77.7600 MHz Reference Clock Circuitry

The SONET OC-12 line reference clock can be categorized into two classes of applications, WAN and LAN. The scope of this document only covers the LAN case.

For WAN applications, a WAN compliant clock must be employed. This type of reference basically must be Phase Lock Looped (Line Timed) to the WAN network and must have no phase hits during a switch-over if loss of network reference is lost and have a long hold over. To achieve such a stringent requirement, an external digital PLL with a VCXO could be utilized to synchronize to the recovered 77.76MHz clock, RCLK or 8KHz frame pulse, RFPO.

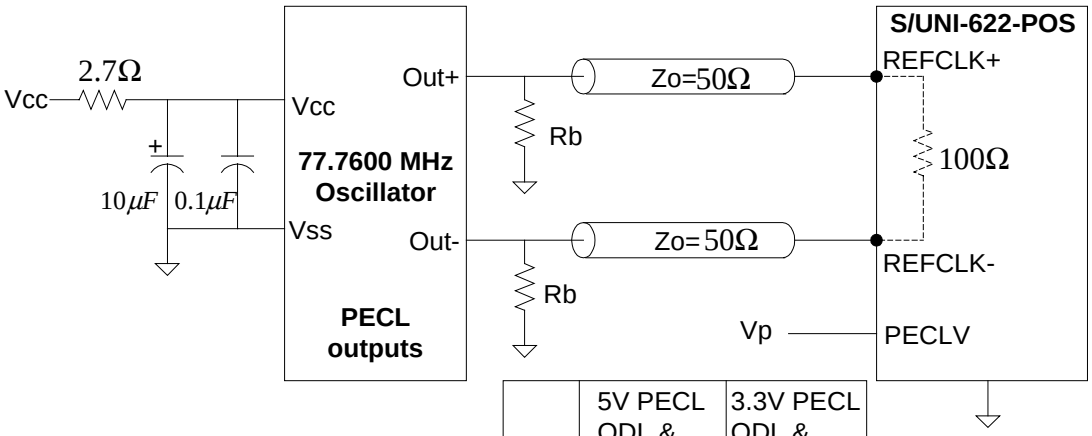
For LAN applications, a 77.76 MHz reference on this board consist of a PECL differential output, 77.76MHz oscillator. For LAN applications or edge switches, a 20ppm oscillator is adequate.

The PM5356 band PM5357 can accommodate either 5V or 3.3V PECL inputs. The PECLV pin selects which voltage range, 5V or 3.3V PECL, both the REFCLKP/N and RXD+/- pins will comply to. Both signals have to be either 3.3V or 5V PECL, depending on the PECLV pin. Both 3.3V and 5V PECL have a 0.8Vp-p swing but the 5V PECL is typically 3.2V to 4.1V. The 3.3V PECL is 1.6V to 2.4 V.

The PECLV pin on the framer programs both the ODL PECL I/F pins and the 77.76MHz Oscillator PECL inputs. Therefore, if the ODL is the same voltage as the Oscillator (both are either 3.3V or 5V type) then you can use the Oscillator circuit shown in Figure 15: 77.7600 MHz Reference Oscillator below. If the ODL and the oscillator are of different voltage, (ODL is 5V and Oscillator is 3.3V), then you must A.C. couple the oscillator with 0.01uF capacitors as shown in Figure 16: Mixing PECL 5V and 3.3V ODL and 77MHz Oscillators.

A single 100 ohm terminating resistor across the PECL signals is preferred over the two resistors per PECL trace method unless the signal is a.c. coupled as in Figure 16: Mixing PECL 5V and 3.3V ODL and 77MHz Oscillators. The single resistor method offers fewer components and because of component congestion near the 304 ball SBGA, it is easier to place one resistor than four. To avoid a transmission stub and reflections, place the terminating resistor(s) after the PCB trace contacts the chip pins (balls). In addition, keep the TXD+/- and RXD+/- traces to less than 4cm and ensure each pair is of equal length.

Figure 15: 77.7600 MHz Reference Oscillator



	5V PECL ODL & Oscillator	3.3V PECL ODL & Oscillator
Vcc	5V	3.3V
Rb	330ohm	150ohm
Vp	gnd	3.3V

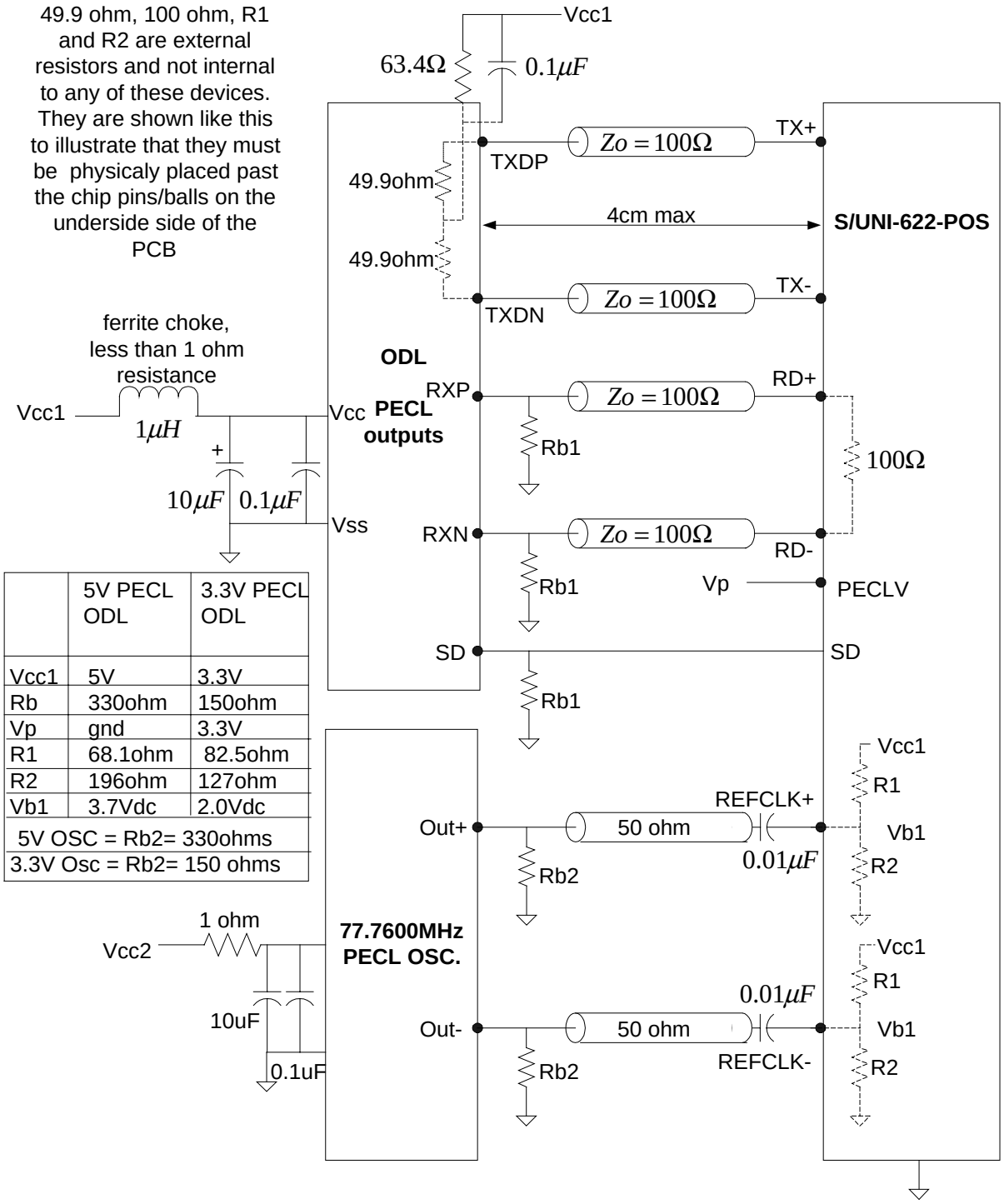
It is recommended that a low jitter oscillator be used to achieve the 0.10UIp-p (0.01UIrms) output Intrinsic Jitter. Low reference jitter is required because the clock synthesis unit (CSU) has to multiply the 77MHz reference by eight to generate the transmit 622Mhz. The jitter and noise is also multiplied.

Special attention must be given to ensure the Oscillator has a clean power supply since the output frequency will be modulated (jitter) by the DC voltage level or the AC noise. A RC type of voltage low pass filter is utilized to produce pole at 6Khz. A 2.7Ohm series resistor is used followed by 10µF Tantalum capacitor and a 0.1µF ceramic. The 2.7ohm resistor can't be too large because of DC IR loss. The 10µF Tantalum eliminates low frequency noise. Ceramic capacitor is used for high frequency de-coupling since ceramic capacitors have a much better high frequency response than Tantalum.

The two PECL devices, ODL and the 77.76 PECL Reference Oscillator, can be of different voltage type, 5V or 3.3V. However it is preferable to strap the PECLV pin for the ODL's requirements because the SD signal is a DC signal and level shifting will require extra active components. You can AC couple (use 0.01µF ceramic caps) and level shift the oscillator appropriately as shown below. Ensure that the 100 ohm resistor is placed after the chip pins instead of before the pins, otherwise a short stub may cause reflection problems.

It is not recommended to use a TTL oscillator and convert to PECL since this would introduce extraneous jitter.

Figure 16: Mixing PECL 5V and 3.3V ODL and 77MHz Oscillators



	5V PECL ODL	3.3V PECL ODL
Vcc1	5V	3.3V
Rb	330ohm	150ohm
Vp	gnd	3.3V
R1	68.1ohm	82.5ohm
R2	196ohm	127ohm
Vb1	3.7Vdc	2.0Vdc
5V OSC = Rb2= 330ohms		
3.3V Osc = Rb2= 150 ohms		

7.2.2.1 TXD+/- 15mA Current Drivers

The PM5357/PM5356 use CMOS open Drain 15mA current steered differential drivers as shown below. Since these TXD+/- drivers are not standard PECL BIPOLAR logic (Emitter Coupled Logic), with open emitter outputs, it is important to use exactly the circuit illustrated in “Figure 18: PM5357 TXD+/- Open Drain Current Drivers”, to interface to the ODL.

At any one time, only one of the framer TXD outputs is sinking 15mA of current while the other one is off in a high impedance state. Here is an analysis of the TXD+/- drivers:

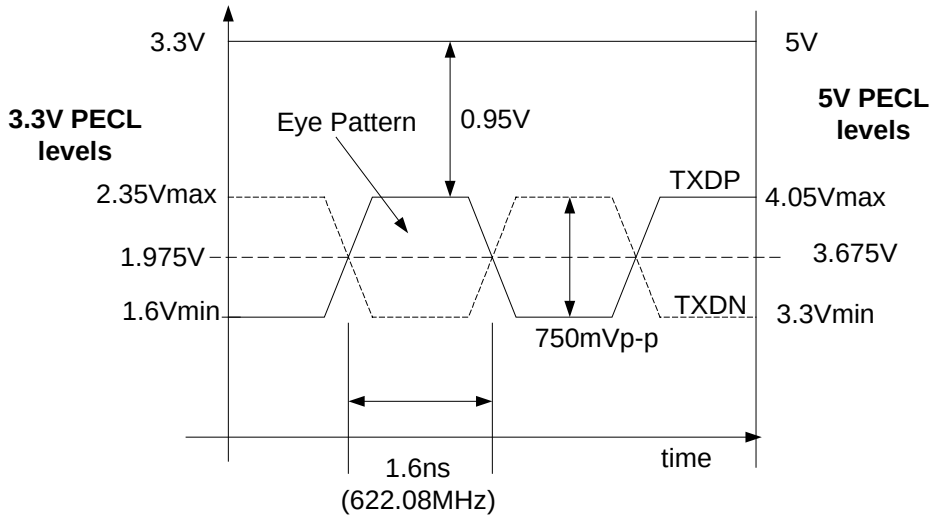
$$15mA \times 49.9\Omega = 750mVp-p$$

and

$$15mA \times 63.4\Omega = 0.951mVdc$$

Since 15mA always flows through the 63.4 Ω resistor, there will always be a DC drop of 0.951V across this resistor. An extra 0.1µF capacitor is added across the 63.4 Ω to make sure that this 2.35Vdc, an ‘ac ground’ voltage, has no ripple or noise. So the ac voltage at the ODL TXDP and TXDN inputs are as shown in figure below. The same calculations can be used for the 5V ODL with the same peak to peak voltage of 0.75 Vp-p but level shifted up and centered around 3.7V

Figure 17: PECL STS-12 Vp-p



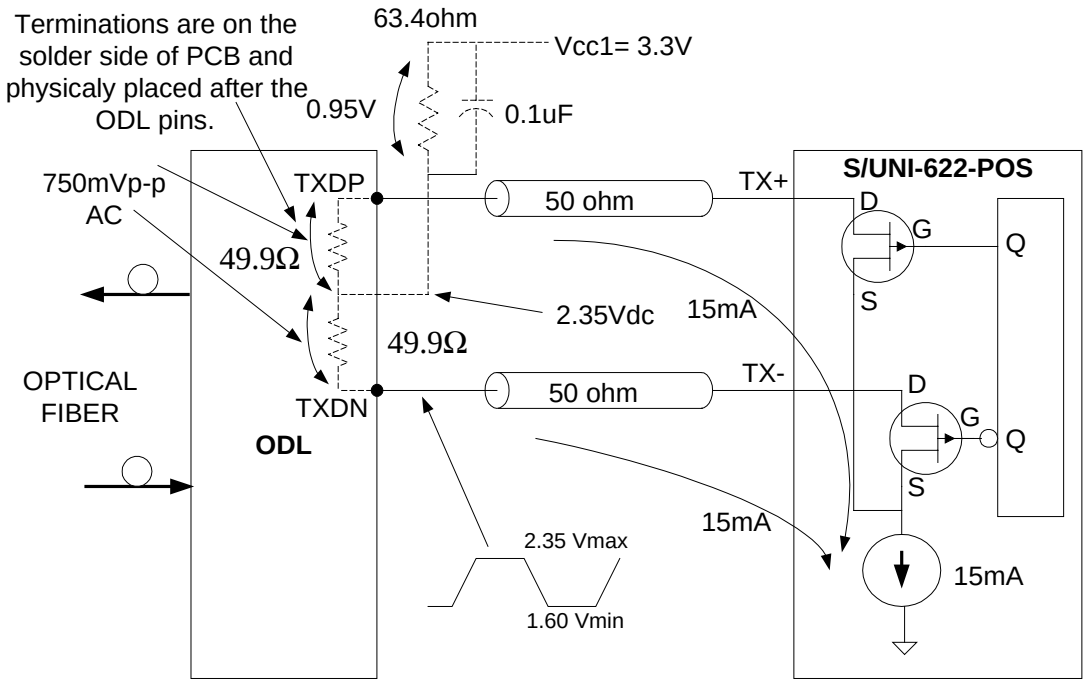
It’s critical that controlled PCB transmission line type traces be used for this high-speed 622.08 MHz signals with typical edge rates of 250ps. Even though the

symbol rate is actually only half that speed, at 311.04 MHz, the 250ns edges must be treated like transmission line to achieve the desired jitter performance.

Because the terminations are outside the ODL and not inside the ODL package, there is a short stub on the ODL PCB. Ideally the terminating resistors should be located on the ODL PCB at the inputs to the driver as shown below.

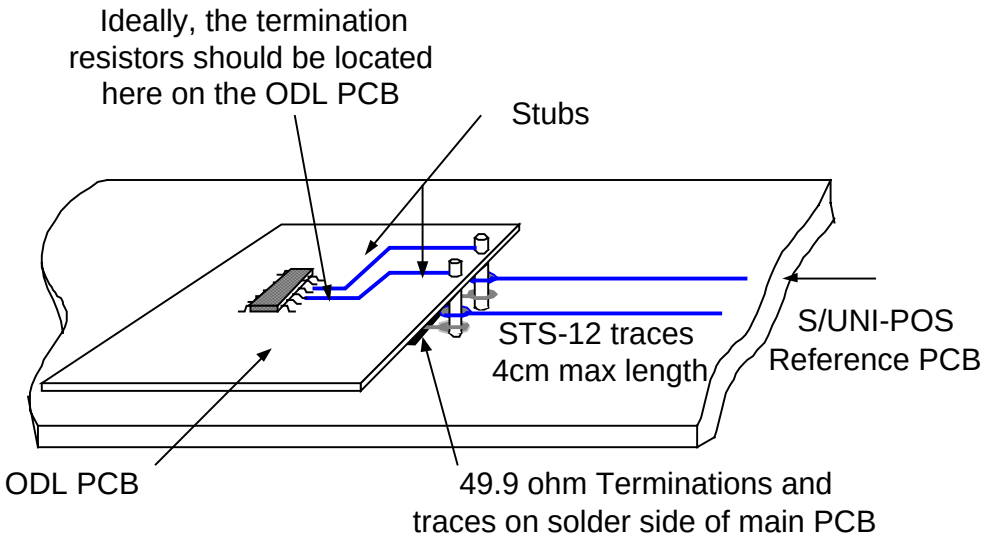
Because of this stub, the ODL should not be farther than 4cm away from the S/UNI-622-POS. For longer traces, a PECL buffer is recommended on the TXD+/- signals and an ODL with integrated termination like the Siemens V23826-H18-C313 AC/DC option.

Figure 18: PM5357 TXD+/- Open Drain Current Drivers



Ensure that the 49.9ohm resistors are placed after the ODL pins to avoid having a stub in the PCB trace as shown in Figure 19: Location of Terminations of TXD+/-. The terminating impedance, two resistors in this case, must be placed at the farthest end of a transmission line.

Figure 19: Location of Terminations of TXD+/-



7.3 POS_BLOCK, Sheet 3

The POS_BLOCK shows the PM5357 S/UNI-622-POS chip, all interface signals and power connections. If only ATM functionality is required, the PM5356 S/UNI-622-MAX may be soldered in the same footprint.

There are no Series resistors used to source terminate the UTOPIA/POS-PHY bus lines because the traces to the terminating device, the FPGA, are very short. However, if the traces were longer, one could use 51 Ω termination resistors combined with the output impedance of the UTOPIA/POS-PHY pads matches the impedance of the trace at 65 Ohms.

A 2K Ohm resistor is placed across the TDREF0 and TDREF1 pins. An LED displays line RX alarm status for the S/UNI-622-POS via a buffer 74HC04 chip. The RALRM output must be enabled in register 0x00E and 0x00F. RALRM out can be programmed to go high if there is alarms such as LAIS, PAIS, LRDI, PRDI, LOS< RDI, LOF, OOF, LOP, pointer AIS, LOPC, LCD, SFBER, and SDBER.

A 1K Ohm resistor is also placed in series with the power supply to limit the Vbias and Pbias current to prevent latch-up. A 0.1µF is added to eliminate high frequency noise. A 100 Ω series resistor is also required to the QAVD biasing pins to prevent latchup.

PECLV pin can be tied high or low with the resistor option, depending on whether 3.3V or 5V PECL interfaces are used for the 77.76 MHz clock reference and ODL.

The board has several test points such as RCLK and TCLK to facilitate debugging.

APS[4:0] pins are tied low through 4.7KΩ resistors. The APS pins provide a control bus between two S/UNI-622-POS devices to implement a 1+1 APS function. When using APS mode, line data is passed from one S/UNI-622-POS device to another using the FPIN, PIN[7:0], FPOUT, and POUT[7:0] pins. The APS function is not implemented in this reference design.

Care must be employed to ensure good PECL termination. In a far-end parallel termination scheme as employed on this case, usually the 100 Ω resistor should be placed after the chip pins otherwise the traces may be seen as stubs and reflections may occur. Reflections can cause poor jitter performance.

For more information on the PM5356 and PM5357 please refer to the data sheets.

7.3.1 Loop Filter Capacitor

A 47nF capacitor is placed across the loop filter pins, C1 and C0 to ensure a stable recovered clock. To maintain jitter transfer peaking of less than 0.1db over the life of the product, the capacitor must be a stable 47nF +/-5%. The best practical choice is a Class 2 X7R SMT ceramic type which has low aging characteristics, and a +5% to –10% capacitance change over -40°C to +85°C temperature.

7.3.2 Pullup and Pulldown Resistors

All unused CMOS inputs should be tied off high or low.

Unused PECL pins such as RRCLK+ and RRCLK- (or RRCLKP and RRCLKN respectively) should be tied to the opposite polarity. Failure to tie RRCLK+ and RRCLK- to complementary values will result in signal contention within the device which may cause problems with device operation.

When tying an input to ground, the pin may be connected directly to ground. When tying an input to 3.3V or 5V, a 4.7Kohm resistor should be used in order to prevent latch up during power up.

7.4 Power Supply Filter for the PM5357 Sheet 4

This page shows how to clean up the power supply to the S/UNI-622-POS. Because this IC has mixed analog and digital circuits, care must be used to eliminate noise from affecting the critical analog sections. The analog power supply must be filtered as shown below.

In addition, 0.1µF ceramic capacitors are used to filter the digital supply.

These chips will function in either a 3.3V only system or a mixed 3.3V and 5V TTL UTOPIA bus environment. Typical power planes should be used in a multi layer board with sufficient filtering with high quality high frequency ceramic 0.1µF caps on the digital rail and bulk filtered at the board connectors.

The S/UNI-622-POS performs clock and data recovery at a very high speed. Analog circuitry responsible for clock and data recovery must be free of noise to ensure reliable operation. Less sensitive analog power pins are grouped together and filtered with a single 0.1 µF capacitor. The more sensitive analog power pins of the S/UNI-622-POS are de-coupled using a low pass RC filter method. If there is a lot of power supply noise, >100mVp-p in the 3.3V rail, and a 5V supply is available, then a linear regulator approach is recommended.

7.4.1 Passive RC low pass power supply Filter

If there is no 5V rail available and the 3.3V supply is not very noisy (less than 100mVp-p at all frequencies), then this method is acceptable. Several capacitors may have to be paralleled to achieve the filtering across the desired frequency band. The 10µF capacitors should be X5R ceramic type and not Tantalum. Also use a 0.1µF X5R for high frequency noise reduction. The Issue 3 schematics use this passive filter method.

The X5R type capacitors have excellent low and high frequency response as seen in the graph below. The lower the impedance is, the better the capacitor for filtering. An excellent manufacturer of small size, non-polarized ceramic capacitors is Taiyo Yuden of 1930 North Thoreau, Drive, Suite 190, Schaumburg IL, 60173 USA, 1-80036-TAIYO. The X5R capacitors are similar to X7R except the high temperature spec is +85°C instead of 125°C for the X7R. These X5R ceramics are available up to 10µF at 6.3 Volts.

Figure 20: Tantalum & X5R Ceramic Impedance vs. Freq.

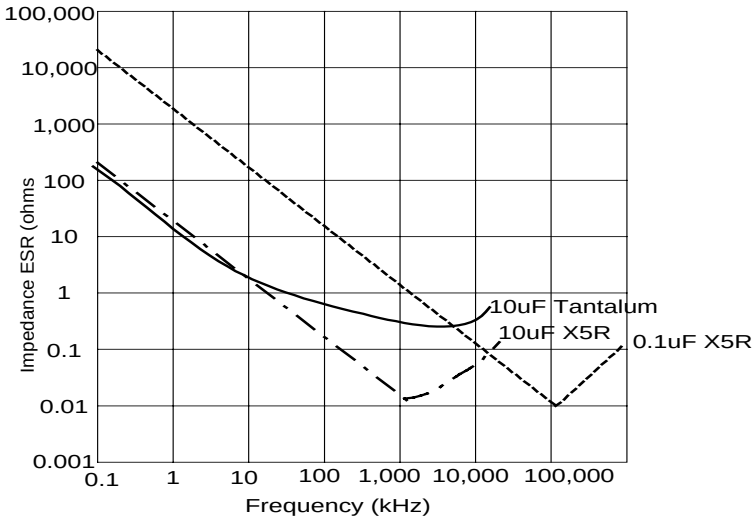
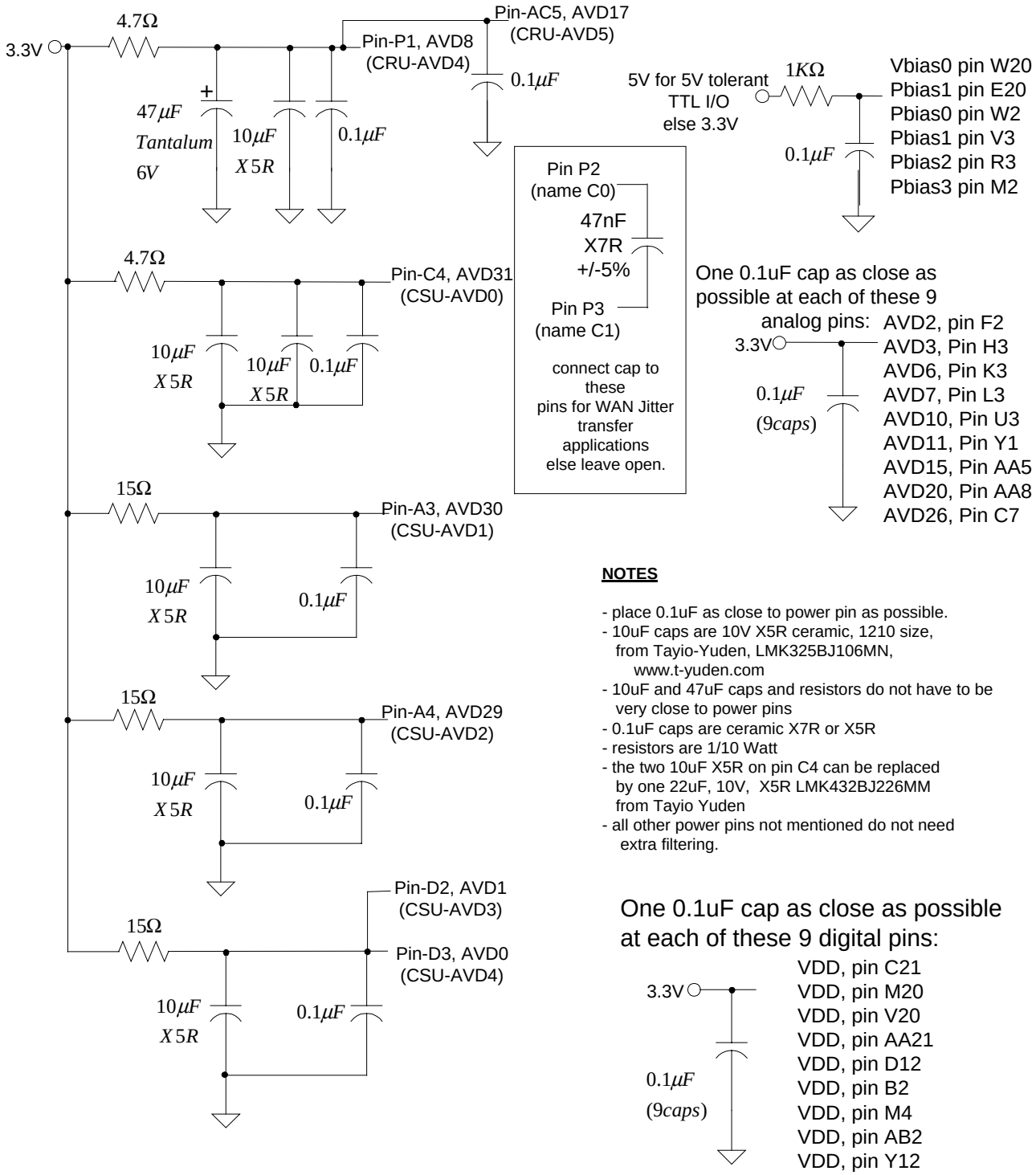


Figure 21: Passive RC Analog Power Supply Filtering



NOTES

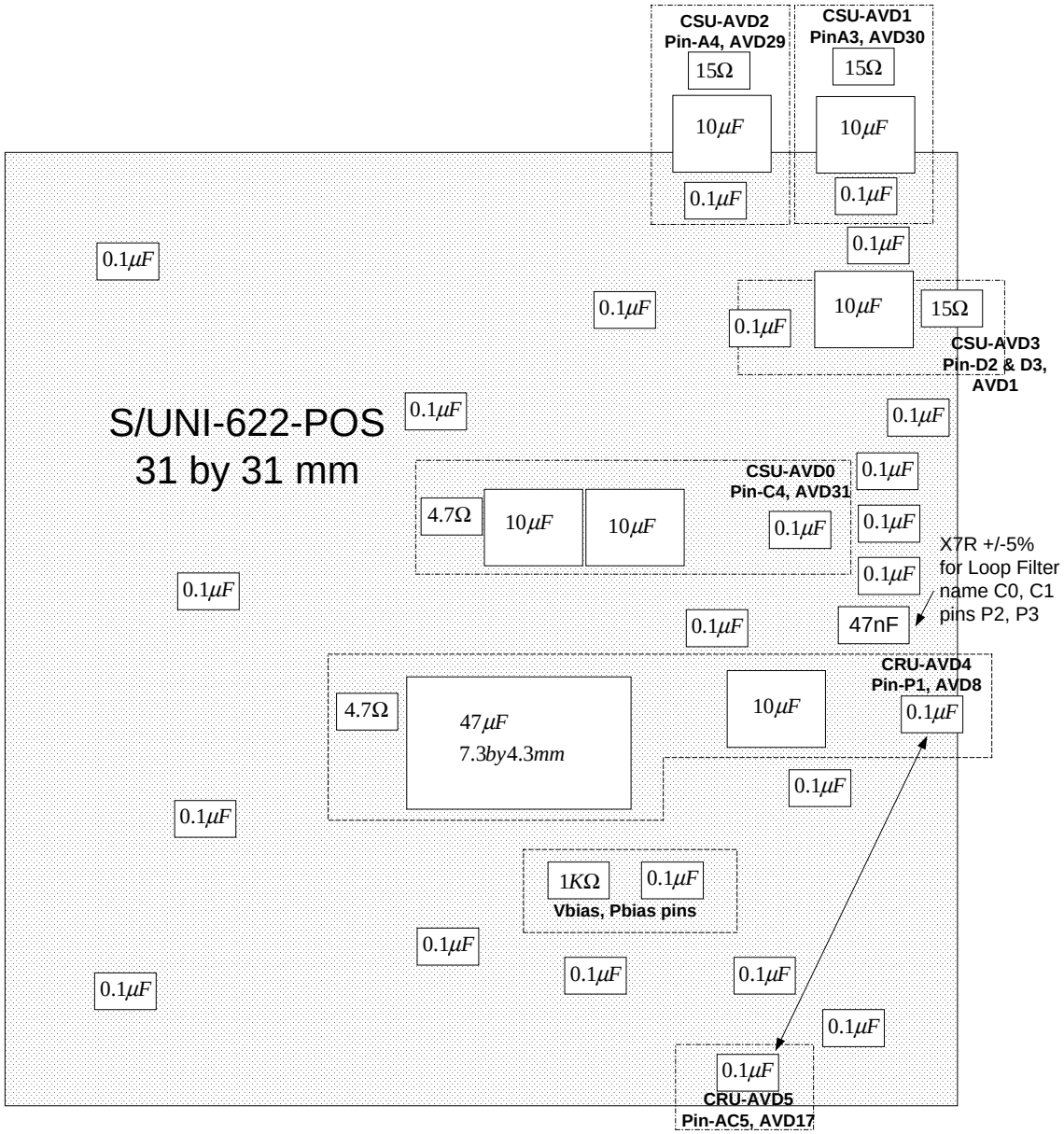
- place 0.1uF as close to power pin as possible.
- 10uF caps are 10V X5R ceramic, 1210 size, from Tayio-Yuden, LMK325BJ106MN, www.t-yuden.com
- 10uF and 47uF caps and resistors do not have to be very close to power pins
- 0.1uF caps are ceramic X7R or X5R
- resistors are 1/10 Watt
- the two 10uF X5R on pin C4 can be replaced by one 22uF, 10V, X5R LMK432BJ226MM from Tayio Yuden
- all other power pins not mentioned do not need extra filtering.

One 0.1uF cap as close as possible at each of these 9 digital pins:

VDD, pin C21
VDD, pin M20
VDD, pin V20
VDD, pin AA21
VDD, pin D12
VDD, pin B2
VDD, pin M4
VDD, pin AB2
VDD, pin Y12

Figure below shows relative size of components and is not meant to show placement location since it's difficult to place components on the solder side of a BGA.

Figure 22: RC Passive Filter Method Mechanical Diagram



Parts Count

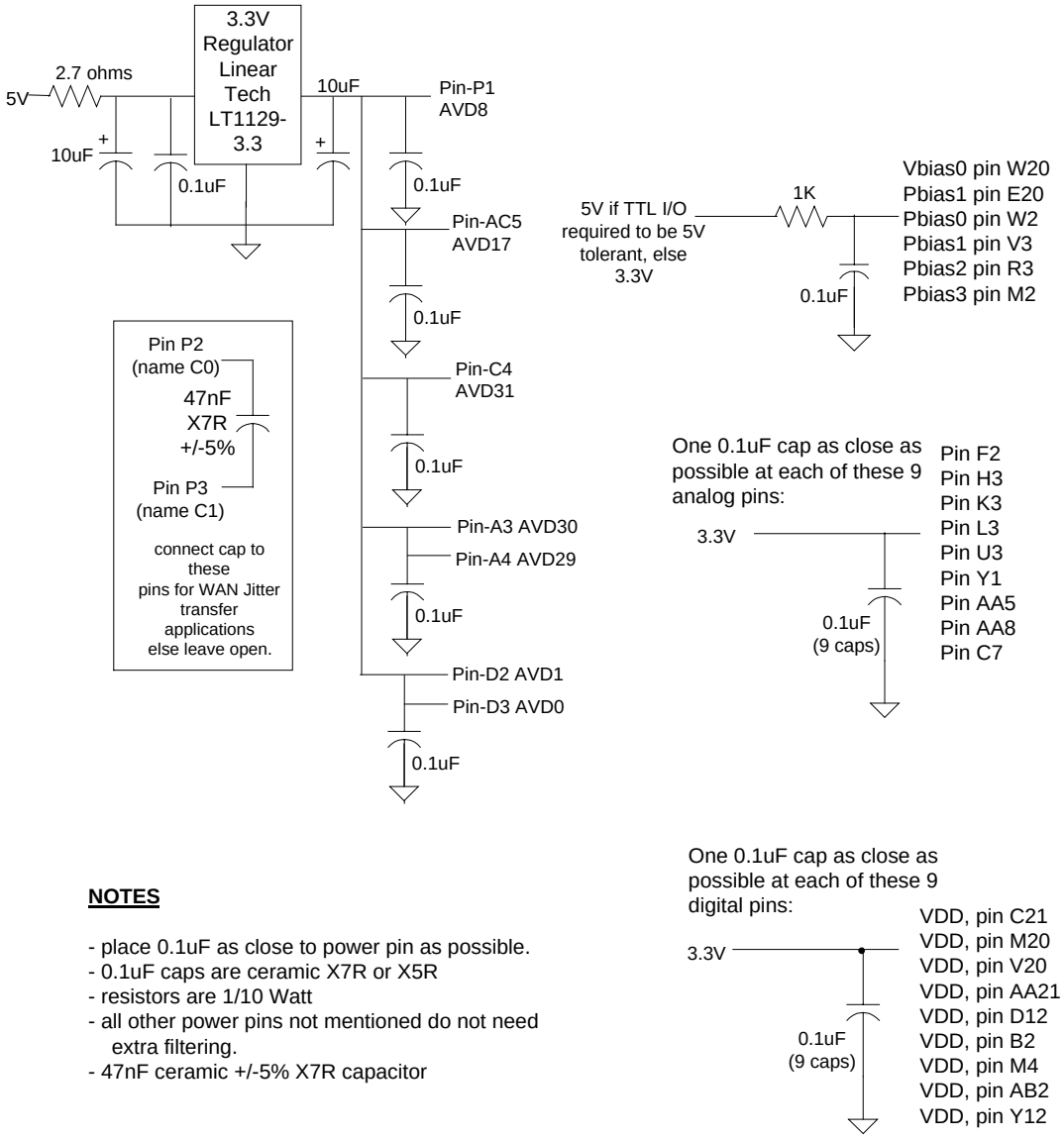
6 - 10uF 10V, X5R, 1210 (3.2 x 2.5 mm) size ceramic caps, LMK325BJ106MN
24 - 0.1uF, X7R, 0805 body (2 by 1.25mm)
1 - 47nF +/-5% ceramic X7R Class 2 capacitor
3 - 15 ohm R's, 1/10 W, 0805 body (2 by 1.25mm)
2 - 4.7 ohm Resistor, 1/10 W, 0805 body (2 by 1.25mm)
1 - 47uF Tantalum capacitor, 6.3V, SMT

Note: the resistors and the 10uF/ 47uF caps do not have to be close to the chip pins.

7.4.2 Linear Regulator Filter Method

If there is a 5V supply available, and the 3.3V supply has a lot of noise (>100mVp-p), then a better method to filter the analog supplies is with a “low drop-out voltage regulator” such as the LT1129-3.3 from Linear Technology. This regulator typically has about a 50db noise rejection up to about 500 kHz. Further noise attenuation is achieved with a front end the RC pre-filter (2.7 ohm + 10 µF) and a high frequency 0.1µF ceramic at the input to the regulator. A 10 µF Tantalum is required at the output for regulator stability.

Figure 23: Linear Regulator Power Supply Filter Schematic

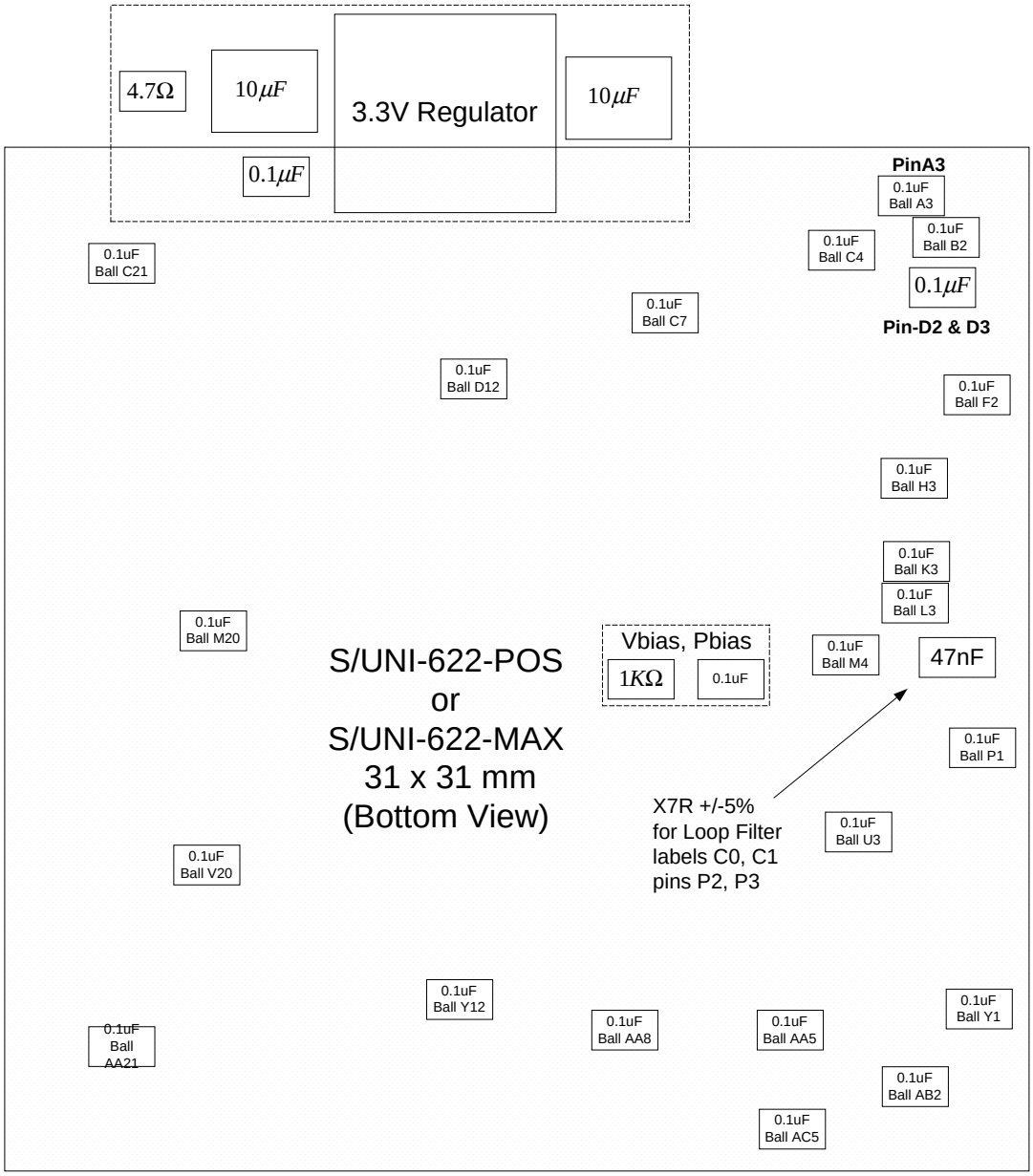


NOTES

- place 0.1uF as close to power pin as possible.
- 0.1uF caps are ceramic X7R or X5R
- resistors are 1/10 Watt
- all other power pins not mentioned do not need extra filtering.
- 47nF ceramic +/-5% X7R capacitor

Figure below shows relative size of components and is not meant to show placement location since it's difficult to place components on the solder side of a BGA.

Figure 24: Linear Regulator Filter Mechanical Layout



Parts Count

2 - 10uF 10V, Tantalum, 6V
26 - 0.1uF, X7R, 0805 body (2 by 1.25mm)
1 - 47nF +/-5% ceramic X7R capacitor
1 - 2.7 ohm Resistor, 1/10 W, 0805 body (2 by 1.25mm)
1 - 1Kohm resistor
1 - 3.3VLinear Regulator, SOT-23

7.5 FPGA, Sheet 5 and 6

This reference board has a large general purpose Xilinx XC4000 series FPGA (XC4036XLA-HQ240-9NS), filtering, configuration EEPROMs (XC1701), external download header J3, and thumb-wheel switch selector the EPROMS.

The FPGA, U13, is used to interface to the S/UNI-622-POS drop side to give this board some ATM and packet functionality. We chose the largest and fastest device we could find so that we were not restricted during our development. Information on this device is available from Xilinx.

At the time of this document, only the ATM drop side loopback was implemented and debugged. The ATM loopback code for the FPGA is enclosed in this document. ATM transparent, POS generation and POS transparent may be available in the future.

Several pins were brought out into headers (TP's) just in case we wanted to use this device for a different function than originally envisioned. Although they are tied off to ground, provision was made so that the ground trace can be easily cut.

The FPGA has eight LEDs connected to the general purpose I/O pins so that code could be written to selectively light these depending on the FPGA performance at power up and real time status. At power up, all the LEDs are on and when the FPGA is downloaded correctly from the EPPROMS, only the first LED is left on.

A header, J2 is used to select how the FPGA is to be configured at power up. With all the jumpers installed, the FPGA is programmed via the J3 (on page 6), serial cable adapter from a PC development setup. This is only used at time of code debugging. With all the J6 jumpers removed, the FPGA is configured at power up from one of four serial EEPROMs located on page 6 of the schematics.

The serial EEPROMs, U9, U12, U17 and U17 can be used to configure the FPGA for ATM loopback, ATM transparent to the J5 backplane, Packet generation/receiving, and packet transparent. Depending on the thumb wheel selector switch, U1, one of four different functions can be jammed into the FPGA at power up. The XC1701L EEPROM devices contain 832,528 bits. 20 pin PLCC sockets are used to facilitate ease of changing these programmable devices.

7.6 cPCI BUS Interface Sheet 7

This page contains the CompactPCI^{TM} bus backplane interface circuitry. It consists of the cPCI connector J1, the PLX bridge chip PCI-9050-1, serial EEPROM, NM93CS46 and power supply.

7.6.1 cPCI Backplane Connector J1

The J1 cPCI connector details can be found in the CompactPCI™ specification, PICMG 2.0 R2.1. All register accesses to the S/UNI-622-POS and FPGA are performed through connector. J1 can optionally supply 3.3V and 5V power to the board. Not all cPCI pins are used in this design. Please refer to the enclosed schematic for a detailed pin description.

7.6.2 PLX cPCI Bridge chip, PCI9050

The PCI 9050 provides a compact high performance PCI bus target (slave) interface for adapter boards. For more information on this device, please refer to the manufacturer's specification found on the PLX Technology web site. This device is programmed, via the external serial EEPROM, U14 at power up, for a multiplexed, 8 bit local data bus. The PLX chip allows the board to map several devices such as the S/UNI-622-POS and the FPGA to the cPCI bus.

The signals from the J1 connector to the PLX chip are tightly controlled and must adhere to the cPCI physical specification for proper operation. Ten ohm series terminating resistors are used to minimize reflection in all the signals.

Any unused inputs such as the unused LAD (address/data) pins are pulled up with 4.7K resistors.

Also, all tri-state outputs, such as RDB, are pulled up via a 4.7K resistor to prevent the bus from chattering during power up.

We added a couple of test points (RST_POS_FPGA, R_A) isolated by 10 ohm resistors to allow us to reset each chip manually by grounding a node. This allowed us to reset each chip without resetting the whole system which takes a few minutes re-boot from disk.

The address/data bus is multiplexed and the lowest order address is A2. The PLX does 32 bit, 4 byte accesses to/from the framer/FPGA and the cPCI system Software selects the bottom byte only. Notice that the top three data bytes on the PLX are not connected to the bus.

7.6.3 Serial EEPROM

The PLX chip, PCI9050, requires a configuration EEPROM during power up to configure itself. A serial device, U14, NM93CS46 contains the following code to configure the PLX for our system.

Table 1: PLX EPROM Configuration Code

EPROM Offset	Register Offset	EEPROM Value	Register Description
0	PCI 02	9050	Device ID
2	PCI 00	10B5	Vendor ID
4	PCI 0A	0680	Class code
6	PCI 08	0000	Class code (revision is not loadable)
8	PCI 2E	5357	Subsystem ID
A	PCI 2C	11F8	Subsystem Vendor ID
C	PCI 3E	FFFF	(Maximum Latency and Minimum Grant are not loadable.)
E	PCI 3C	01FF	Interrupt Pin (Interrupt Line Routing is not loadable.)
10	LOCAL 02	0FFF	MSW of Range for PCI to Local Address Space 0 (1 MB)
12	LOCAL 00	FF00	LSW of Range for PCI to Local Address Space 0 (1 MB)
14	LOCAL 06	0FFF	MSW of Range for PCI to Local Address Space 1
16	LOCAL 04	F800	LSW of Range for PCI to Local Address Space 1
18	LOCAL 0A	0000	MSW of Range for PCI to Local Address Space 2
1A	LOCAL 08	0000	LSW of Range for PCI to Local Address Space 2
1C	LOCAL 0E	0000	MSW of Range for PCI to Local Address Space 3
1E	LOCAL 0C	0000	LSW of Range for PCI to Local Address Space 3
20	LOCAL 12	0FFF	MSW of Range for PCI to Local Expansion ROM (62 KB)
22	LOCAL 10	0000	LSW of Range for PCI to Local Expansion ROM (62 KB)
24	LOCAL 16	0000	MSW of Local Base Address (Remap) for PCI to Local Address Space 0
26	LOCAL 14	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 0
28	LOCAL 1A	0000	MSW of Local Base Address (Remap) for PCI to Local Address Space 1
2A	LOCAL 18	1001	LSW of Local Base Address (Remap) for PCI to Local Address Space 1
2C	LOCAL 1E	0000	MSW of Local Base Address (Remap) for PCI to Local Address Space 2
2E	LOCAL 1C	0000	LSW of Local Base Address (Remap) for PCI to Local Address Space 2
30	LOCAL 22	0000	MSW of Local Base Address (Remap) for PCI to Local Address Space 3
32	LOCAL 20	0000	LSW of Local Base Address (Remap) for PCI to Local Address Space 3
34	LOCAL 26	0000	MSW of Local Base Address (Remap) for PCI to Local Expansion ROM
36	LOCAL 24	0000	LSW of Local Base Address (Remap) for PCI to Local Expansion ROM
38	LOCAL 2A	5401	MSW of Bus Region Descriptors for Local Address Space 0
3A	LOCAL 28	40C0	LSW of Bus Region Descriptors for Local Address Space 0
3C	LOCAL 2E	0080	MSW of Bus Region Descriptors for Local Address Space 1
3E	LOCAL 2C	0000	LSW of Bus Region Descriptors for Local Address Space 1
40	LOCAL 32	0080	MSW of Bus Region Descriptors for Local Address Space 2
42	LOCAL 30	0000	LSW of Bus Region Descriptors for Local Address Space 2
44	LOCAL 36	0080	MSW of Bus Region Descriptors for Local Address Space 3
46	LOCAL 34	0000	LSW of Bus Region Descriptors for Local Address Space 3
48	LOCAL 3A	0000	MSW of Bus Region Descriptors for Expansion ROM Space
4A	LOCAL 38	0000	LSW of Bus Region Descriptors for Expansion ROM Space
4C	LOCAL 3E	0000	MSW of Chip Select (CS) 0 Base and Range Register
4E	LOCAL 3C	1101	LSW of Chip Select (CS) 0 Base and Range Register
50	LOCAL 42	0000	MSW of Chip Select (CS) 1 Base and Range Register
52	LOCAL 40	1801	LSW of Chip Select (CS) 1 Base and Range Register
54	LOCAL 46	0000	MSW of Chip Select (CS) 2 Base and Range Register
56	LOCAL 44	0000	LSW of Chip Select (CS) 2 Base and Range Register
58	LOCAL 4A	0000	MSW of Chip Select (CS) 3 Base and Range Register
5A	LOCAL 48	0000	LSW of Chip Select (CS) 3 Base and Range Register
5C	LOCAL 4E	0000	MSW of Interrupt Control/Status Register
5E	LOCAL 4C	0000	LSW of Interrupt Control/Status Register
60	LOCAL 52	0002	MSW of EEPROM Control and Miscellaneous Control Register
62	LOCAL 50	4492	LSW of EEPROM Control and Miscellaneous Control Register

7.6.4 Power Supply

The board is powered via the J1 connector from the system cPCI backplane. The 5V and the 3.3V rails are bulk filtered as they enter the board with 47µF tantalum capacitors. These power rails are also fused with 2 Amp fuses to prevent the board from severe damage in case of a circuit failure. Because a fuse has a finite “on resistance/impedance”, a second 47µF is located on the other side of this fuse. An LED is provided for each supply to alert the user if the power is on.

7.7 SYS_INTERFACE, Sheet 8

The SYS_INTERFACE block contains the J5 UTOPIA board connector and the UTOPIA bus clock oscillator.

7.7.1 50mHz UTOPIA Oscillator

A 50 MHz oscillator, 100ppm, is used for the POS-PHY Level 2 or Utopia Level interface rate. If there was a UTPOIA Level 3 provision, a 100 MHz crystal oscillator could have been used. The oscillator does not need any special power supply filter since jitter is not an issue like it is for the 77.7600MHz line side clock reference. However, because of the tight bus timing requirements, a buffer is used to provide low skewed clocks to the PM5357, the FPGA, and to the external J5 connector.

7.7.2 J5 UTOPIA Connector

The J5 connector uses a PMC-Sierra Inc. proprietary pin out for the UTOPIA Level 2 bus as shown in Table 2: J5 UTOPIA Level 2 Connector.

The S/UNI-622-POS UTOPIA Level 2 interface is connected to the drop side J5 connector through the FPGA. The pin names shown below have the prefix “SYS_” added on the signal names of the schematic.

Table 2: J5 UTOPIA Level 2 Connector

Pin Name	Type	Pin No.	Function
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Output	D2 B2 E3 D3 B3 A3 E4 D4 B4 A4 E5 D5 B5 A5 E6 D6	UTOPIA: Receive Cell Data Bus For Utopia Level 2 this bus carries the ATM cell octets that are read from the receive FIFO. For Utopia Level 3 only RDAT[7:0] are valid. POS-PHY: Receive Packet Data Bus For POS-PHY Level 2 this bus carries Packets that are read from the selected receive FIFO. For POS-PHY Level 3, only RDAT[7:0] are valid.
RPRTY	Output	B6	Receive bus parity. The receive parity signal indicates the parity of the RDAT bus.
RENB	Input	A6	Receive Write Enable. The RENB signal is an active low input which is used to initiate reads from the receive FIFO.
RCA RPA	Output	B11 B11	UTOPIA: Receive Direct Cell Available This signal indicates an available cell. POS-PHY: Direct Receive Packet Available. For POS-PHY Level 2, this signal indicates when data is available in the receive FIFO. For POS-PHY Level 3 this signal is not used as RVAL signals valid data on the bus.
RSOC RSOP	Output	D7 D7	UTOPIA: Receive Start of Cell This signal marks the start of cell on the RDAT bus. POS-PHY: Receive Start of Packet This signal marks the start of packet on the RDAT bus.
RERR	Output	E8	POS-PHY: Receive Error This signal indicates that the current packet has been aborted. This signal is ignored in Utopia ATM modes.

Pin Name	Type	Pin No.	Function
REOP	Output	B7	POS-PHY: Receive End of Packet This signal marks the end of packet on the RDAT bus. This signal is ignored in Utopia ATM modes.
RMOD	Output	B7	RX modulo: Indicates number of bytes in the last RDAT bus transaction of a packet.
RVAL	Output	D8	In POS mode, RAVL indicates signals RDAT, RSOP, REOP, RMOD, RPRTY and RERR are valid.
RFCLK3	Output	A1	50 MHz UTOPIA bus clock buffered by the FPGA and same time delay as the actual UTOPA signals.
RFCLK1	Output	C1	50 MHz UTOPIA bus clock straight from the oscillator buffer.
TENB	Input	E17	Utopia and POS-PHY: Transmit Write Enable. The TENB signal is an active low input which is used to initiate writes to the transmit FIFO
TCA	Output	D12	Utopia: Transmit cell available signal This signal is used to indicate available cell FIFO space by the PHY port.
TPA		D12	POS-PHY: Direct Transmit Packet Available. This signal transitions to high when a programmable minimum number of free space is available in the transmit FIFO.
TSOC	Input	B16	Utopia: Transmit Start of Cell The transmit start of cell signal marks the start of cell on the TDAT bus.
TSOP		B16	POS-PHY: Transmit Start of Packet For POS-PHY Level 2 this signal indicates the first word of a packet. In POS-PHY Level 3 this signal indicates the first byte in a packet.
TERR	Input	A15	POS-PHY: Transmit Error This signal indicates the current packet must be aborted. This signal is ignored in Utopia ATM mode
TEOP	Input	D16	POS-PHY: Transmit End of Packet This signal marks the end of a packet on the TDAT bus. This signal is ignored in Utopia ATM modes.

Pin Name	Type	Pin No.	Function
TMOD	Input	E16	POS-PHY: Transmit Word Modulo For POS-PHY Level 2, this signal indicates the size of the current word. For POS-PHY Level 3 this signal is ignored. This signal is ignored in Utopia ATM modes.
TPRTY	INPUT	D17	Transmit bus parity. The transmit parity signal indicates the parity of the TDAT bus.
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	INPUT	B21 D21 A20 B20 D20 E20 A19 B19 D19 E19 A18 B18 D18 E18 A17 B17	Utopia: Transmit Cell Data Bus This bus carries the ATM cell octets that are written to the selected transmit FIFO. POS-PHY: Transmit Packet Data Bus This data bus carries the POS packet octets that are written to the selected transmit FIFO. For POS-PHY Level 3, only TDAT[0:7] are valid.
TFCLK2	Output	A1	50 MHz UTOPIA bus clock buffered by the FPGA and same time delay as the actual UTOPIA signals.
TFCLK1	Output	C1	50 MHz UTOPIA bus clock straight from the oscillator buffer.
NC	NC	D9…	Many No Connect Pins. See schematic
3.3VDC	Power	C3, C4	3.3V power supply
GND	Power	B1, D1	Ground

8 SOFTWARE CONSIDERATIONS

8.1 Path Signal Label 'C2'

Upon reset the S/UNI-622-POS/MAX register 0x48, Path Signal Label, SONET/SDH C2 byte, defaults to 0x01, which signifies an equipped unspecific payload. This device will stuff a 0x01 into the C2 byte in the SONE path overhead until it is changed. This register should be reprogrammed with the value 0x13 when in ATM mode or value 0xCF when in Packet over SONET (POS) mode so that the Path C2 byte will contain the correct payload type. The receiver should have a matching C2 byte so that a signal label mismatch (PSLM) alarm is not declared. If there is a path signal label mismatch the PSLMPAIS bit in register 0x0D will enable path AIS insertion. In this case all ones will be inserted into the receive SONET/SDH payload, the PM5356/PM5357 will not be able to acquire cell delineation and a PATH alarm will be declared.

Upon power up, register 0x54 should be programmed with the expected path signal label of 0x13 for ATM and 0xCF for Packet over SONET (POS).

8.2 SONET or SDH Configuring

The SONET and SDH fiber standards for optical networking are very similar, with only minor differences in overhead processing. The main difference between the SONET and SDH standards lies in the handling of some of the overhead bytes. Other details, like framing, and data payload mappings are equivalent in SONET and SDH. By default, PMC's S/UNI-POS powers up in SONET mode. However, it can be configured to operate in SDH mode.

The bit error rate (BER) monitoring requirements are also slightly different between Bellcore GR-253-CORE (SONET) and ITU.707 (SDH) An application note, PMC-950820, explains in detail the different parameters for the RASE block.

The table below shows the various register settings to configure the POS for either SONET or SDH mode

Table 3: SONET vs. SDH Configuration

Register/bits	SONET	SDH
SDH_J0/Z0 (0x01)[1]	0	X
ENSS (0x3D)[2]	0	1
LEN16(Path, 0x28)[3]	0	1
LEN16(Section, 0x50)[3]	0	1
S[1:0] (0x46)[4]	00	10

Notes:

1) SONET requires Z0 bytes to be set to the number corresponding to the STS-1 column number. SDH considers those bits as reserved.

2) SDH specification requires the detection of SS bits to be “10”

3) SONET uses 64 bytes message/SDH uses 16 bytes message

4) SS is undefined for SONET but must be set to “10” for SDH

9 PCB CONSIDERATIONS

Because of the high speed 622MHz PECL differential drivers, and other fast edge signals such as the UTOPIA bus, this PCB requires careful layout. Typically the drivers for these have rise/fall times in excess of 1ns. High speed traces should be as short as possible, transmission lines are to be used where indicated and standard terminations must be incorporated to prevent signal reflections.

Standard FR-4 PCB material can be used for this application with as many layers as is required to derive the final board thickness, achieve enough layers for signal routing and attain the required trace impedance. Please refer to the first page of the artwork for more detail on the reference design PCB.

We chose the following stack up layers:

Table 4: Reference Design PCB Stack Up

Layer	Location
Top	Top Signal Layer , Component side
3.3V PLANE	Power
GND_PLANE	Ground
SIG1	Signal Layer
SIG2	Signal Layer
VCC_PLANE	5V Power Layer
GNDA_PLANE	Ground
BOTTOM	Bottom layer, Solder Side

Although only one ground plane is required, two are used to attain the desired board thickness and correct trace impedance. A ground layer or a power plane can be used to achieve the desired signal transmission line trace impedance assuming there is adequate coupling between them.

The PECL 622MHz and 50 MHz traces are 50 ohms and they are 8 mil wide. The rest of the board is laid out with 5 mil and these are 65 ohm impedance.

Traces that are long and have a signal that has relatively fast rise/fall times should be routed with a Stripline.

$$l = \frac{T_r}{D}$$

$l =$ length of rising edge, in Inches

T_r = rise time of edge (ps)

D = delay of material (ps/in)

Stripline delay for FR-4 PCB material is about 188 ps/in, PECL drivers typically exhibit 250ps rise/fall times, and UTOPIA drivers are about 1ns. Therefore:

$$l = \frac{T_r}{D} = \frac{250}{180} = 1.33in.$$ (3.4cm)

Traces with *length less than* $\frac{l}{6}$*,* are considered lumped and do not need terminations. PECL traces that are less than $\frac{1.33in}{6}$ = 0.22in/0.56cm, and CMOS level UTOPIA bus traces less than 0.89in/2.26cm, do not need to be terminated.

Please refer to the High Speed Digital Design Handbook for more detail regarding transmission lines and terminations.

9.1 PECL Interface Issues

All unused differential PECL inputs should be tied such that the positive input and negative input are complementary (have opposite logic values). For example if RRCLK+ is tied to 3.3V, therefore RRCLK- should be tied to ground. Or; RRCLK+ is tied to ground and RRCLK- should be tied to 3.3V.

The PECLV and PBIAS pins affect both the optical PECL interface as well as the REFCLK+/- interface. Therefore REFCLK+/- must have the same signal reference level as the optical PECL interface.

Because of the transmission stub created by the ODL internal PCB trace and through-hole solder mounting pins, traces between the optics and the S/UNI-622-POS should be limited to a maximum of **4 cm** long. No vias should be present on the point to point traces except where required for the terminating components. Any vias present along the traces will degrade jitter performance.

These differential traces should be of equal length and have as few bends as possible. To prevent transmission stubs, terminating components (resistors) should be placed after the IC pin(s) and usually on the solder side (bottom) of the PCB.

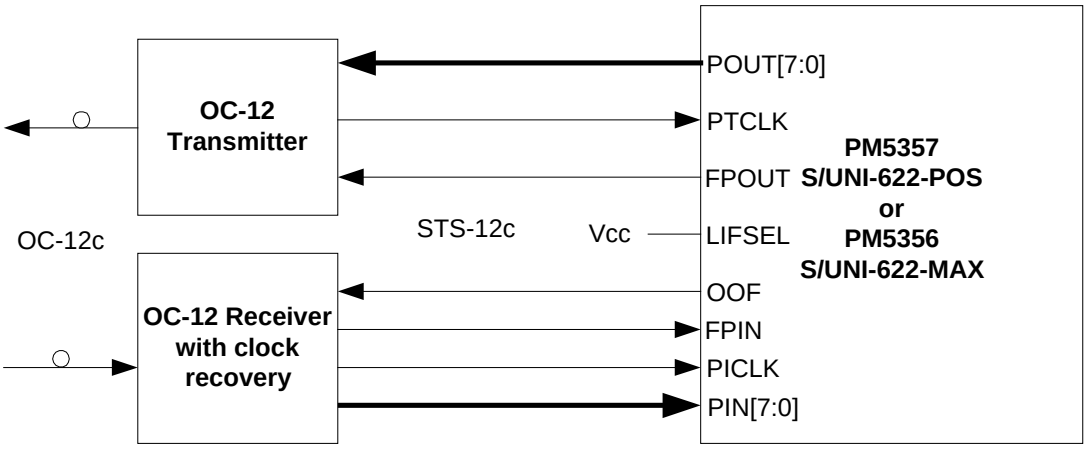
9.2 Clock and Data Recovery

Although the S/UNI-622-POS(MAX) has an optional external clock/data recovery interface, it is best to use the internal clock and data recovery. This is the cheapest method, has the lowest parts count, takes up the least amount of board space and exceeds jitter requirements of Bellcore GR-253/CORE.

The external clock/data recovery can be utilized by using the framer's parallel interface through the chip's PIN[7:0], RRCLK+/-, FP, OOF and POUT[7:0] pins.

As illustrated below, devices like the HP RGR2622 Clock/Data SONET Receiver Module, which have their own clock recovery circuit, can be used in conjunction with an Optical Transmitter to interface the S/UNI-622-POS to the SONET fiber.

Figure 25: External Clock and Data Recovery



10 APS (AUTOMATIC PROTECTION SWITCHING)

The PM5357 S/UNI-622 POS, and the PM5356 S/UNI-622-MAX, have added circuitry and special function pins to allow two of these devices to be optionally configured to operate in a “1+1” APS mode. For more information on APS, please refer to section 5.3 of GR-253-CORE. APS is a feature that allows redundant circuits to be switched in if a fiber is broken or a circuit board has failed.

10.1 APS Hardware Configuration:

For APS, the S/UNI-622-POS framer registers must be set up as follows:

Table 5: APS configuration of the Working framer

S/UNI-622-MAX/POS pin	Description of connection
LIFSEL	GND
PICL	GND
PIN[7:0]	GND
FPIN	GND
PTCLK	GND
POUT[7:0]	Connect to PIN[7:0] of the protection PM5356/PM5357
APS[4:0]	Connect to the APS[4:0] of the protection PM5356/PM5357
FPOUT	Connect to FPIN of protection PM5356/PM5357
TCLK	Connect to PICLK of protection PM5356/PM5357

Both the working and the protection S/UNI-622-POS/MAX timing must be synchronous. They can’t be independently looptimed.

- The FIFO on the Protection S/UNI needs to be reset during system reset and when the CSU is held in Reset.

- During normal operation, when the RX traffic is selected from the working channel the register must be set up as listed below:

Table 6: APS HW configuration of the Protection framer

S/UNI-622-MAX/POS pin	Description of connection
LIFSEL	GND
PICL	TCLK from the working PM5356/PM5357
PIN[7:0]	Connect to POUT[7:0] of the working PM5356/PM5357
FPIN	Connect to the FPOUT of the working PM5356/PM5357
PTCLK	GND
POUT[7:0]	Not Used
APS[4:0]	Connect to the APS[4:0] of the working PM5356/PM5357
FPOUT	Not used

10.2 APS Software Configuration

For “1+1” APS, S/UNI-622-POS/MAX framer must have register 0x06H set up as follows.

Table 7: Register set-up during normal operation

Register 0x06H BIT LABEL	WORKING PM5356/PM5357	PROTECTION PM5356/PM5357
APSFEBE	0	0
APSRDI	0	0
APSPD	0	1
APSPOE	0	1
APSEN	1	1

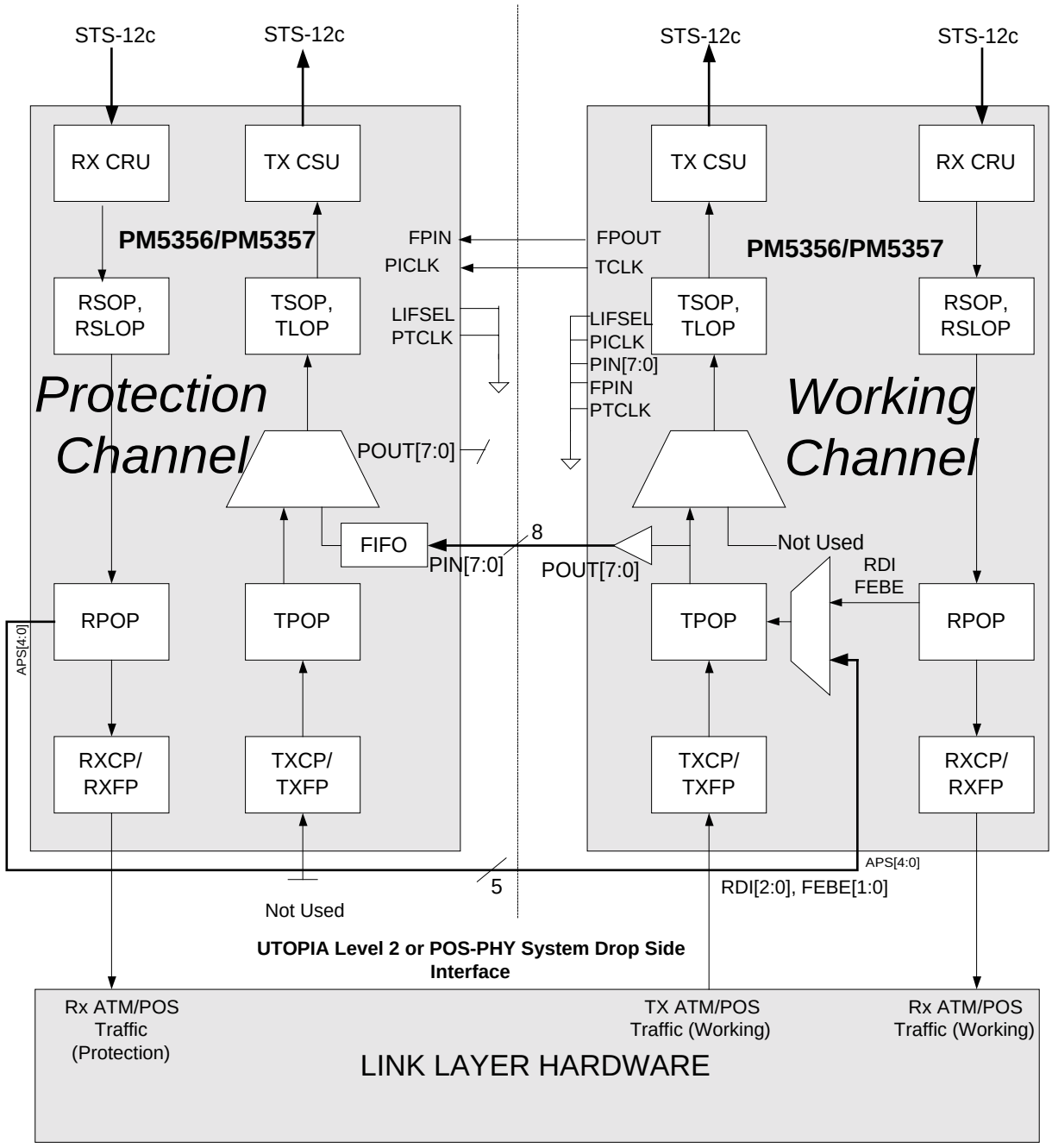
During protection operation, when the RX traffic is selected from the protection channel the register must be set up as follows:

Table 8: Register configuration in Protection Operation

Register 0x06H BIT LABEL	WORKING PM5356/PM5357	PROTECTION PM5356/PM5357
APSFEBE	0	0
APSRDI	0	0
APSPD	0	1
APSPOE	0	1
APSEN	1	1

Bellcore GTR-253-CORE requires that the APS protection occurs at the Path level as in the PM5356/PM5357 shown below. If only fiber protection is required, the PM5356/PM5357 protection/working devices can be located on the same system PCB or for added protection, on separate cards within a system chassis.

Figure 26: "1+1" APS using PM5356 built in APS function



11 POWER SUPPLY CONSIDERATIONS

11.1 Power Up/Down Considerations

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to blow these ESD protection devices or trigger latch up. For more information on the required power up sequence, refer to the S/UNI-622-POS data sheet. The following features on the S/UNI-622-POS reference design ensure power up and power down occur properly.

- A 1.0K Ohm resistor is placed in series between the 5V supply and the VBIAS and PBIAS pins. This resistor prevents excessive current from flowing from VDD through VBIAS and PBIAS to the 5V supply in case the 3V supply to VDD is applied before the 5V supply is applied to the bias pins.

- The QADV pins also needs a 100 ohm series resistor to limit inrush currents and prevent latch-up.

- VDD, QAVD, and regular AVD pins are supplied from the same 3.3V power plane. This keeps the voltage difference between the AVD pins, VDD and QAVD pins small thus preventing current flow from AVD pins to the VDD, and QAVD pins. Sensitive AVD pins are filtered using a 3.3V, 100mA voltage regulator powered from the 5V power plane. These sensitive AVD pins are current limited by the voltage regulator so that each pin cannot draw current higher than the 100 mA maximum latch up current.

11.2 Grounding

Only one ground plane is recommended with no power or ground cuts in these planes. This one ground plane is shared among digital and analog signals. One ground plane simplifies design and layout. As in this design, more than one ground plane layers can be used, but all ground connections (vias) are made to all layers to make it appear as one ground plane. A trace characteristic impedance can be realized by providing the current return path either through a ground or power plane.

It is very important to ensure proper analog supply decoupling as outlined below.

Since the Optical interfaces (ODL's) are optically isolated, there is no requirement for heavy duty high-voltage and/or high energy protection as in other metallic physical mediums such as T1/E1.

11.3 System Side Transmission Line Terminations

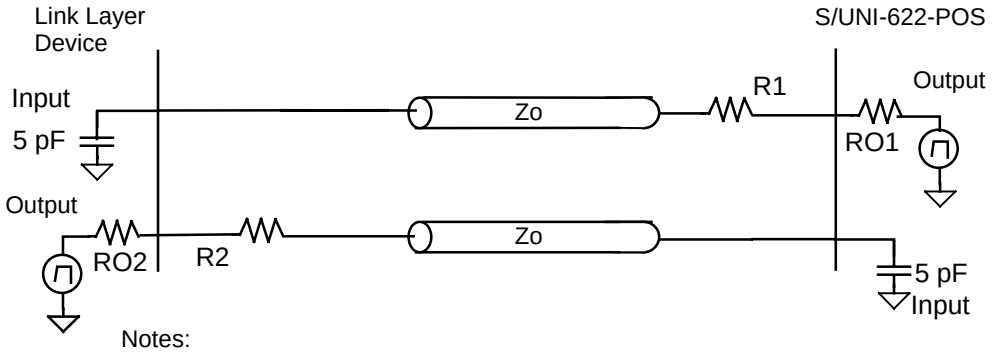
The S/UNI-622-POS is capable of system side interface speeds up to 100 MHz. Because of the high frequency content of the system side signals, trace termination may be required to ensure reliable data transmission across the interface.

All signals on the system side interface of the S/UNI-622-POS Reference Design are short point to point 50 MHz UL2 between the POS and the FPGA do not require any terminations.

A “series source terminating resistors” may be required in a system where the UTOPIA Bus drivers have a fast rise/fall time and the distance between the POS chip and the link layer device is substantial. If we consider that these CMOS UTOPIA drivers have typical 1ns edges then traces longer than 0.89in/2.26cm should be terminated. See section 9, “PCB considerations”, for detail on transmission lines.

Because the drivers are CMOS and have limited current drive/source capabilities, parallel far end terminations can’t be used. For point to point transmission like this, series source termination is a good option. The figure below illustrates the relative positioning and values of these series source termination resistors. Resistor values may vary depending on Zo transmission line impedance and the output impedance of the I/O driver.

Figure 27: System Interface Terminations



Notes:

- Terminations shown are for 3.3V Link Layer Device
- Zo (trace impedance) 65Ω

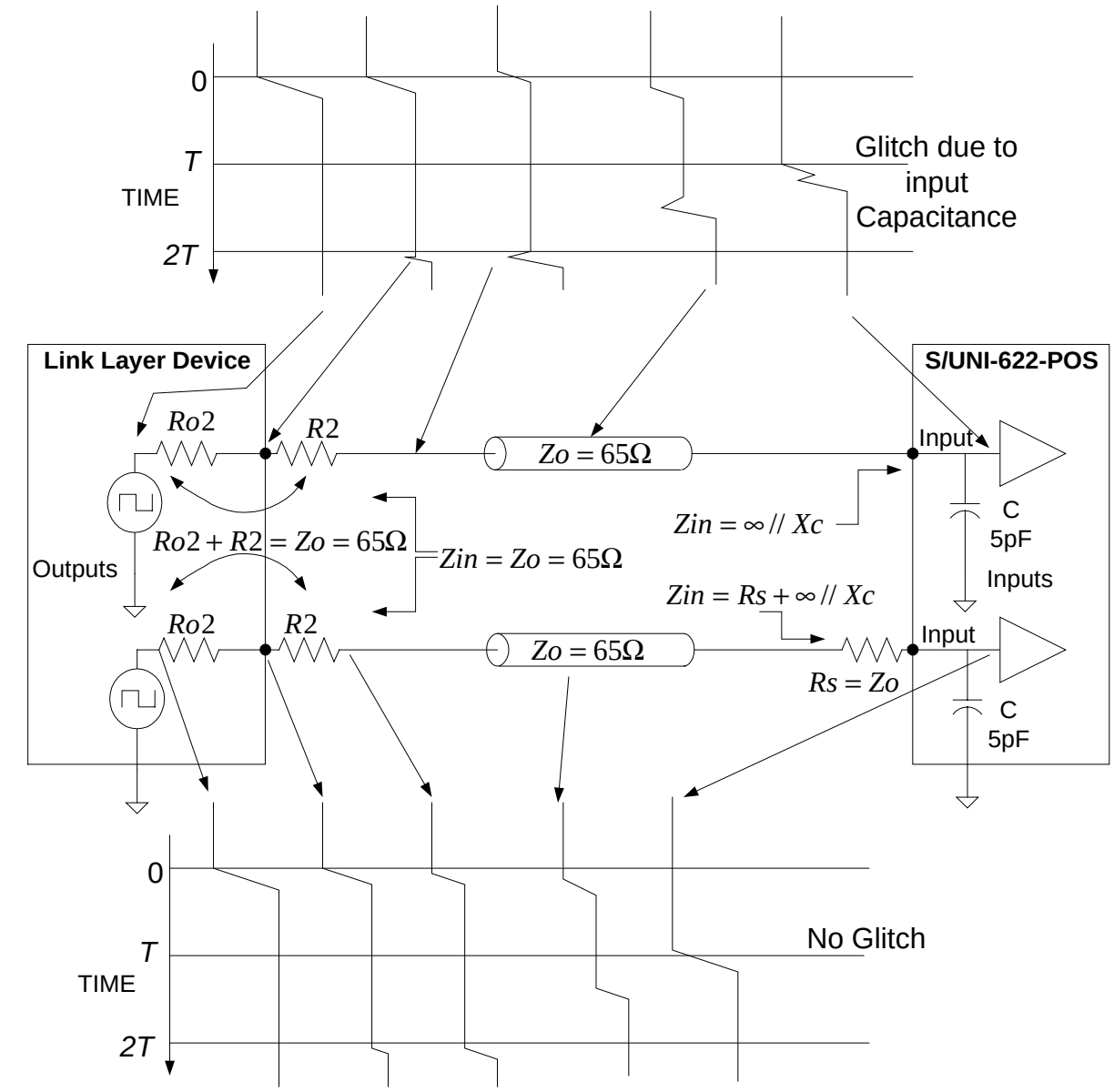
R1 = Zo – RO1 ≈ 56Ω R2 = Zo – RO2 ≈ 56Ω

This termination scheme assumes that the link layer device drives signals at 3.3V levels. Because of the relative uncertainty of the output impedance (RO1 and RO2), it’s best to have Zo as large as possible so that the output impedance

is as small as possible relative to Zo. However, a large Zo means a narrow, difficult to manufacture PCB trace. A small Zo would require wide traces and would take up a lot of PCB real-estate. However, a narrow trace is required to be able to route the trace between chip pins/balls. As a compromise, a 50ohm Zo was chosen for the 622MHz signals and the 77.76MHz clocks. The rest of the PCB traces are a compromise at 65 ohms. It is difficult to measure or control the a.c. output impedance of a driver consistently. In addition, this impedance is different for the rising and the falling edge. The impedance for device outputs is not typically published unless it's a "bus Driver" type of IC. However, for practical applications, the output a.c. impedance is typically around 10-25 ohms. In this case, if the traces were longer than 2.26cm, 56 ohm series resistors could have been used.

This "series source termination" scheme relies on the fact that the far end is infinite impedance. However, as shown in Figure 28: Series Source Termination, all CMOS type infinite impedance inputs have finite capacitive inputs of about 5pF. So, initially when the signal, rising or falling edge, hits the input pin, it looks like a short circuit until the capacitor is charged/discharged and then the input looks like an infinite impedance. This causes a small glitch reflected back which may cause a problem. A simple way to solve this is to put another series resistor (65 ohm in this case), right at the input to the far-end pin, equal to the impedance of the transmission line.

Figure 28: Series Source Termination



12 TYPICAL JITTER MEASUREMENTS

12.1 Intrinsic Jitter

This reference board exceeded GR-253-CORE Intrinsic Jitter specifications of 0.1 UI p-p and 0.01 UI rms. Typical Transmit Intrinsic jitter measurements are as follows. All measurements were taken with an HP 717 jitter test set transmitting PRBS-23 data, and the 12 kHz HP filter enabled on the RX side as per GR-253-CORE. Because the HP717 did not have provisions for originating ATM cells, UTOPIA drop-side loop-back was not possible during the jitter tests.

Table 9: Intrinsic jitter calibration tests

ATM/SONET Data Source	Jitter UI_{pp}	Jitter UI_{rms}
Adtech AX4000	0.117	0.014
HP 717	0.004	0.001

Table 10: Intrinsic jitter test results with HP 717

Test Method	Jitter UI_{pp}	Jitter UI_{rms}
Standard test: Non-loop time mode, (using the on board PECL 77.76 MHz) reference oscillator) and HP717 originating optical data into POS reference board.	**0.056**	**0.005**
No optical signal into the POS reference board. Non-loop time mode, using the on board PECL 77.76 MHz reference oscillator.	0.048	0.003
Serial Line Loop Back. SLLE bit enabled in register 0x02 of POS chip with data originated from HP 717	0.009	0.002
Loop time mode using a HP717 tester as the OC-12 optical data source and LOOPT bit set in Register 0x02 of the POS chip.	0.007	0.002

12.2 Jitter Tolerance

Jitter Tolerance was measured using an HP 717 Jitter Tolerance test set with and without optical attenuation. We used 5V ODL (HP's HFCT5208B) and 3.3V ODL (Siemens V23826-H18-C363) and the results below exceeded Bellcore requirements. Typical measurements are shown below.

Figure 29: Jitter Tolerance Test Set-up

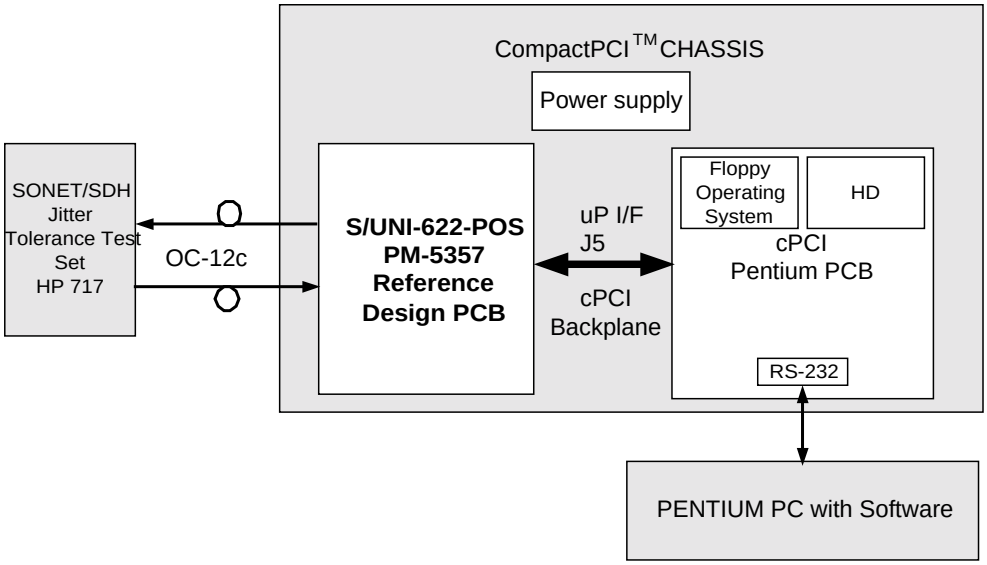


Figure 30: Jitter Tolerance without Optical Attenuation

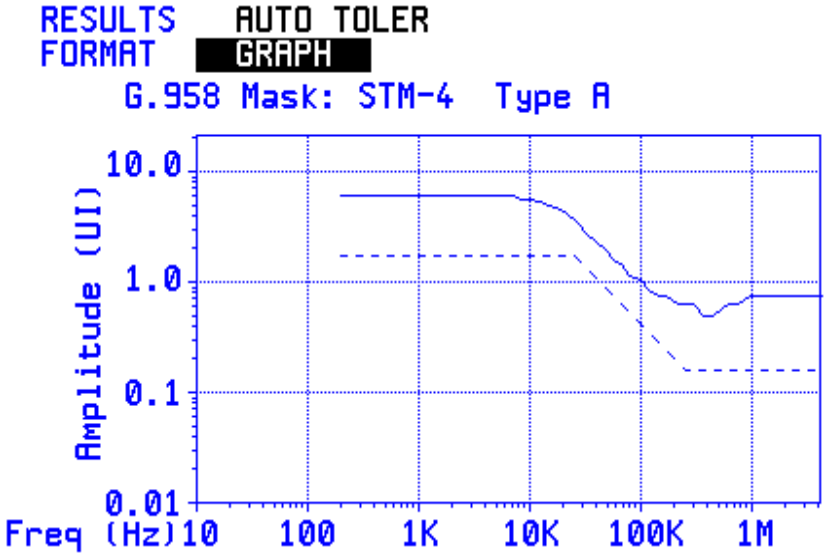


Figure 31: Jitter Tolerance with Optical Attenuation

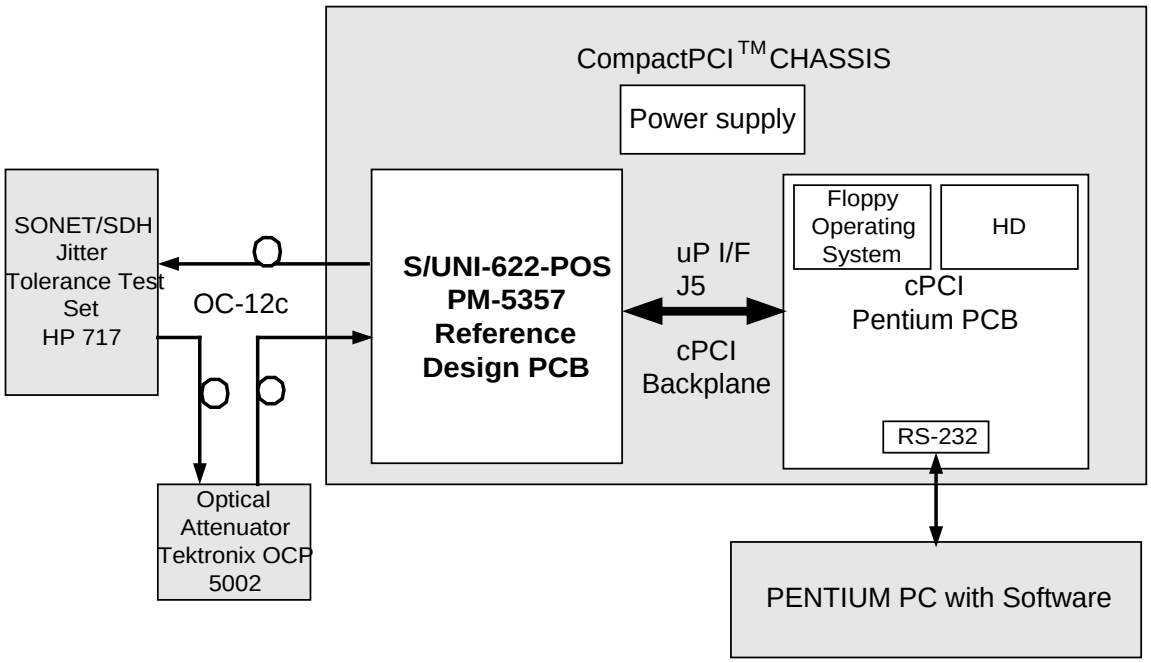
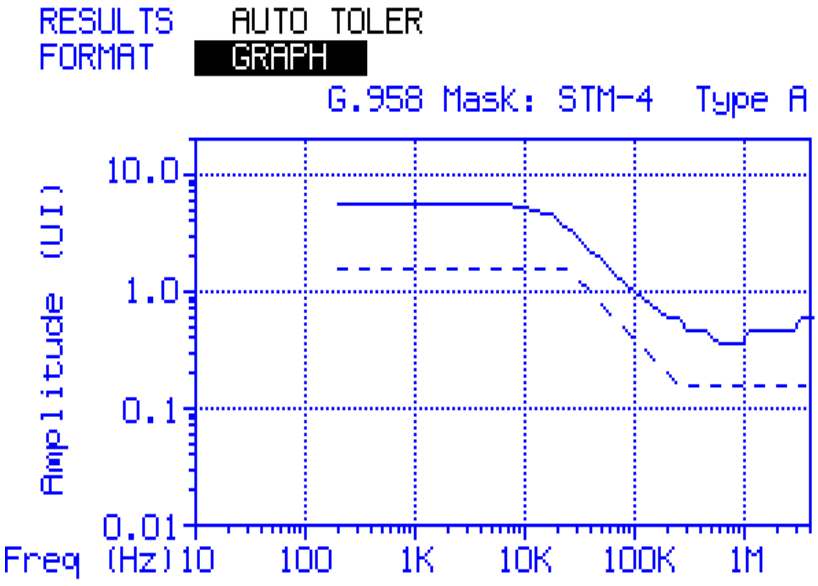


Figure 32: Jitter Tolerance with Optical Attenuation



13 OSCILLOSCOPE MEASUREMENTS

This section presents sample oscilloscope measurements. They were performed with a fiber loop-back cable installed and TCLK was used as the scope trigger.

13.1 Differential Scope Probe

A lot of the signals shown here were done with a Tektronix differential probe. The measurements taken show that the signal has a peak to peak voltage of twice of what we expected. As illustrated below, this is because the probe chooses one of the inputs as the reference, and measures the other signal with respect to this reference:

Figure 33: Differential scope probe analysis

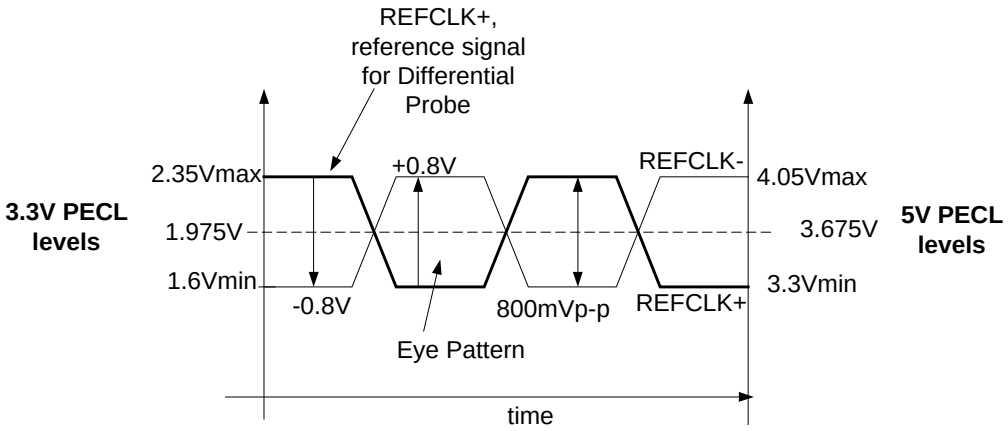
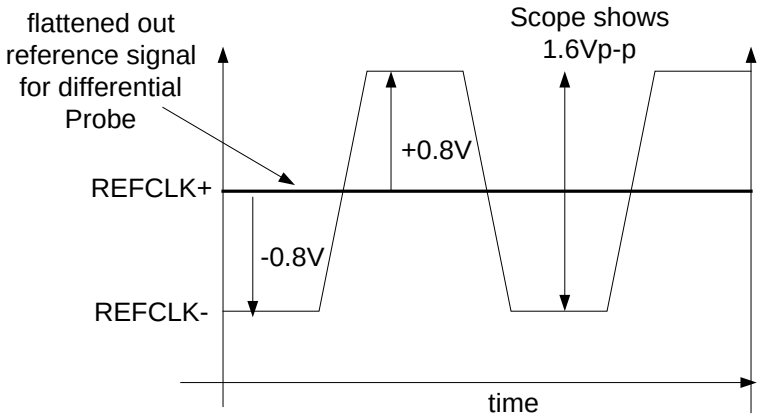


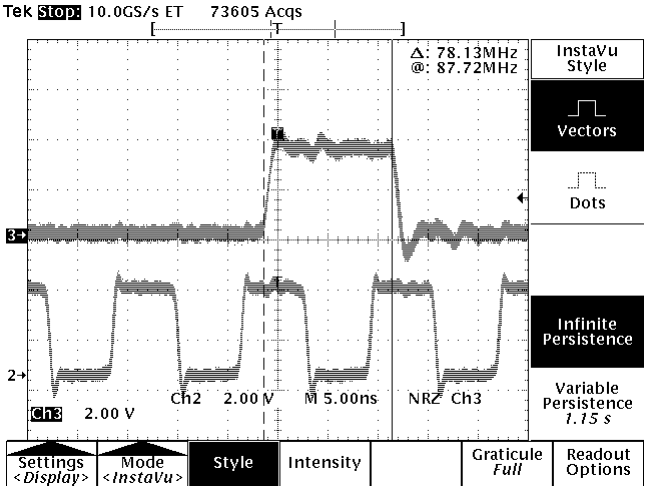
Figure 34: What the differential probe actually sees



13.2 RFPO (Receive Frame Pulse Out)

The board is in Fiber loopback mode. Channel 3 is RFPO (pin AB19 - PM5357) and Channel 2 is the TCLK (pin B19- PM5357) used as the trigger.

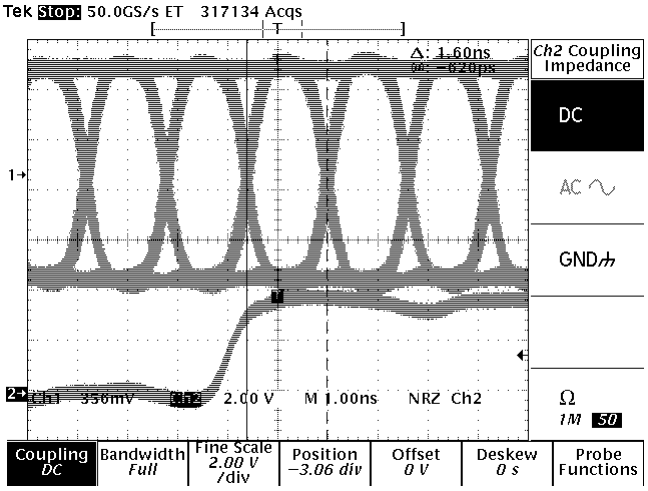
Figure 35: Diagram RFPO (Receive Frame Pulse)



13.3 RXD+/- (Receive Data)

Board is in fiber Loopback. Channel 1 is a differential measurement of the RXD+/- (across the 100 ohm terminating resistor near the RXD+/- pins of the PM5357) and Channel 2 is the TCLK (pin B19 - PM5357) used as the trigger.

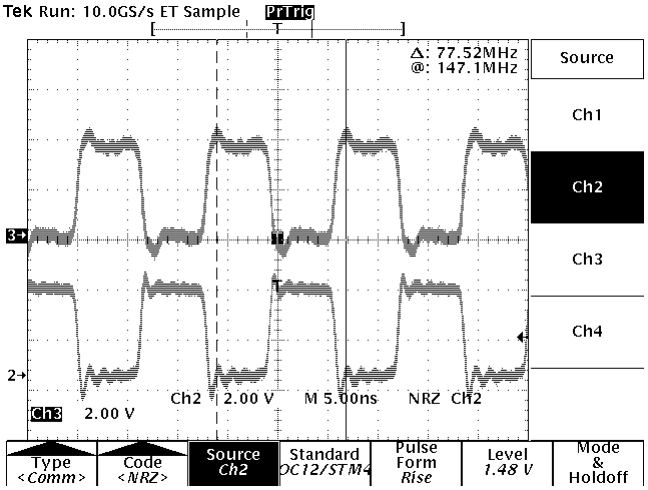
Figure 36: RXD+/- Eye (Receive Data)



13.4 RCLK (Recovered Clock)

The PCB is in fiber loopback. Channel two, the trigger, is the Transmit 77Mhz clock and channel 3 is the recovered divide by eight Receive clock, RCLK.

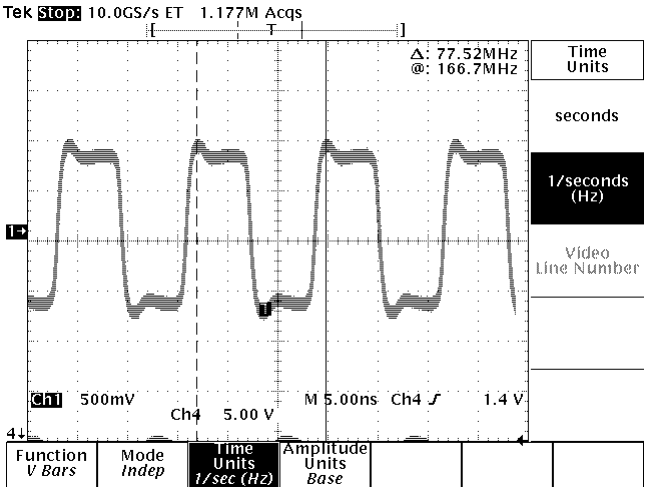
Figure 37: RCLK (Recovered Clock)



13.5 REFCLK+/-

Differential scope probe measurement of the Reference clock, REFLCK+ and REFCLK-, at the terminating 100 ohm resistor. Due to an anomaly of the differential probe, the clock is actually 0.8Vp-p not 1.6Vp-p as shown below. The probe looks at one of the signals and uses as a reference and thus the other signal is either –0.8V or +0.8V with respect to that reference. See section “Differential Scope Probe” for explanation.

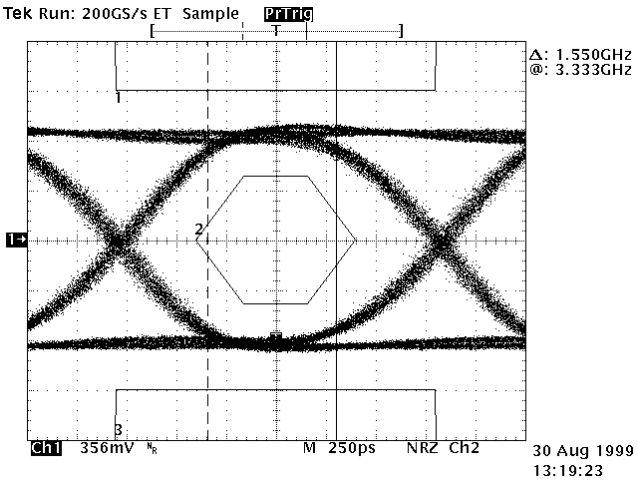
Figure 38: REFCLK+/-, 77.76mHz Reference clock



13.6 RXD+/- eye with OC-12 template

Differential scope measurement of the TXD+/- signal at the RXD pin 100 ohm terminating resistor. Included in this figure is the OC-12 mask.

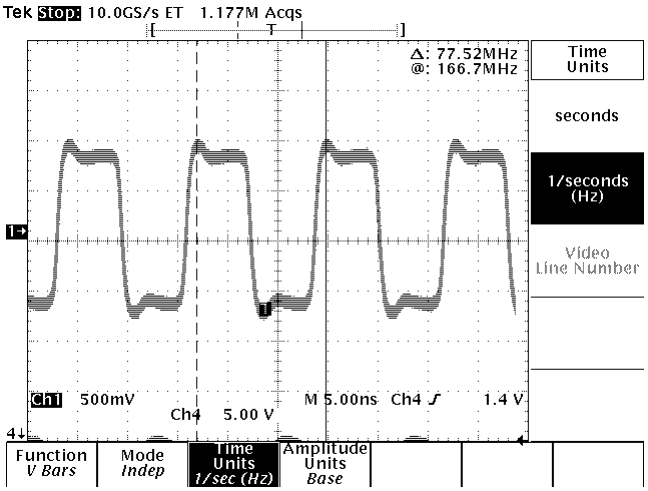
Figure 39: RXD+/- eye with OC-12 template



13.7 Transmit Reference Clock, TCLK 77.76MHz

This is a differential 0.8Vp-p clock. The Differential probe shows this signal to be twice the voltage. . See section “Differential Scope Probe” for explanation.

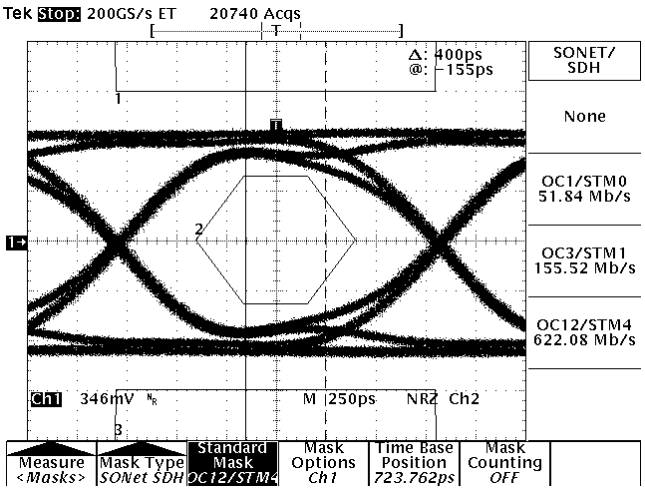
Figure 40: 77.7600 MHz Reference Clock



13.8 TXD+/- Eye with OC-12 Template

This differential signal was measured across the termination 49.9 ohm resistors close to the Optical Device.

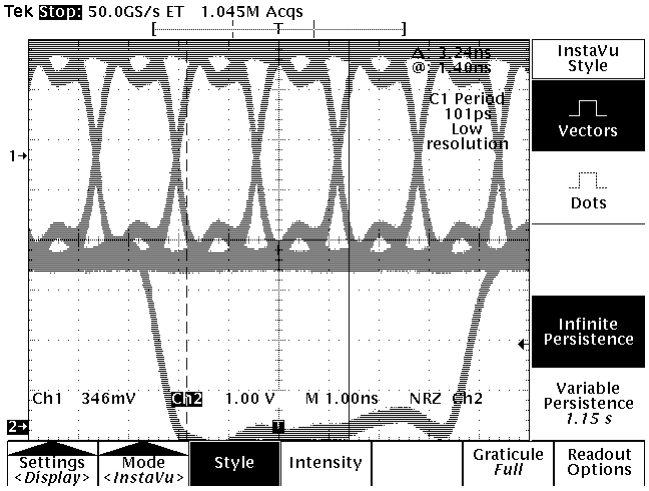
Figure 41: TXD+/- Eye with OC-12 Template



13.9 Differential TXD+/- with TCLK as the trigger

Channel 1 shows the TXD+/- signal and channel 2 shows the TCLK trigger.

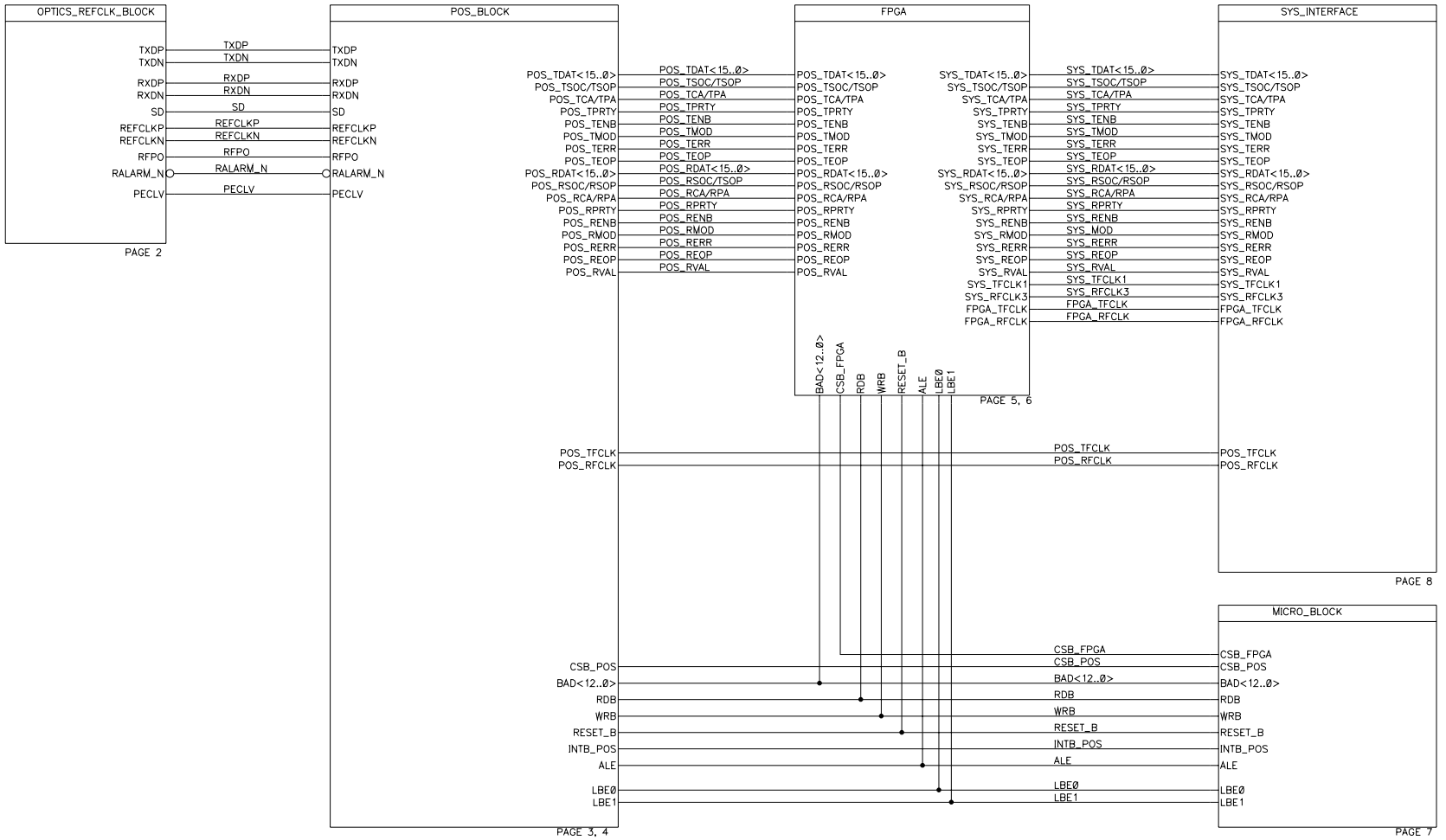
Figure 42: Differential TXD+/- with TCLK as Trigger



14 SCHEMATICS REVISION 3

The enclosed PCB (silk-screened as "…1.0 1999") layout is manufactured to Issue 2 schematics. The enclosed Issue 3 schematic are only slightly modified unreleased Rev 2 schematics. Please see the "**Public Revision History**" section in the front of this document for detail change list.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING

TITLE=622_POS_ROOT
ABBREV=622_POS_ROOT
LAST_MODIFIED=Mon Dec 20 14:14:20 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-981070 *DRAFT* DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: 99/03/29
TITLE: S/UNI-622-POS REFERENCE DESIGN ROOT DRAWING	REVISION NUMBER: 3
ENGINEER: PMC-SIERRA SA	PAGE: 1 OF 8

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

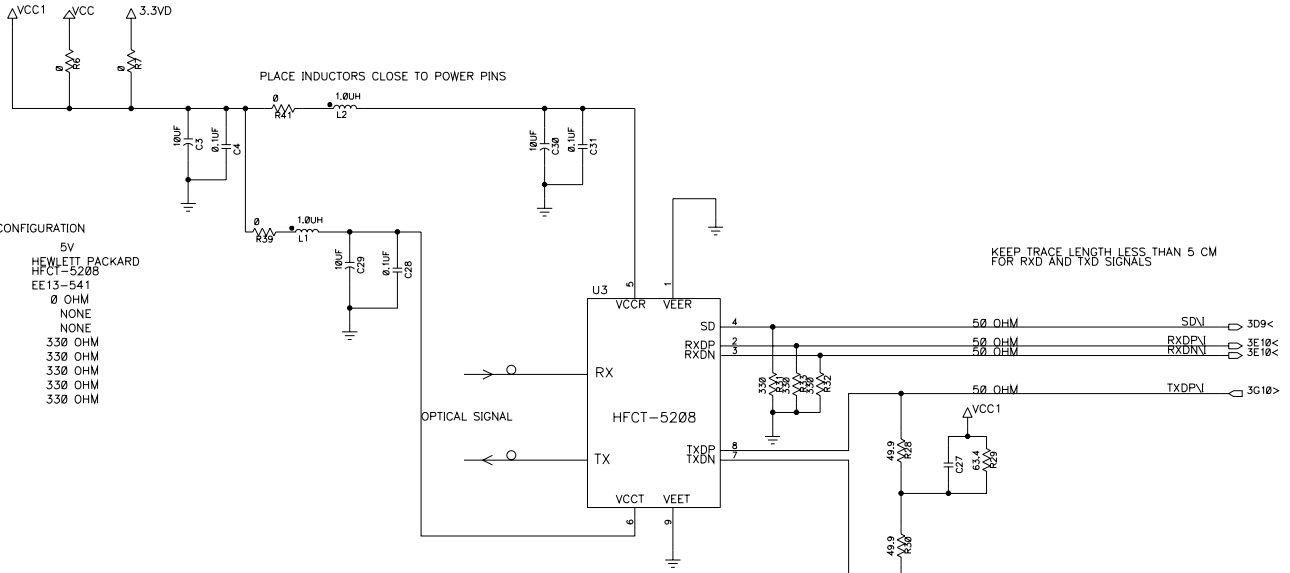
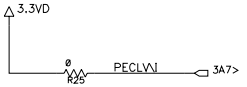
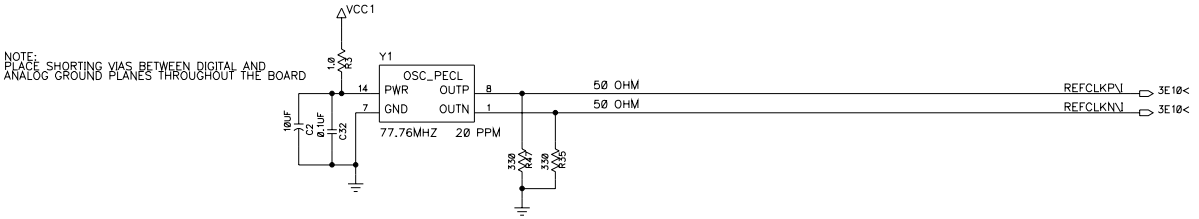


TABLE: 3.3V AND 5V LINE INTERFACE CONFIGURATION

REF. DES.	3.3V	5V
U3	SIEMENS V23826-H18-C363	HEWLETT PACKARD HFCT-5208
Y1	EE14-541	EE13-541
R6	NONE	Ø OHM
R7	Ø OHM	NONE
R25	Ø OHM	NONE
R31	150 OHM	330 OHM
R32	150 OHM	330 OHM
R33	150 OHM	330 OHM
R35	150 OHM	330 OHM
R47	150 OHM	330 OHM

KEEP TRACE LENGTH LESS THAN 5 CM
FOR RXD AND TXD SIGNALS



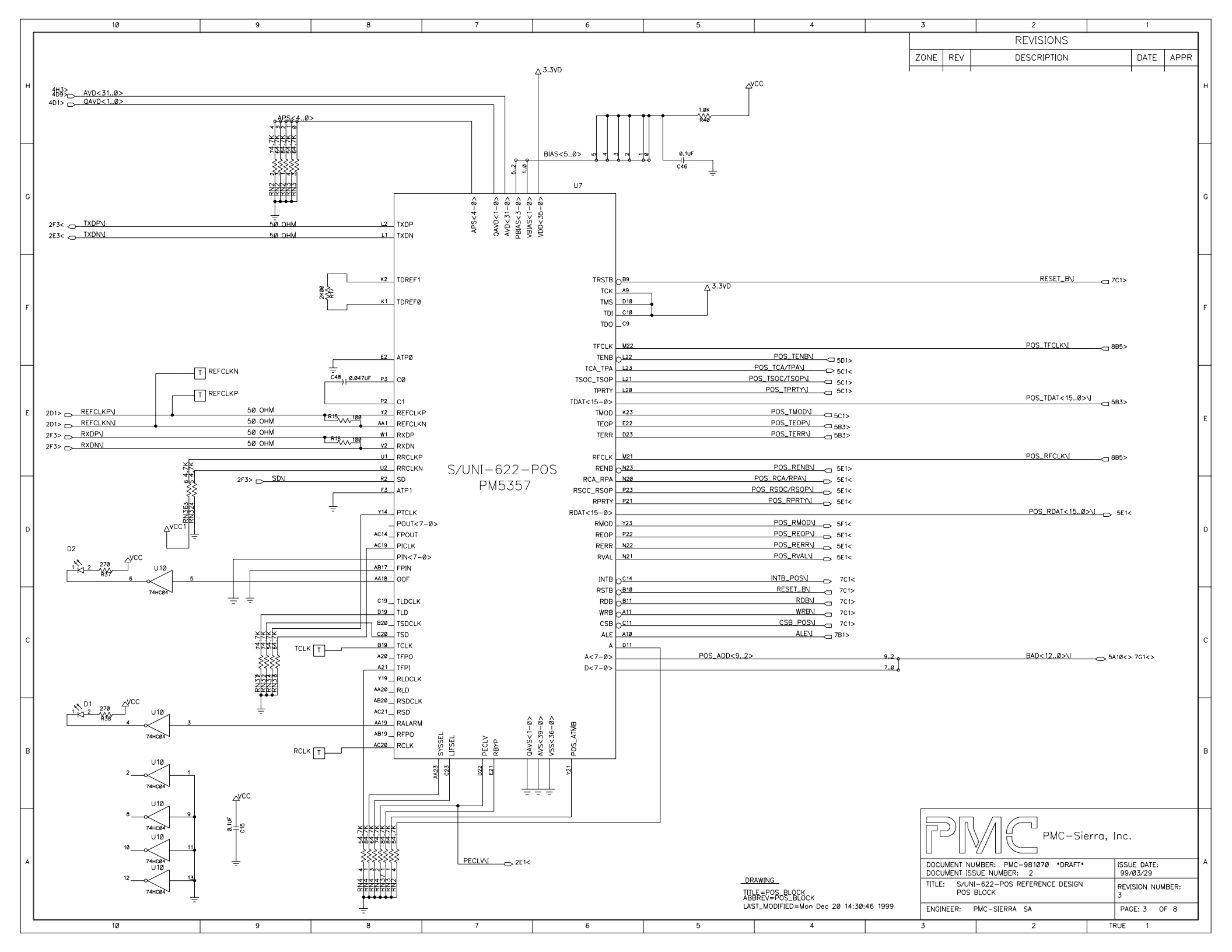


DRAWING

TITLE=OPTICS_REFCLK_BLOCK
ABBREV=OPTICS_REFCLK_BLOCK
LAST_MODIFIED=Mon Dec 20 14:30:41 1999

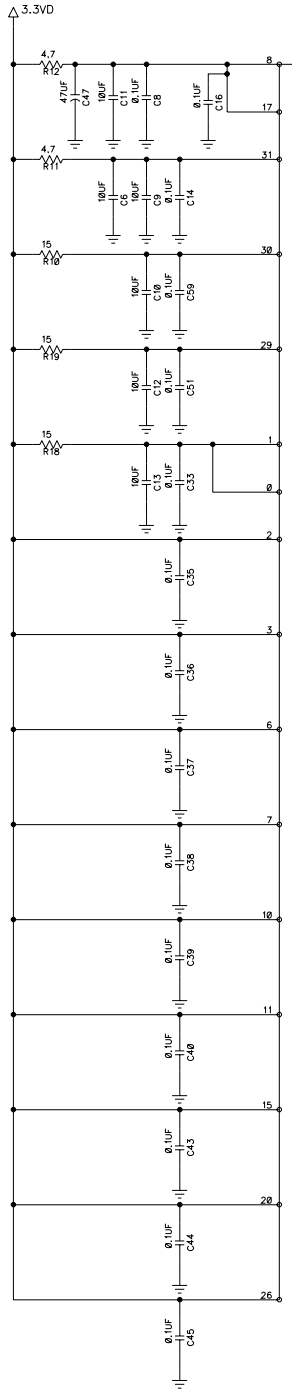
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-981070 *DRAFT* DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: 99/03/29
TITLE: S/UNI-622-POS REFERENCE DESIGN OPTICS_REFCLK_BLOCK	REVISION NUMBER: 3
ENGINEER: PMC-SIERRA SA	PAGE: 2 OF 8


REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPR
S/UNI-622-POS
PM5357
U7
3.3VD
VCC
AVD<31..0>
QAVD<1..0>
APS<4..0>
BIAS<5..0>
1.0K
R40
0.1UF
C46
TXDP
TXDN
50 OHM
TDREF1
TDREF0
ATP0
C0
C1
0.047UF
C48
REFCLKN
REFCLKP
REFCLKP\
REFCLKN\
RXDP\
RXDN\
R15
R16
100
SD\
SD
ATP1
PTCLK
POUT<7-0>
FPOUT
PICLK
PIN<7-0>
FPIN
OOF
TLDCLK
TLD
TSDCLK
TSD
TCLK
TFPO
TFPI
RLDCLK
RLD
RSDCLK
RSD
RALARM
RFPO
RCLK
SYSSEL
LIFSEL
PECLV
RBYP
QAVS<1-0>
AVS<39-0>
VSS<36-0>
POS_ATMB
PECLV\
2E1<
TRSTB
TCK
TMS
TDI
TDO
RESET_B\
TFCLK
TENB
TCA_TPA
TSOC_TSOP
TPRTY
TDAT<15-0>
TMOD
TEOP
TERR
RFCLK
RENB
RCA_RPA
RSOC_RSOC
RPRTY
RDAT<15-0>
RMOD
REOP
RERR
RVAL
INTB
RSTB
RDB
WRB
CSB
ALE
A
A<7-0>
D<7-0>
POS_ADD<9..2>
POS_TFCLK\
POS_TENB\
POS_TCA/TPA\
POS_TSOC/TSOP\
POS_TPRTY\
POS_TDAT<15..0>\
POS_TMOD\
POS_TEOP\
POS_TERR\
POS_RFCLK\
POS_RENB\
POS_RCA/RPA\
POS_RSOC/RSOP\
POS_RPRTY\
POS_RDAT<15..0>\
POS_RMOD\
POS_REOP\
POS_RERR\
POS_RVAL\
INTB_POS\
RESET_B\
RDB\
WRB\
CSB_POS\
ALE\
BAD<12..0>\
D1
D2
270
R37
R38
74HC04
VCC1
0.1UF
C15
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-981070 *DRAFT*
DOCUMENT ISSUE NUMBER: 2
ISSUE DATE: 99/03/29
TITLE: S/UNI-622-POS REFERENCE DESIGN POS BLOCK
REVISION NUMBER: 3
ENGINEER: PMC-SIERRA SA
PAGE: 3 OF 8
DRAWING
TITLE=POS_BLOCK
ABBREV=POS_BLOCK
LAST_MODIFIED=Mon Dec 20 14:30:46 1999

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

POWER DECOUPLING FOR SENSITIVE ANALOG PINS

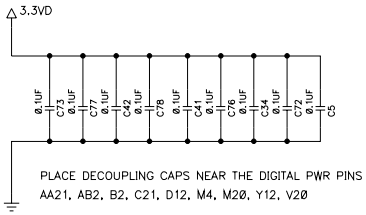


NOTE:

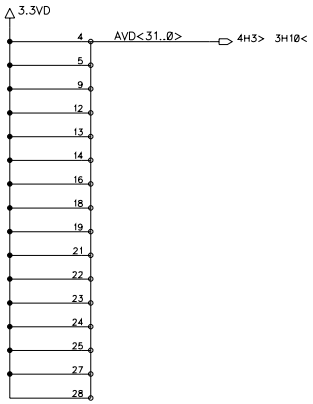
-PLACE 0.1UF CAPACITORS AS CLOSE TO ASSIGNED CHIP PINS AS POSSIBLE.

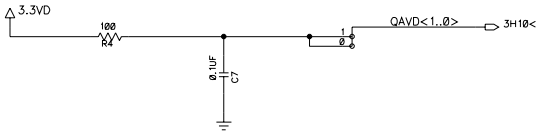
-RESISTORS AND 10UF CAPACITORS CAN BE FURTHER AWAY FROM THE CHIP.

-10UF CAPACITORS ARE CERAMIC X5R 10V, TAIYO-YUDEN LMK325BJ106MN



PLACE DECOUPLING CAPS NEAR THE DIGITAL PWR PINS
AA21, AB2, B2, C21, D12, M4, M20, Y12, V20





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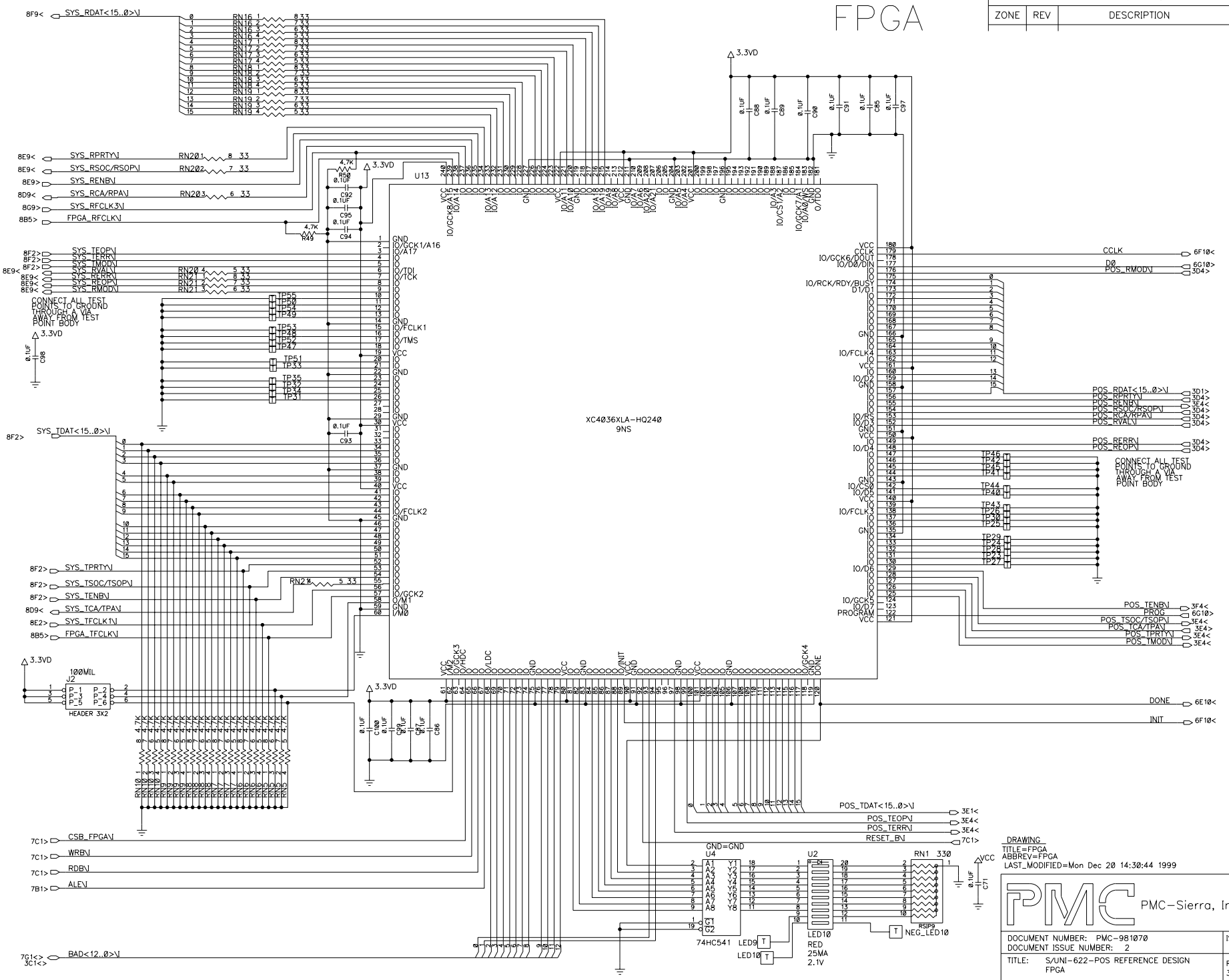
TITLE=POS_BLOCK
ABBREV=POS_BLOCK
LAST_MODIFIED=Mon Dec 20 14:30:47 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-981070 *DRAFT* DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: 99/03/29
TITLE: S/UNI-622-POS REFERENCE DESIGN POS BLOCK	REVISION NUMBER: 3
ENGINEER: PMC-SIERRA SA	PAGE: 4 OF 8

FPGA

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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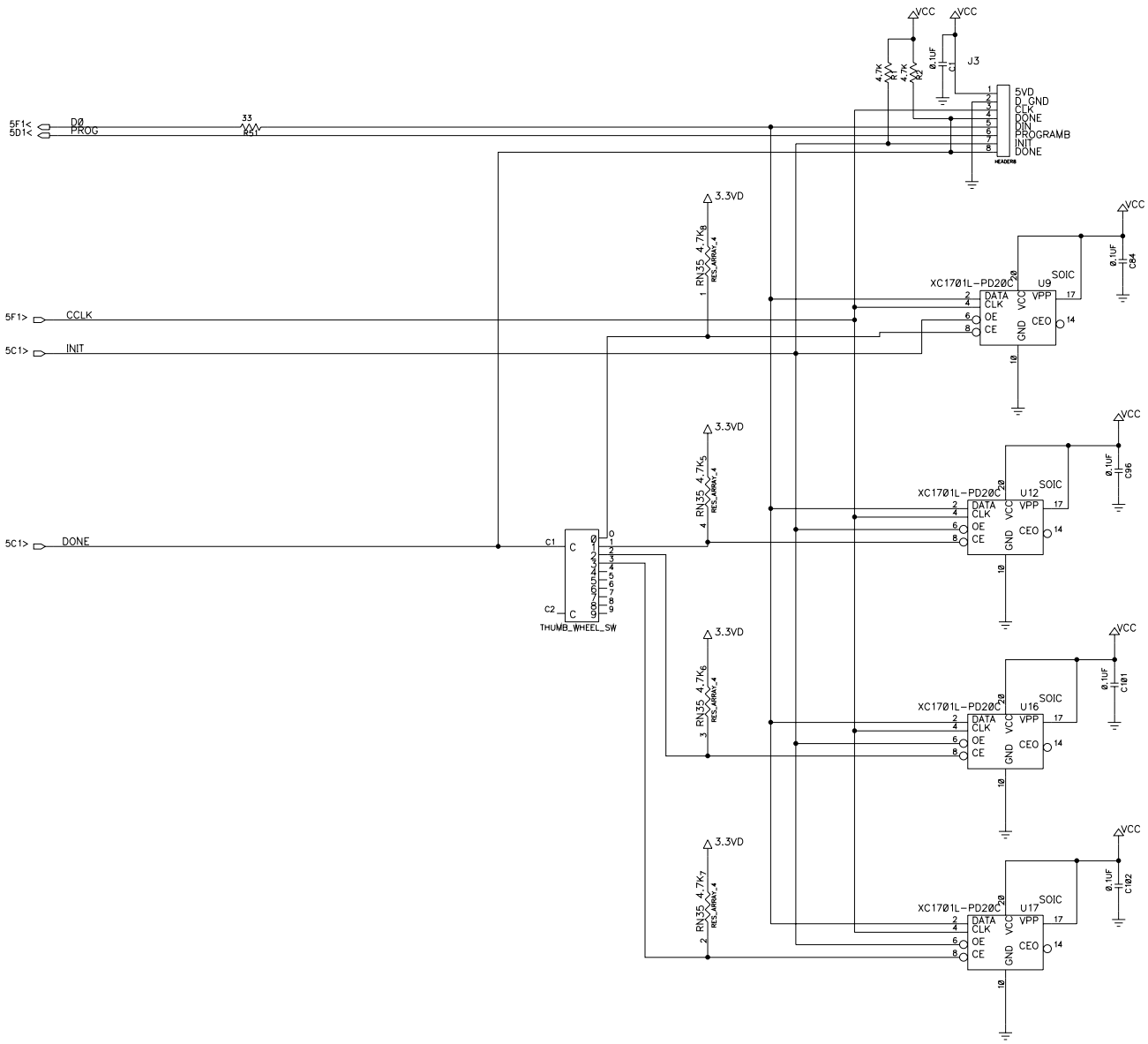
LAST_MODIFIED=Mon Dec 20 14:30:44 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-981070 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: 99/03/29
TITLE: S/UNI-622-POS REFERENCE DESIGN FPGA	REVISION NUMBER: 3
ENGINEER: PMC-SIERRA SA	PAGE: 5 OF 8

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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LAST_MODIFIED=Mon Dec 20 14:30:45 1999

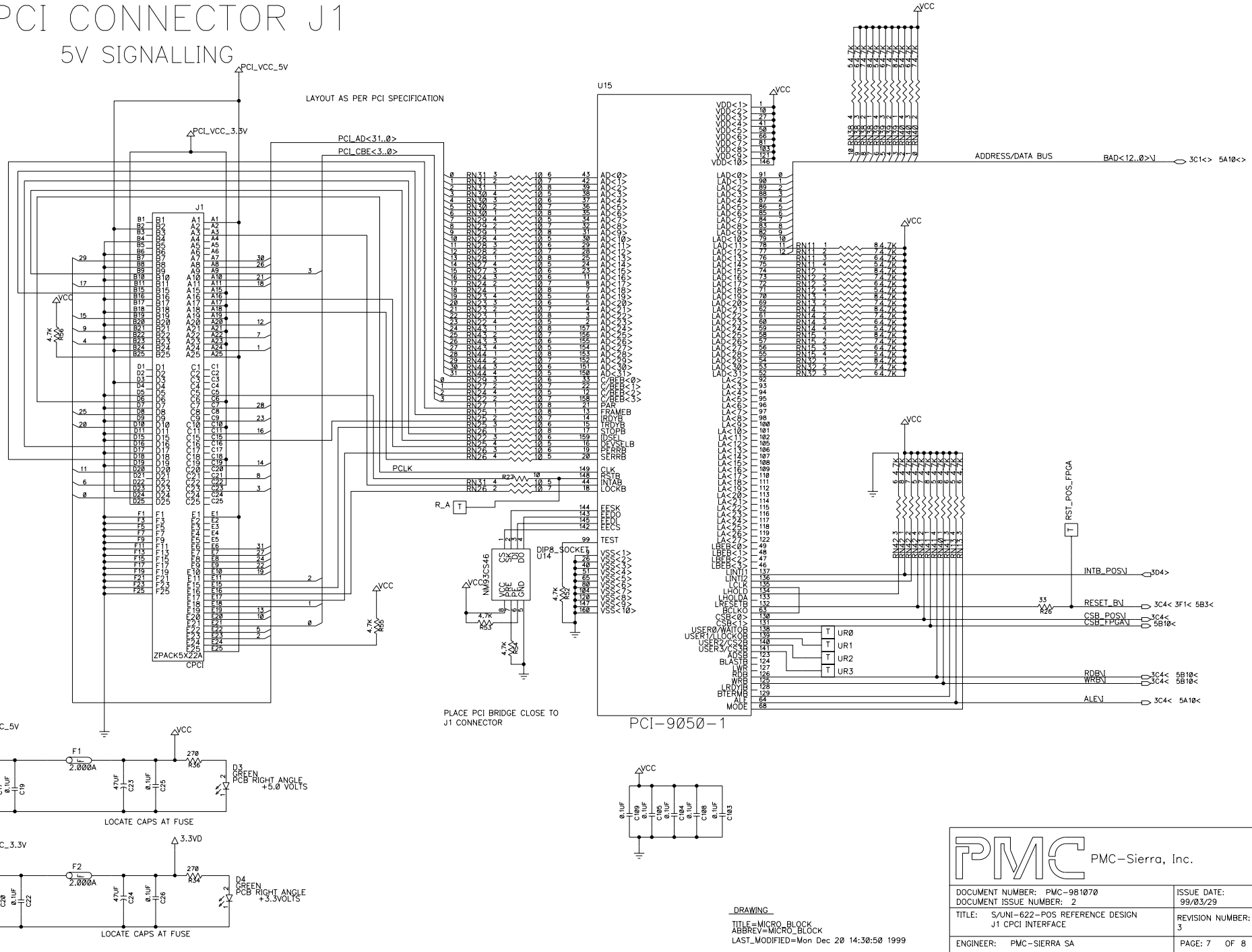
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-981070 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: 99/03/29
TITLE: S/UNI-622-POS REFERENCE DESIGN FPGA	REVISION NUMBER: 3
ENGINEER: PMC-SIERRA SA	PAGE: 6 OF 8

CPCI CONNECTOR J1

5V SIGNALLING

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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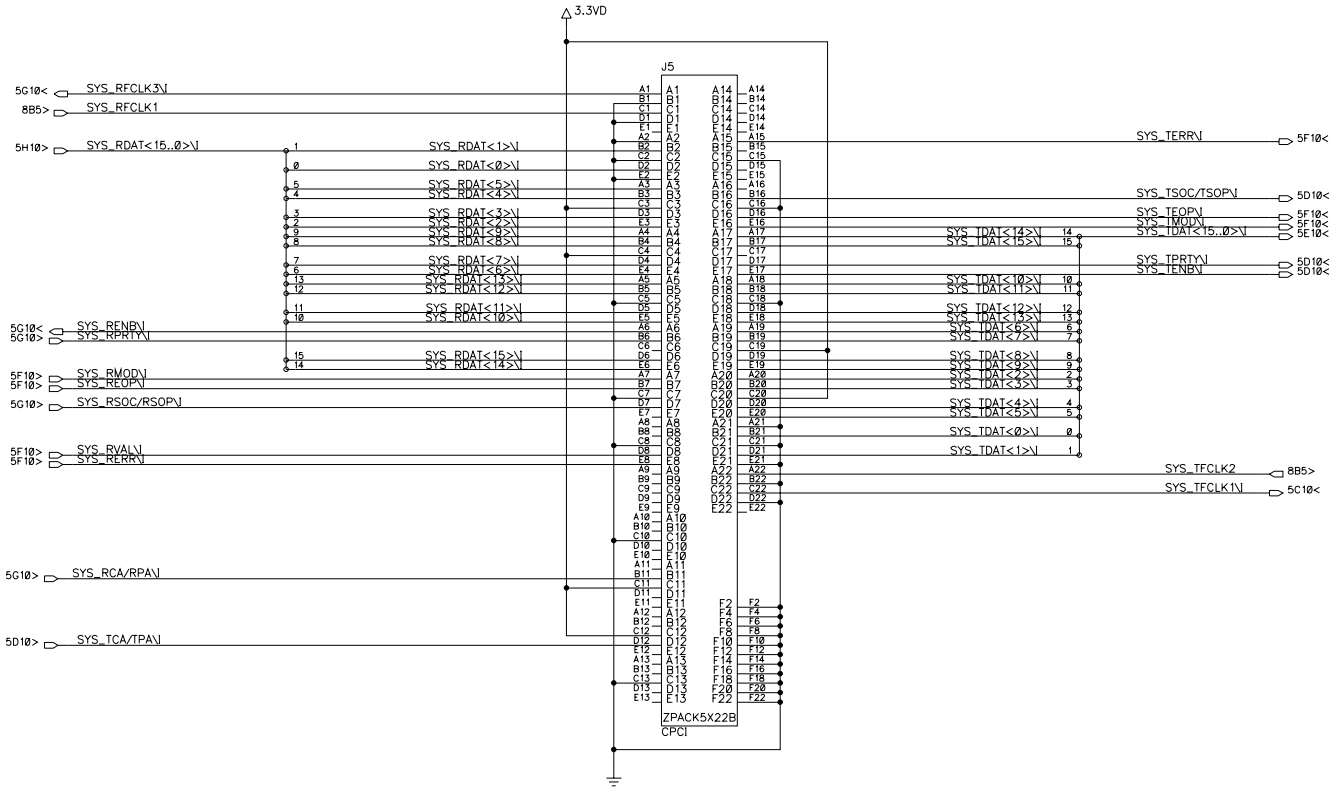
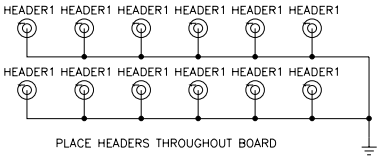
ABBREV=MICRO_BLOCK
LAST_MODIFIED=Mon Dec 20 14:30:50 1999

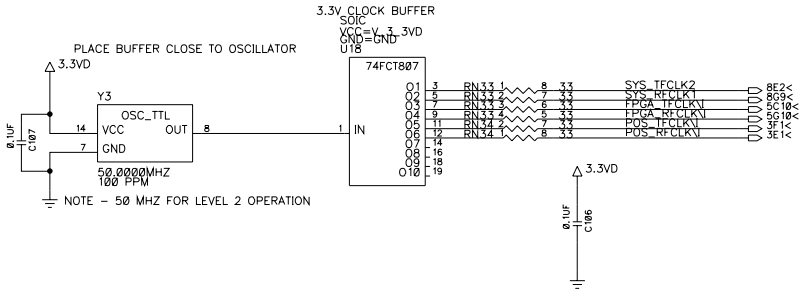
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-981070 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: 99/03/29
TITLE: S/UNI-622-POS REFERENCE DESIGN J1 CPCI INTERFACE	REVISION NUMBER: 3
ENGINEER: PMC-SIERRA SA	PAGE: 7 OF 8

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







DRAWING

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ABBREV=SYS_INTERFACE
LAST_MODIFIED=Mon Dec 20 14:30:52 1999

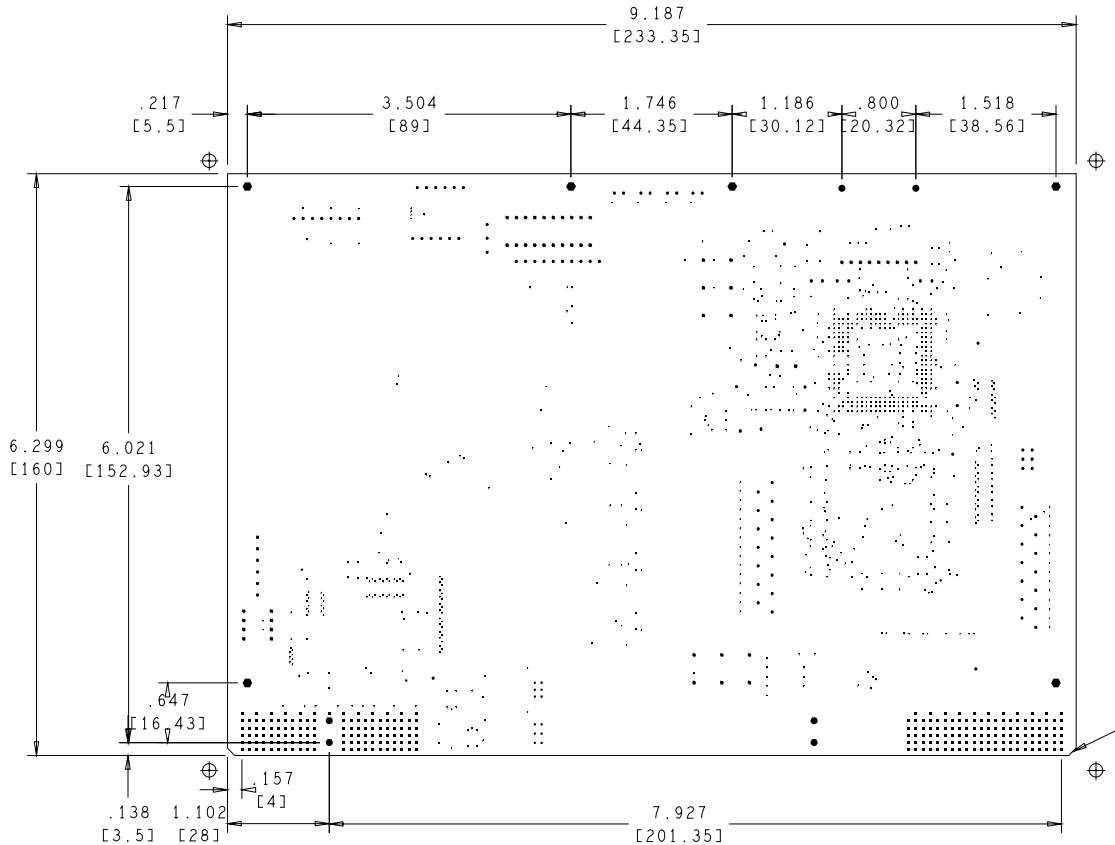
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-981070 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: 99/03/29
TITLE: S/UNI-622-POS REFERENCE DESIGN SYSTEM INTERFACE	REVISION NUMBER: 3
ENGINEER: PMC-SIERRA SA	PAGE: 8 OF 8

15 PCB LAYOUT REVISION 1

The enclosed PCB (silk-screened as "…1.0 1999") layout is manufactured to Issue 2 schematics. The enclosed Issue 3 schematic are only slightly modified unreleased Rev 2 schematics. Please see the "**Public Revision History**" section in the front of this document for detail change list.

REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED



ARTWORK FILM
TOP LAYER
3V3 PLANE
GROUND PLANE
SIG1 LAYER
SIG2 LAYER
VCC PLANE
GNDA PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
SOLDER PASTE TOP
SOLDER PASTE BOTTOM
MECH DRAWING
ASSY TOP
ASSY BOTTOM

FINISHED HOLES SIZE			
All Units are in mils			
FIGURE	SIZE	PLATED	QTY
·	13.0	PLATED	859
•	25.0	PLATED	244
·	25.0	PLATED	17
•	36.0	PLATED	101
•	42.0	PLATED	51
•	79.0	PLATED	2
•	78.74	NOT PLATED	4
•	106.299	NOT PLATED	6

PMC-SIERRA S/UNI-622-POS REV 1.0 1999

Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
FR-4	DIELECTRIC	-------	-------	5 mil	4.5
COPPER	CONDUCTOR	3V3 PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	3.0 mil	4.5
COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	8.0 mil	4.5
COPPER	CONDUCTOR	SIG1	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	20 mil	4.5
COPPER	CONDUCTOR	SIG2	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	8 mil	4.5
COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	3 mil	4.5
COPPER	CONDUCTOR	GNDA PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	5 mil	4.5
COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------

Note: All 8 mils traces are 50 Ohm controlled impedance.
All 5 mils traces are 65 Oms controlled impedance.

Notes:

1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers.
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are spedified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN			
TOLERANCES ON:				
2 PL DECIMALS ±	CHECKED			
3 PL DECIMALS ±	ENGRG			
ANGLES ±	ISSUED			
FRACTIONS ±				

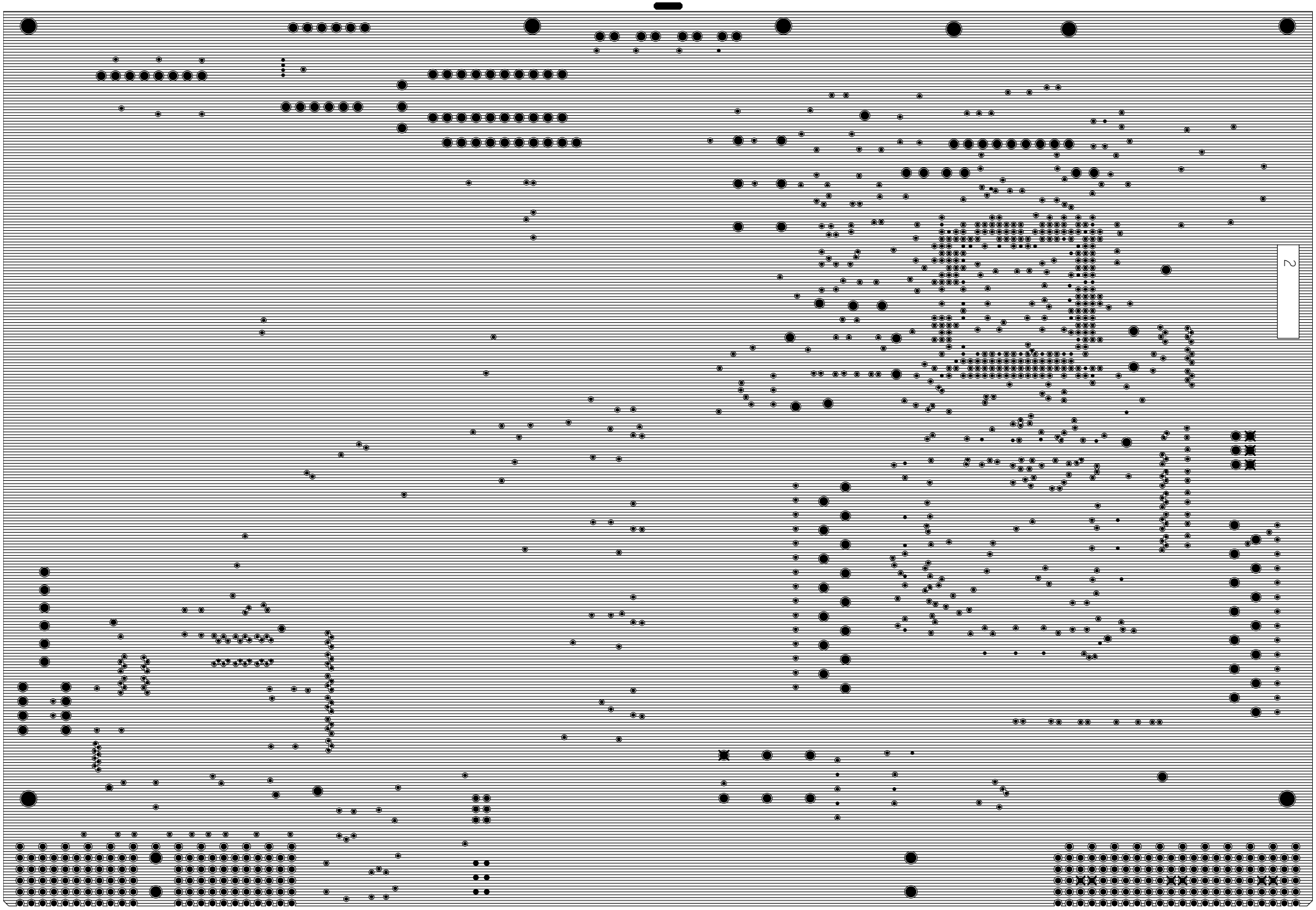
PMC-Sierra, Inc.

105-8555 Baxter Place, Burnaby B.C.
Canada, V5A 4V7

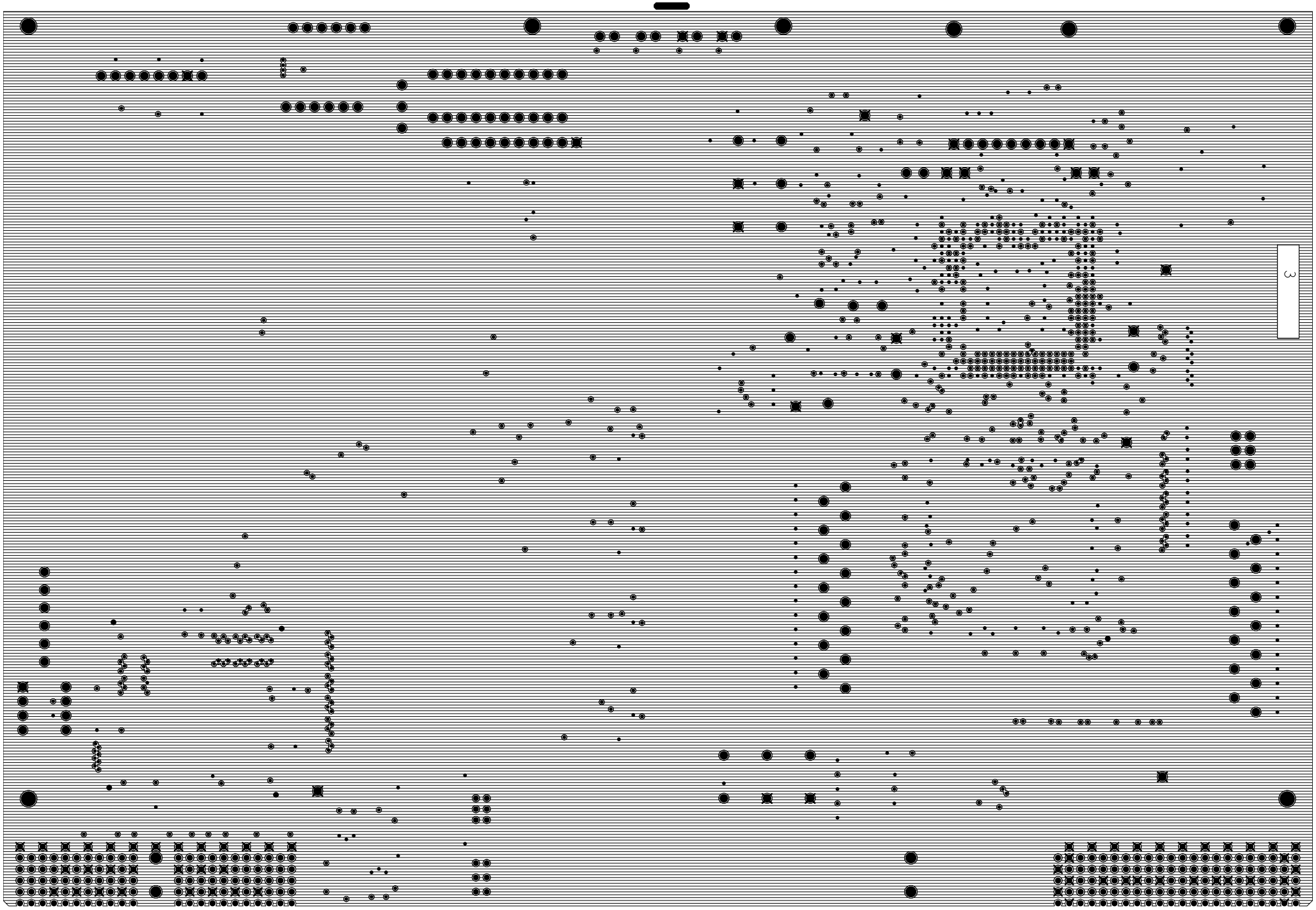
Tel: 604 415-6000 Fax: 604 415-6200

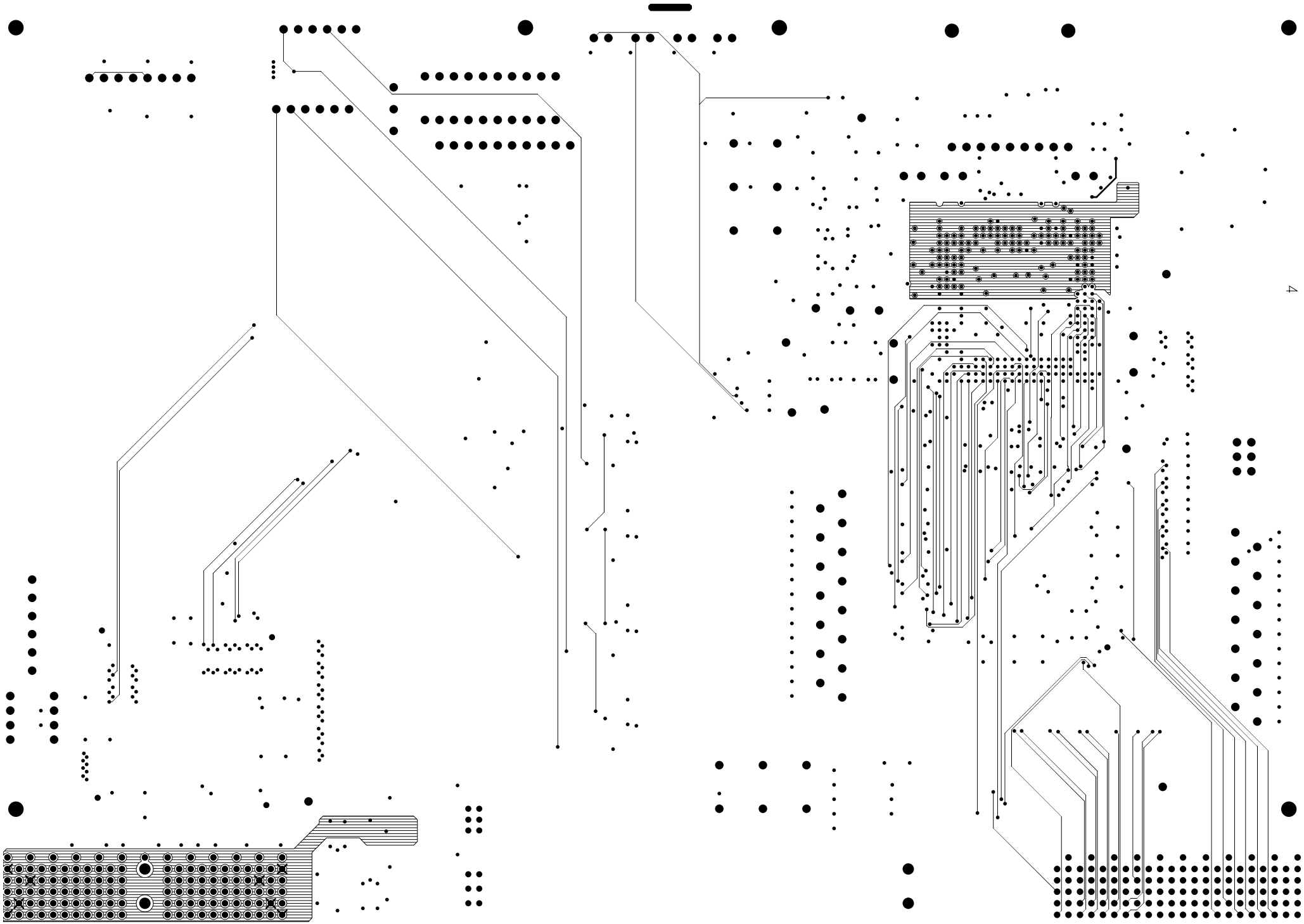
SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF

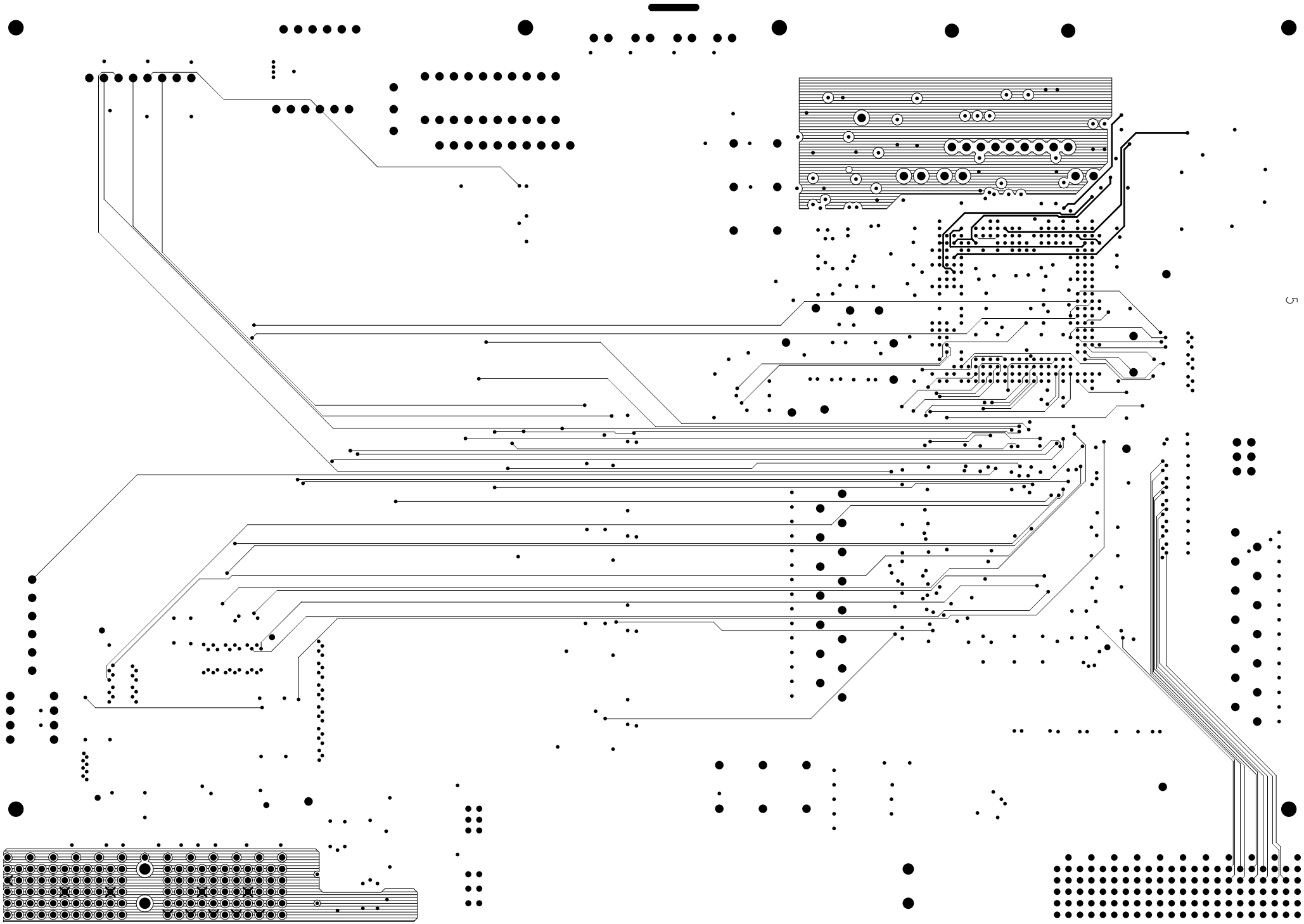
3V3 PLANE



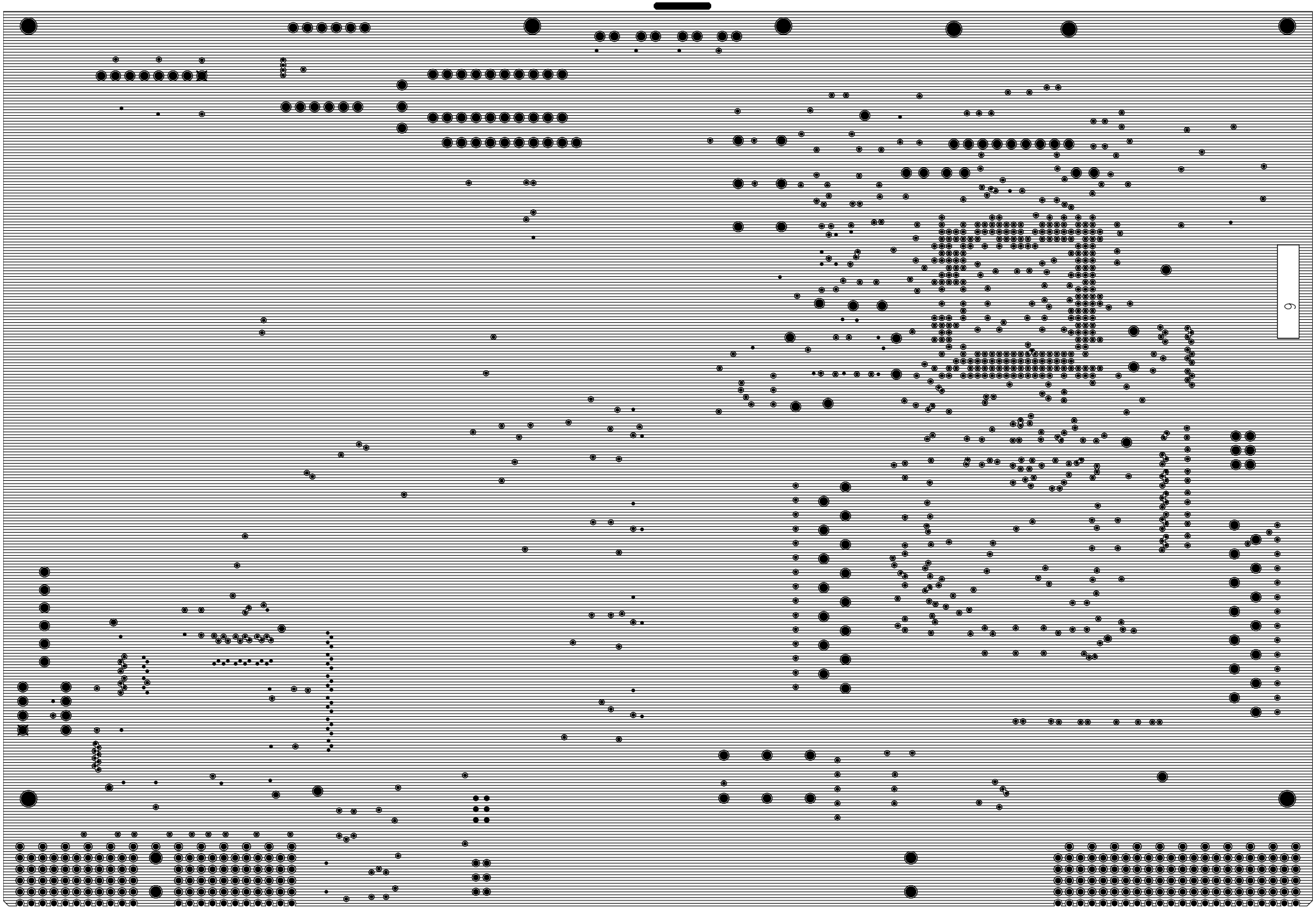
GND_PLANE



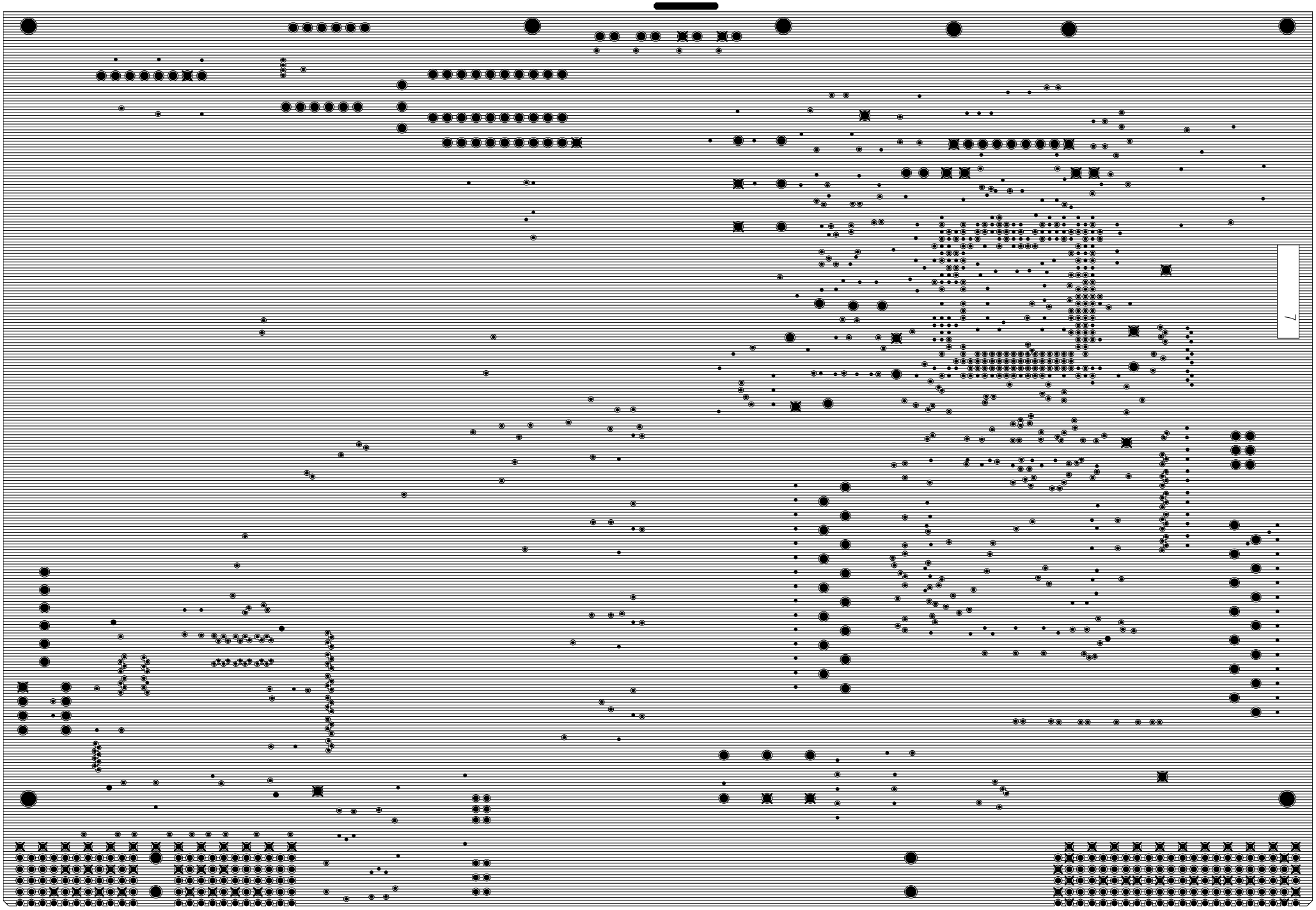




VCC_PLANE

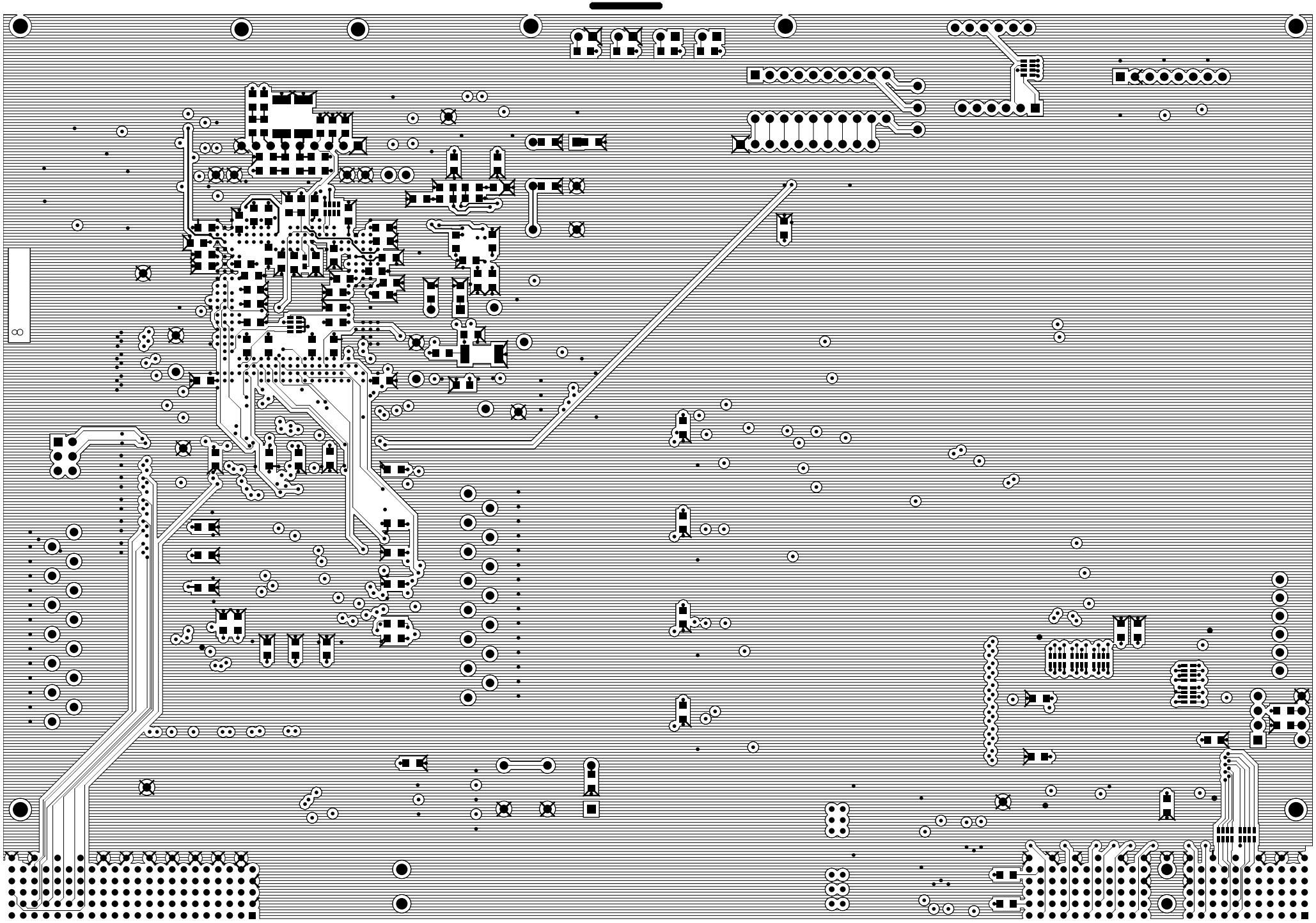


GNDA_PLANE

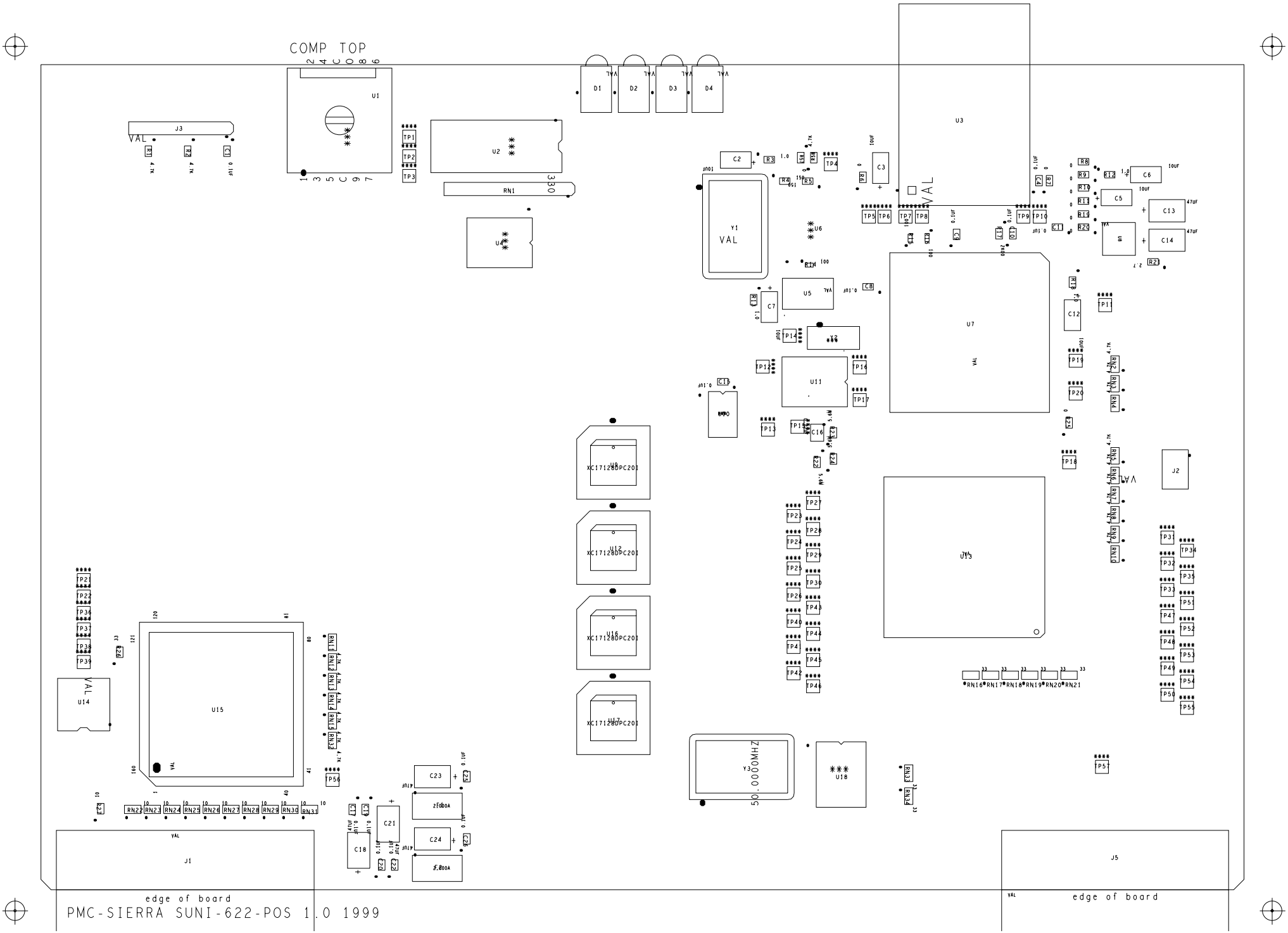


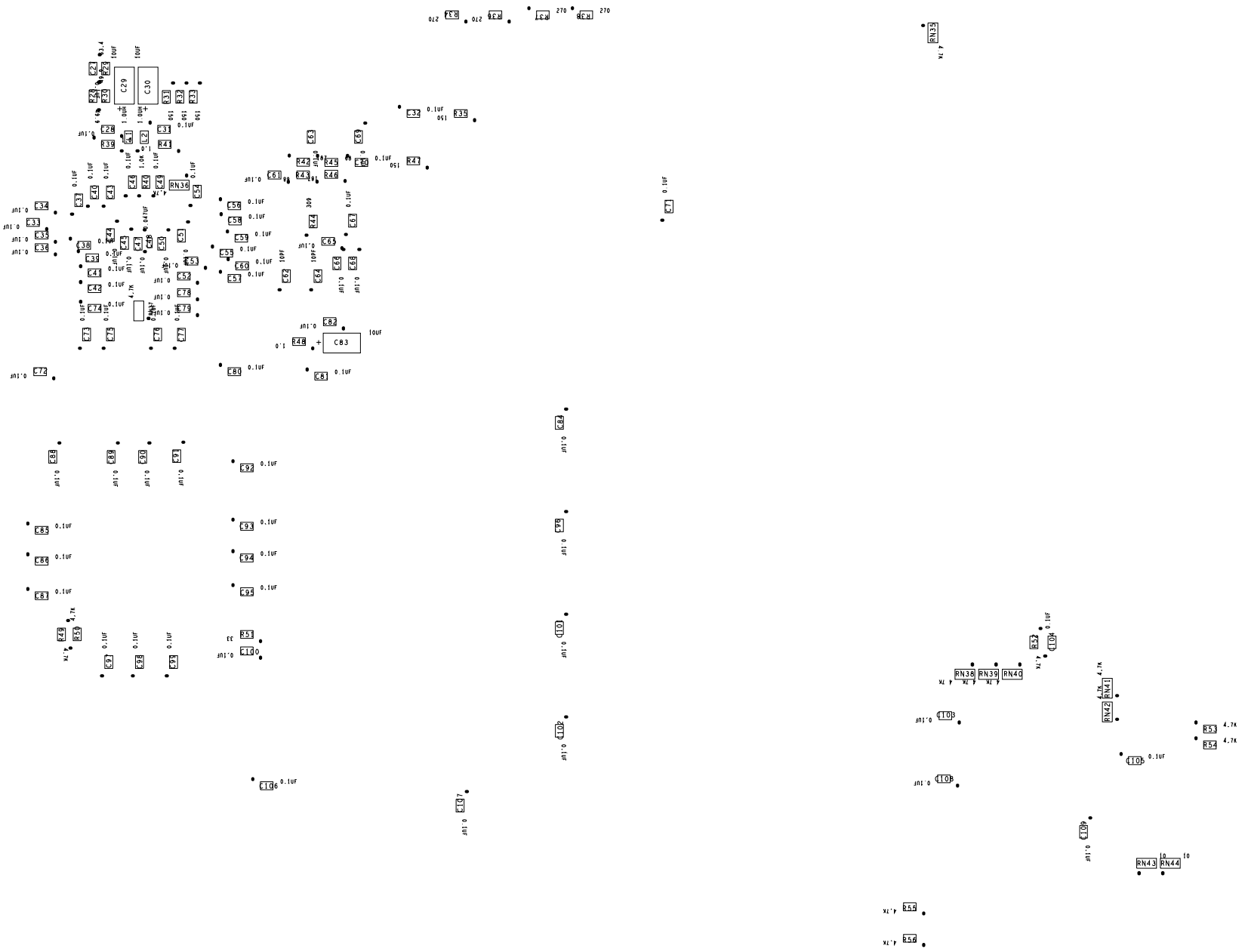
PMC-SIERRA SUNI-622-POS 1.0 1999

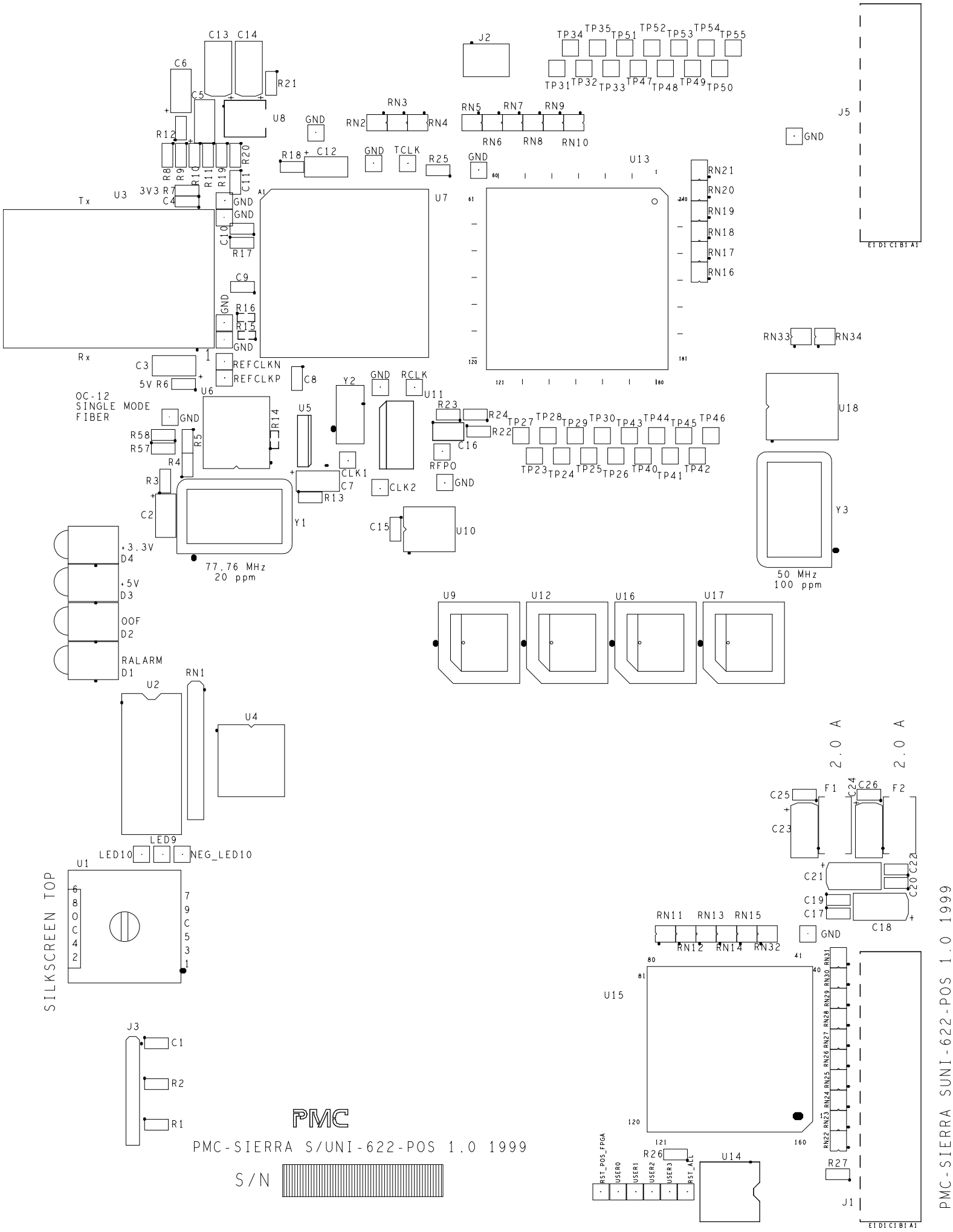
BOTTOM LAYER



PMC-SIERRA SUNI-622-POS 1.0 1999


COMP TOP
edge of board
PMC-SIERRA SUNI-622-POS 1.0 1999
edge of board




C13 C14
C6
C5
R21
U8
R12
R8 R9 R10 R11 R19 R20
C11
3V3 R7
C4
U3
Tx
Rx
GND
C10
R17
C9
R16
R15
C3
5V R6
OC-12
SINGLE MODE
FIBER
R58
R57
R5
R4
R3
C2
U6
R14
U5
Y1
77.76 MHz
20 ppm
+3.3V
D4
+5V
D3
OOF
D2
RALARM
D1
U2
RN1
U4
LED9
LED10
NEG_LED10
U1
SILKSCREEN TOP
J3
C1
R2
R1
J2
RN3
RN2
RN4
R18
C12
TCLK
R25
RN5 RN7 RN9
RN6 RN8 RN10
U7
REFCLKN
REFCLKP
C8
Y2
RCLK
U11
CLK1
C7
R13
CLK2
C15
U10
R23
R24
R22
C16
RFPO
TP34 TP35 TP51 TP52 TP53 TP54 TP55
TP31 TP32 TP33 TP47 TP48 TP49 TP50
TP27 TP28 TP29 TP30 TP43 TP44 TP45 TP46
TP23 TP24 TP25 TP26 TP40 TP41 TP42
U13
RN21
RN20
RN19
RN18
RN17
RN16
J5
E1 D1 C1 B1 A1
RN33
RN34
U18
Y3
50 MHz
100 ppm
U9
U12
U16
U17
2.0 A
2.0 A
F1
F2
C25
C24
C26
C23
C21
C22
C20
C19
C17
C18
RN11 RN13 RN15
RN12 RN14 RN32
U15
RN31 RN30 RN29 RN28 RN27 RN26 RN25 RN24 RN23 RN22
R26
U14
RST_POS_FPGA
USER0
USER1
USER2
USER3
RST_ACL
R27
J1
PMC
PMC-SIERRA S/UNI-622-POS 1.0 1999
S/N
PMC-SIERRA SUNI-622-POS 1.0 1999


SILKSCREEN BOTTOM
PWC-SIERRA SUNI-622-PQG 0.1 2000
A1 B1 C1 D1 E1
A1 B1 C1 D1 E1
C87 C86 C85 C88 C72 C33 C35 C36 C34
R50 R49
C73 C74 C42 C41 C39 C38 C37 C40 C43 C44 C28 R39 R28 C27 R29
C75 C97 C89 C98 C90 C99 C91 RN37 C45 C47 C48 C50 C46 R40 C49 L1 L2 R30 C29 C30
C76 C77 C79 C78 C52 C53 C51 C54 RN36 C31 R41 R31 R32 R33
C106 C100 R51 C95 C94 C93 C92 C80
C57 C60 C55 C59 C58 C56
C61 R48 C62 R42 C63
C81 C64 R44 R43 C65 R46 R45
C66 C82 C68 C67 C70 C69
C83
R47 C32
C107 R35 R34 R36
C102 C101 C96 C84 R37 R38
C71
R56 R55 RN35
C108 C103 RN38 RN39 RN40 R52 C104
C109 RN42 RN41 C105 RN43 RN44
R54 R53

16 REV 3 BOM (BILL OF MATERIALS)

Part Name - Value	Description	Distributor Info.	Manufacturer	JEDEC Type	Ref Des	Qty
74FCT807_SOIC2-BASE	Ten output low skew clock buffer	PI49FCT3807AS		SOIC20W	U18	1
74HC04_SOIC-123	Hex HC Inverter			SOIC14	U10	1
74HC541, SOIC-HCMOS	Octal HC Buffer	74HC541DW		SOIC20W	U4	1
CAPACITOR-0.047µF, X7R_0805	Ceramic, Class 2, X7R, +/-5% tolerance	NEWARK -- 85F219	AVX-08055C473JATN	603	C48	1
CAPACITOR-0.1µF, 50V, X7R_805	Ceramic			SMDCAP805	C1, C4, C8-C11, C15, C17, C19, C20, C22, C25-C28, C31-C47, C49-C60, C63, 71-C81, C84-C109	65
CAPACITOR-10µF, 10V, TANT TEH	Tantalum	DIGI-KEY -- PCT2106CT-ND		SMDTANCAP_C	C2, C3, C5-C6, C12, C29, C30	7
CAPACITOR-47µF, 10V, TANT TEH	Tantalum	DIGI-KEY -- PCT2476CT-ND		NEC_D	C13, C14, C18, C21, C23, C24	6
FUSE__SMD_SOCKET-2.000A, NANO	2 Amp Fuse	DIGIKEY -- F1224CT-ND		NANO_SMF_SOC KET	F1, F2	2
HEADER1-BASE		DIGI-KEY S1011-36-ND		TST_PT_1	TP4, 7-11, 13,16,18, 19, 56, 57	12
HEADER_3X2_JUMPER-BASE		DIGI-KEY S2012-36-ND		HEADER_3X2	J2	1
HEADER_8_100 MIL-BASE		DIGI-KEY S1011-36-ND		SIP8	J3	1
LED-GREEN, PCB RIGHT ANGLE	LED	DIGI-KEY -- LU20095-ND	DIGI-KEY -- LT1066-ND	LED	D1-D4	4
LED10-RED, 25MA, 2.1V	LED			DIP20_SOCKET	U2	1

Part Name - Value	Description	Distributor Info.	Manufacturer	JEDEC Type	Ref Des	Qty
47uF Tantalum capacitor	47uF, 6.3V, Tantalum	Digikey			C47	
352152-1 ZPACK5X22FH_BSCPI_2MM	CONNECTOR ZPACK cPCI 2MM HM 110 POS. TYPE B WITH GND SHIELD		AMP	ZPACK5X22FH_BSCPCI	J5	
352068-1 ZPACK5X22FH_ASCPCI_2MM	CONNECTOR ZPACK cPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD		AMP	ZPACK5X22FH_ASCPCI	J1	
INDUCTOR-1.0µH, , PANASONIC	1µH SMT choke, less than 1 Ohm Resistance	DIGI-KEY -- PCT1187CT-ND	Panasonic PN# ELJ-FD1R0KF	SMDRES805	L1, L2	2
LT1129CST_SOT-3.3V	Low Drop out 3.3V Linear Voltage Regulator	LT1129CST-3.3	Linear Technology, LT1129-3.3	SOT223-3	U8	1
8-pin dip socket	Serial EEPROM for PLX chip			DIP8_SOCKET	U12	1
NM93CS46EN	1-Kbit Serial EEPROM OTP	NM93CS46EN	National (Fairchild) Semiconductor M93CS46.html, National PN#NM93CS46EN	8 pin dip	U12	1
OSC_PECL_-77.76MHZ, 20 PPM	77.7600 MHz Crystal Oscillator 20 PPM, PECL differential outputs. Low output jitter and fast rise/fall times	http://www.conwin.com/cgi-bin/psearch.cgi?type=Clock&family=PECL	5V type, Saronix 99T27M or type, Connor Winfield EH13-541 or 3.3V type from Connor Winfield EH14-541	CRYS14	Y1	1
OSC_TTL_DIP-50.0000MHZ, 100 PPMA	Oscillator, 50.00 MHz 100 PPM, 3.3V, TTL output	DIGI-KEY -- CTX176-ND	CTS Reeves PN# MXO45HS-50.0000	CRYS14	Y3	1
PCI9050_PQFP-BASE	cPCI Bus Interface Chip	PCI9050-1	PLX PN# PCI9050-1	PQFP160	U13	1
RESISTOR-0, 5%, 603	0 ohm SMT resistor			603	R6, R7	2

Part Name - Value	Description	Distributor Info.	Manufacturer	JEDEC Type	Ref Des	Qty
10µF X5R ceramic capacitors	Taiyo Yuden of 1930 North Thoreau, Drive, Suite 190 , Schaumburg IL, 60173 USA, 1-80036-TAIYO			0805		
RESISTOR-0, 5%, 805		DIGI-KEY -- P<VALUE>ACT-ND	DIGI-KEY -- P10ACT-ND DIGI-KEY -- P<VALUE>GCT-ND	SMDRES805	R9-R12, R23, R24, R29	7
RESISTOR-1.0, 5%, 805				SMDRES805	R3, R17, R22, R39, R41	5
RESISTOR-1.0K, 5%, 805				SMDRES805	R40	1
RESISTOR-10, 5%, 805				SMDRES805	R31	1
RESISTOR-100, 5%, 603				603	R18-R20	3
RESISTOR-150, 5%, 805		DIGI-KEY --	DIGI-KEY --	SMDRES805	R35-R38, R47	5
RESISTOR-2.7, 5%, 805		DIGI-KEY --		SMDRES805	R25	1
RESISTOR-270, 5%, 805		DIGI-KEY --		SMDRES805	R8, R14-R16	4
RESISTOR-2K00, 1%, 805		DIGI-KEY --		SMDRES805	R21	1
RESISTOR-33, 5%, 805		DIGI-KEY --		SMDRES805	R30, R51	2
RESISTOR-4.7K, 5%, 805		DIGI-KEY --		SMDRES805	R1, R2, R49, R50, R52-R56	9
RESISTOR-49.9, 1%, 805		DIGI-KEY --		SMDRES805	R32, R34	2
RESISTOR-63.4, 1%, 805		DIGI-KEY --		SMDRES805	R33	1
RES_ARRAY_4_SMD-10		DIGI-KEY --		RN4	RN14-R23, 34, 35	12
RES_ARRAY_4_SMD-33		DIGI-KEY -- Y4<VALUE CODE>-ND		RN4	RN9-11, 36-40	8

Part Name - Value	Description	Distributor Info.	Manufacturer	JEDEC Type	Ref Des	Qty
RES_ARRAY_4_SMD-4.7K		DIGI-KEY --		RN4	RN2-8, 12, 13, 24-33, 41-44	23
R_SIP9-330	330 ohm sip, 9 position			SIP10	RN1	1
SUNI622POS_SBGA-BASE	PM5357 S/UNI-622-POS packet/ATM framer or PM5356 S/UNI-622-MAX ATM framer		PMC-Sierra Inc.	SBGA_304	U7	1
THUMB_WHEEL_SW-COMMON CW, C&K		DIGIKEY -- CKN6000-ND	C & K Components Inc. PN#3M120	CNK3M12	U1	1
TST_PT-BASE		DIGI-KEY S1011-36-ND		TST_PT_1	TP27-TP55	29
TST_PT-BASE	LED10	DIGI-KEY S1011-36-ND		TST_PT_1	TP1	1
TST_PT-BASE	LED9	DIGI-KEY S1011-36-ND		TST_PT_1	TP2	1
TST_PT-BASE	NEG_LED10	DIGI-KEY S1011-36-ND		TST_PT_1	TP3	1
TST_PT-BASE	RCLK	DIGI-KEY S1011-36-ND		TST_PT_1	TP17	1
TST_PT-BASE	REFCLKN	DIGI-KEY S1011-36-ND		TST_PT_1	TP6	1
TST_PT-BASE	REFCLKP	DIGI-KEY S1011-36-ND		TST_PT_1	TP5	1
TST_PT-BASE	RFPO	DIGI-KEY S1011-36-ND		TST_PT_1	TP15	1
TST_PT-BASE	RST_POS_FP GA	DIGI-KEY S1011-36-ND		TST_PT_1	TP21	1
TST_PT-BASE	R_A	DIGI-KEY S1011-36-ND		TST_PT_1	TP26	1
TST_PT-BASE	TCLK	DIGI-KEY S1011-36-ND		TST_PT_1	TP20	1
TST_PT-BASE	UR0	DIGI-KEY S1011-36-ND		TST_PT_1	TP22	1
TST_PT-BASE	UR1	DIGI-KEY S1011-36-ND		TST_PT_1	TP23	1
TST_PT-BASE	UR2	DIGI-KEY S1011-36-ND		TST_PT_1	TP24	1

Part Name - Value	Description	Distributor Info.	Manufacturer	JEDEC Type	Ref Des	Qty
TST_PT-BASE	UR3	DIGI-KEY S1011-36-ND		TST_PT_1	TP25	1
20 pin PLCC	20 Pin PLCC socket	Digikey PN# ED80007-ND	Mill-Max PN# 540-99-020-17-400-X00X,	PLCC20_SOCKET	U9, U12, U16, U17	4
V23826-H18-C363-3.3V	OC-12 ODL, single or Mulitmode fiber, SONET/SDH	Insight Components Inc., Richmond, BC, Canada	HP Co. ODL, HFBR-5208- 5v, mulitmode,HFCT-5208B-5v, single-mode, or Siemens V23826-H18-C363, 3.3V, single-mode.	LCD-PMD-SOCKET	U3	1
XC1701L_PC20C EEPROM	Serial EEPROM OTP, 832,528 bits			PLCC20	U9, U12, U16, U17	4
XC4036XLA_HQ240_HQFP -9NS	FPGA	XC4036XLA-09HQ240		HQ240	U13	1

17 FPGA ATM LOOPBACK SOURCE VHDL CODE

```
library IEEE;
use IEEE.std_logic_1164.all;

entity ATM_Loopback_latched is
    port (
        TCA: in STD_LOGIC;
        RCA: in STD_LOGIC;
        RDAT: in STD_LOGIC_VECTOR (15 downto 0);
        TDAT: out STD_LOGIC_VECTOR (15 downto 0);
        RENB: out STD_LOGIC;
        TENB: out STD_LOGIC;
        RSOC: in STD_LOGIC;
        TSOC: out STD_LOGIC;
        TFCLK: in STD_LOGIC;
        RFCLK: in STD_LOGIC;
      RESETB: in STD_LOGIC;
      LED: out STD_LOGIC_VECTOR(6 downto 0);
      ALE: in STD_LOGIC;
      LBEB: in STD_LOGIC_VECTOR(1 downto 0);
      LAD: inout STD_LOGIC_VECTOR(1 downto 0);
      BAD: inout STD_LOGIC_VECTOR(1 downto 0);
      WRB: in STD_LOGIC;
      RDB: in STD_LOGIC
--    FPGA_BAD: out STD_LOGIC_VECTOR(10 downto 0);
--    FPGA_WRB: out STD_LOGIC;
--    FPGA_RDB: out STD_LOGIC;
--    FPGA_ALE: out STD_LOGIC
    );
end ATM_Loopback_latched;

architecture ATM_Loopback_arch of ATM_Loopback_latched is

      signal      RENB_D        :   STD_LOGIC;
      signal      RENB_Q        :   STD_LOGIC;
      signal      ENB_D1_D2 : STD_LOGIC;

begin
        RENB_D <= TCA NAND RCA;
        RENB <= RENB_Q;
        LED <= "0000000";
--      FPGA_BAD <= "ZZZZZZZZZZZ";
--      FPGA_WRB <= 'Z';
--      FPGA_RDB <= 'Z';
--      FPGA_ALE <= 'Z';

-- Latch RENB
-- D Flip Flop with Asynchronous Reset
--      TFCLK: in STD_LOGIC;
--      RESETB: in STD_LOGIC;
--      RENB_D: in STD_LOGIC;
--      RENB_Q: out STD_LOGIC;
process (RFCLK, RESETB)
begin
   if RESETB='0' then   --asynchronous RESET active Low
```

```
      RENB_Q <= '1';
   elsif (TFCLK'event and TFCLK='1') then  --TFCLK rising edge
      RENB_Q <= RENB_D;
   end if;
end process;

-- First latch for TENB
-- D Flip Flop with Asynchronous Reset
--      TFCLK: in STD_LOGIC;
--      RESETB: in STD_LOGIC;
--      RENB_Q: in STD_LOGIC;
--      ENB_D1_D2: out STD_LOGIC;
process (TFCLK, RESETB)
begin
   if RESETB='0' then   --asynchronous RESET active Low
      ENB_D1_D2 <= '1';
   elsif (TFCLK'event and TFCLK='1') then  --TFCLK rising edge
      ENB_D1_D2 <= RENB_Q;
   end if;
end process;

-- Second latch for TENB
-- D Flip Flop with Asynchronous Reset
--      TFCLK: in STD_LOGIC;
--      RESETB: in STD_LOGIC;
--      ENB_D1_D2: in STD_LOGIC;
--      TENB: out STD_LOGIC;
process (TFCLK, RESETB)
begin
   if RESETB='0' then   --asynchronous RESET active Low
      TENB <= '1';
   elsif (TFCLK'event and TFCLK='1') then  --TFCLK rising edge
      TENB <= ENB_D1_D2;
   end if;
end process;

-- Register for TDAT
-- Register
--      TFCLK: in STD_LOGIC;
--      RESETB: in STD_LOGIC;
--      RDAT: in STD_LOGIC;
--      TDAT: out STD_LOGIC;
process (TFCLK, RESETB)
begin
   if RESETB='0' then   --RESET active Low
      TDAT <= "0000000000000000";
   elsif (TFCLK'event and TFCLK='1') then  --TFCLK rising edge
      TDAT <= RDAT;
   end if;
end process;

-- D-flip flop for TSOC
-- D-flip flop with asynchronous RESET
--      TFCLK: in STD_LOGIC;
--      RESETB: in STD_LOGIC;
--      RENB_Q: in STD_LOGIC;
--      RSOC: in STD_LOGIC;
```

```
--      TSOC: out STD_LOGIC;
process (TFCLK, RESETB)
begin
   if RESETB='0' then   --asynchronous RESET active Low
      TSOC <= '0';
   elsif (TFCLK'event and TFCLK='1') then  --TFCLK rising edge
      TSOC <= RSOC;
   end if;
end process;
end ATM_Loopback_arch;
```

NOTES

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