PM4388

CABGA TOCTL WITH FREEDM-32

REFERENCE DESIGN

PRELIMINARY INFORMATION

ISSUE 1: SEPT 1998

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	Sept 1998	Document created.

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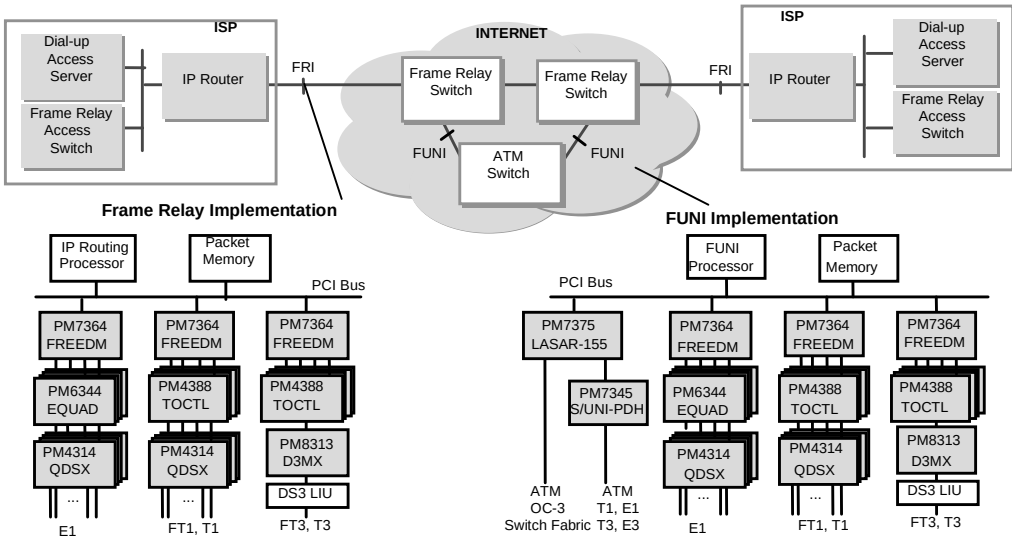
1 OVERVIEW

1.1 Application Perspective

Frame relay is a multiplexed data networking technology supporting connectivity between user equipment (routers, nodal processors/fast packet switches) and between user equipment and the public frame relay network. The frame relay protocol supports data transmission over a connection-oriented path and enables the transmission of variable-length data units over an assigned virtual connection.

Frame relay technology can be used in LAN interconnection, Internet access and Internet backbones using link speeds ranging from 9600 baud to the DS3 rate. Figure 1 illustrates a typical implementation of a frame relay interface (FRI) and a frame relay user to network interface (FUNI) using fractional T1 (FT1), T1, E1 and DS3 rates. Other line options such as J2 and SONET virtual tributary (VT) mapping are not shown in the illustration.

Figure 1 - Frame Relay Inter-networking Overview



User equipment such as routers, T1 multiplexers, front end processors (FEPs), and packet assemblers/dissemblers (PADS) need to support the frame relay interface in order for them to be connected to a private or a public frame relay network.

1.2 Objectives

The purpose of the "CABGA TOCTL with FREEDM-32" reference design is to serve as an example to assist designers of routers and frame relay switches to design their products using PMC-Sierra's FREEDM-32, TOCTL and D3MX standard products.

This design illustrates the frame relay application with an interface to a channelized T3 data stream. The hardware which implements this interface is built, tested and debugged thereby assisting designers to more quickly bring their designs to market.

1.3 Design Constraints

The following hardware constraints have been included in this design:

- Support the PCI local bus revision 2.1, which allows up to four PCI devices per PCI bus segment to be connected to a host processor and packet memory. This constraint allows the reference design to be implemented as an add-in card to any readily available processor board with a revision 2.1 compliant PCI bus. Up to four reference design cards can be interfaced to the processor board.

- Mechanical and electrical constraints for interfacing an add-in card to the processor board, as specified in revision 2.1 of the PCI local bus specification.

The software interfaces to the FREEDM-32 via a host processor on the PCI bus and enables support of network protocol layers necessary to transmit and receive data packets of a PVC. Software procedures are provided to illustrate the following:

- PCI device location and memory resource assignment

- Reset of the hardware via software

- Initialization of the hardware, software and the packet memory

- Activation/deactivation of the hardware

- Provisioning/unprovisioning of PVCs

- Transmit and receive packet processing

- Error handling
- Performance counters
- Diagnostics

The following software constraints have been included in this design:

- The FREEDM-32 data interfaces are the only interfaces the software has access to. The content of the user data field of the HDLC frame is not processed. Other upper layer functions such as congestion management, LMI protocol and multi-cast capability are not implemented.
- Source code is written in the C language and developed using the VxWorks Tornado development environment. Executable code can run on i960 or Pentium based processor boards.

1.4 References

[1] PMC-960840, PMC-Sierra, “TOCTL Octal T1 Framer” Standard Product Datasheet, December, 1997, Issue 4
[2] PMC-920702 PMC-Sierra, “D3MX M13 Multiplexer” Standard Product Datasheet, July, 1998, Issue 5
[3] PMC-960113, PMC-Sierra, "Frame Relay Protocol Engine and Datalink Manager" Standard Product Datasheet, December, 1996, Issue 2
[4] PCI SIG, PCI Local Bus Specification, June 1, 1995, Version 2.1
[5] PCI Compact Specification, PCI Industrial Computers Manufacturers Group, 1995, Version 1.0
[6] PMC-970280, PMC-Sierra, "FREEDM-32 Software Reference Design" Application Note, March, 1997, Issue 1
[7] PMC-961061, PMC-Sierra, "FREEDM-32 PCI Bus Utilization and Latency Analysis" Application Note, February, 1997, Issue 1
[8] PMC-970281, PMC-Sierra, "FREEDM-32 Programmer's Guide" Application Note, March, 1997, Issue 1
[9] PMC-970959 PMC-Sierra, “MC68340 Software for the “FREEDM with TOCTL” Reference Design

2 FEATURE OVERVIEW

This reference design provides the following features:

- Frame relay processing of up to 128 logical channels associated with T1 or channelized T1 data streams. A logical channel can be composed of an unchannelized data stream, or a number of time-slots within a channelized data stream.
- Interfaces to a host processor and packet memory via the PCI local bus.
- Interface to one T3 link carrying channelized data.
- Includes a M13 Multiplexer to provide 28 T1 data streams from a T3 link.
- Includes a T1 framer for each of the 28 T1 data streams.

3 FUNCTIONAL DESCRIPTION

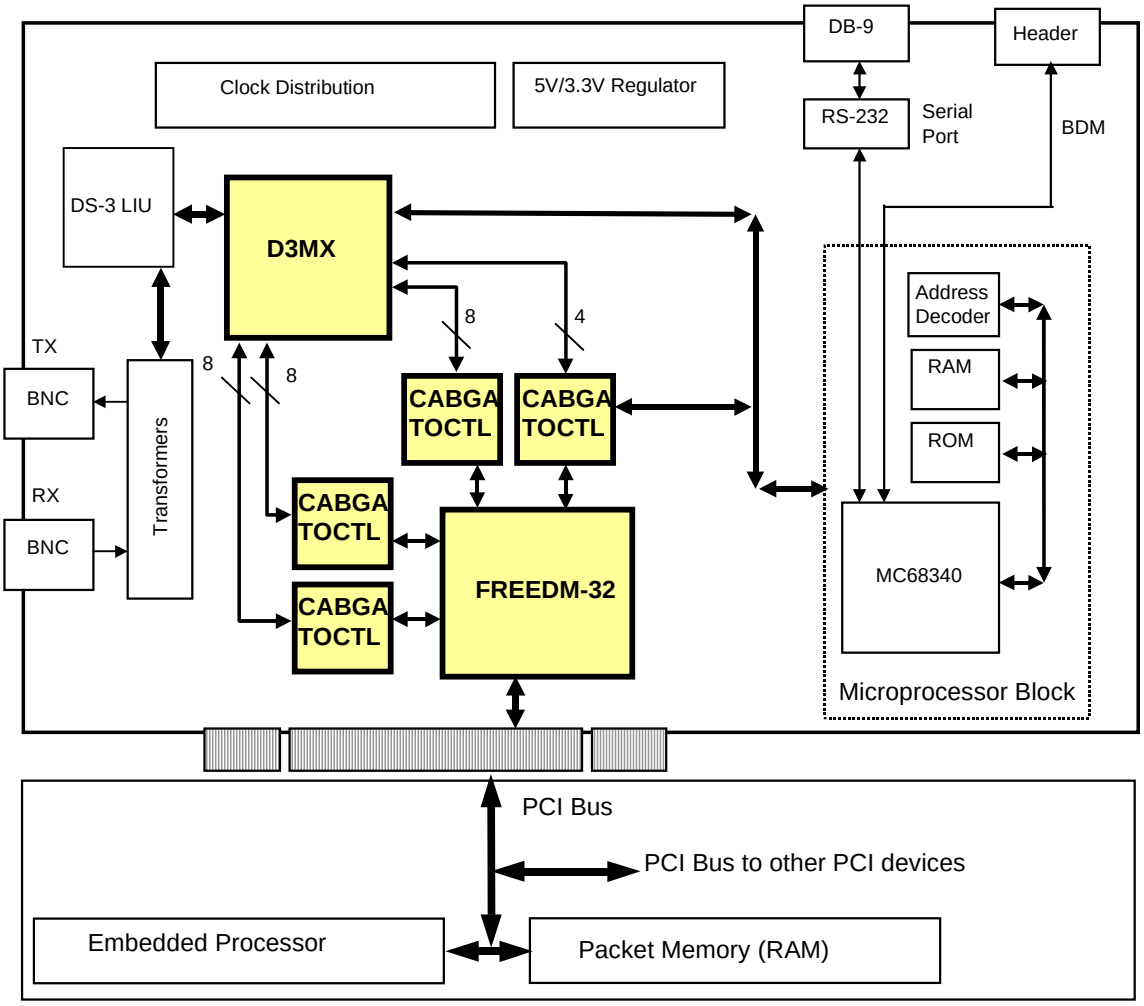
3.1 Reference Design Card

The CABGA TOCTL with FREEDM-32 reference design card is an add-in card that connects the FREEDM-32 to a host processor and packet memory. The host processor may function as an IP routing processor, which serves to route packets among FREEDM-32 channels of the same reference design card, and/or FREEDM-32 channels of different reference design cards. A block diagram showing the reference design card is shown in figure 2.

The frame relay packets from a remote node are available at the channelized T3 interface. The channelized T3 interface connectors provide 28 T1 data streams multiplexed via the D3MX. The remaining four serial ports of the FREEDM-32 are unused.

The on-board microprocessor has a serial port, which enables control and monitoring of the T1 framers and the M13 multiplexer. The serial port can be interfaced to the motherboard, or attached to a terminal.

Figure 2 - Reference Design Card Block Diagram



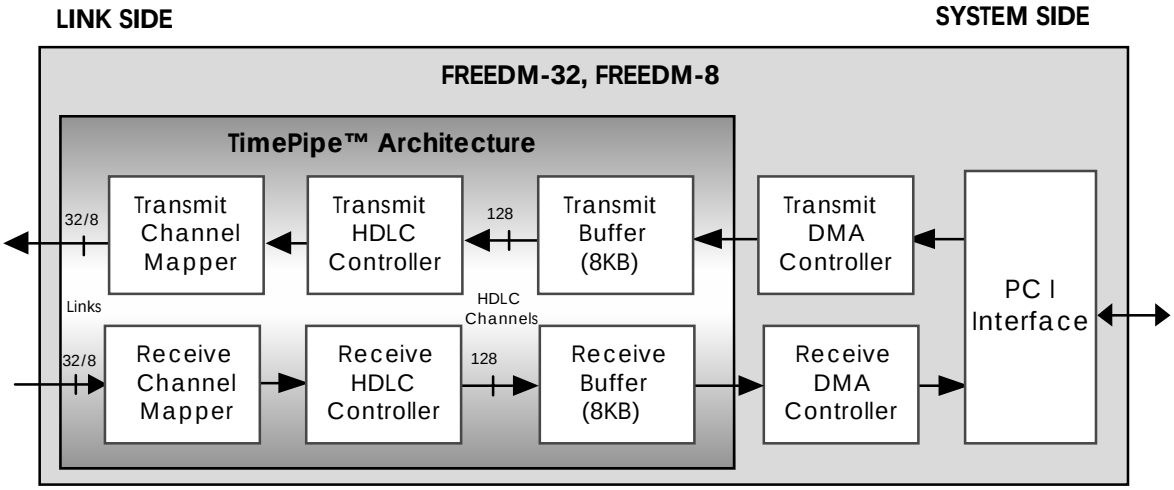
3.2 Frame Relay Protocol Engine and Datalink Manager

The **FR**ame **E**ngin**E** and **D**ata Link **M**anager (FREEDM) is a family of advanced data link layer processors that is ideal for applications such as Internet access equipment, frame relay switches, ATM switches, packet-based CDMA base station controllers and Digital Subscriber Loop Access multiplexers (DSLAM).

The cornerstone of the FREEDM product family is the revolutionary TimePipe™ architecture (as shown in Figure 3). The TimePipe architecture enables a single FREEDM device to support up to 32 physical links, 128 HDLC channels and 8 KB of integral packet buffer in each of the transmit and receive direction. Each one of the 32 physical links can be independently timed from 56 Kbit/s to 52 Mbit/s. This unparalleled level of integration not only simplifies networking

equipment designs, but also enables a new generation of line card designs that can use a common data link layer processor for a wide variety of line rates ranging from T1, E1, E3, T3 to HSSI.

Figure 3 - FREEDM Block Diagram and the TimePipe Architecture



Power is useful only if it can be directed to perform the intended work. The TimePipe architecture is not only powerful but also highly configurable as well. A flexible channel mapper mechanism is provided such that any link can be assigned to any HDLC channel in software. In the case of a channelized application, data carried on one or more time-slots within the same link can be grouped and assigned to a single HDLC channel.

The 8KB packet buffer can be flexibly allocated to active HDLC channels. The 8KB buffer is organized as 512 blocks of 16 byte FIFOs. The number of blocks assigned to any HDLC channel is configurable in software.

In the receive direction, the Receive HDLC Controller performs flag delineation, bit destuffing, CRC verification using either CRC-32 or CRC-CCITT algorithm and length checking. In the transmit direction, the Transmit HDLC Controller performs flag insertion, bit stuffing and CRC calculation using either CRC-32 or CRC-CCITT algorithm.

On the system side, FREEDM provides a 33 MHz, 32 bit PCI 2.1 compliant bus interface. Two efficient transmit and receive DMA controllers are provided to support burst data transfers across the PCI bus.

The following documents should be consulted for further information on the operation and interfaces of the FREEDM-32:

- FREEDM-32 Long form Datasheet [3]
- FREEDM-32 Programmer's Guide [8]
- FREEDM-32 PCI Bus Utilization and Latency Analysis [7]

3.3 PCI Bus Interface to the Host Processor and Packet Memory

The FREEDM-32 is configured, controlled and monitored across the PCI bus interface by a host processor and packet memory (RAM). In some configurations, there may be multiple reference design cards on the PCI bus, and during a bus transaction, one of the FREEDM-32 devices may act as the bus master in accessing the packet memory, or the host processor may act as the bus master in accessing one of the FREEDM-32 registers of a reference design card.

Figure 4 shows an address map for a PCI bus, which shows one FREEDM-32 device. The data structures shown are required to interface one FREEDM-32 to the PCI bus. In this figure, PCI addresses are 32-bit physical addresses, which can be observed at the address pins of the PCI bus interface.

When multiple FREEDM-32's are attached to the bus each FREEDM-32 must have a unique set of the following data structures.

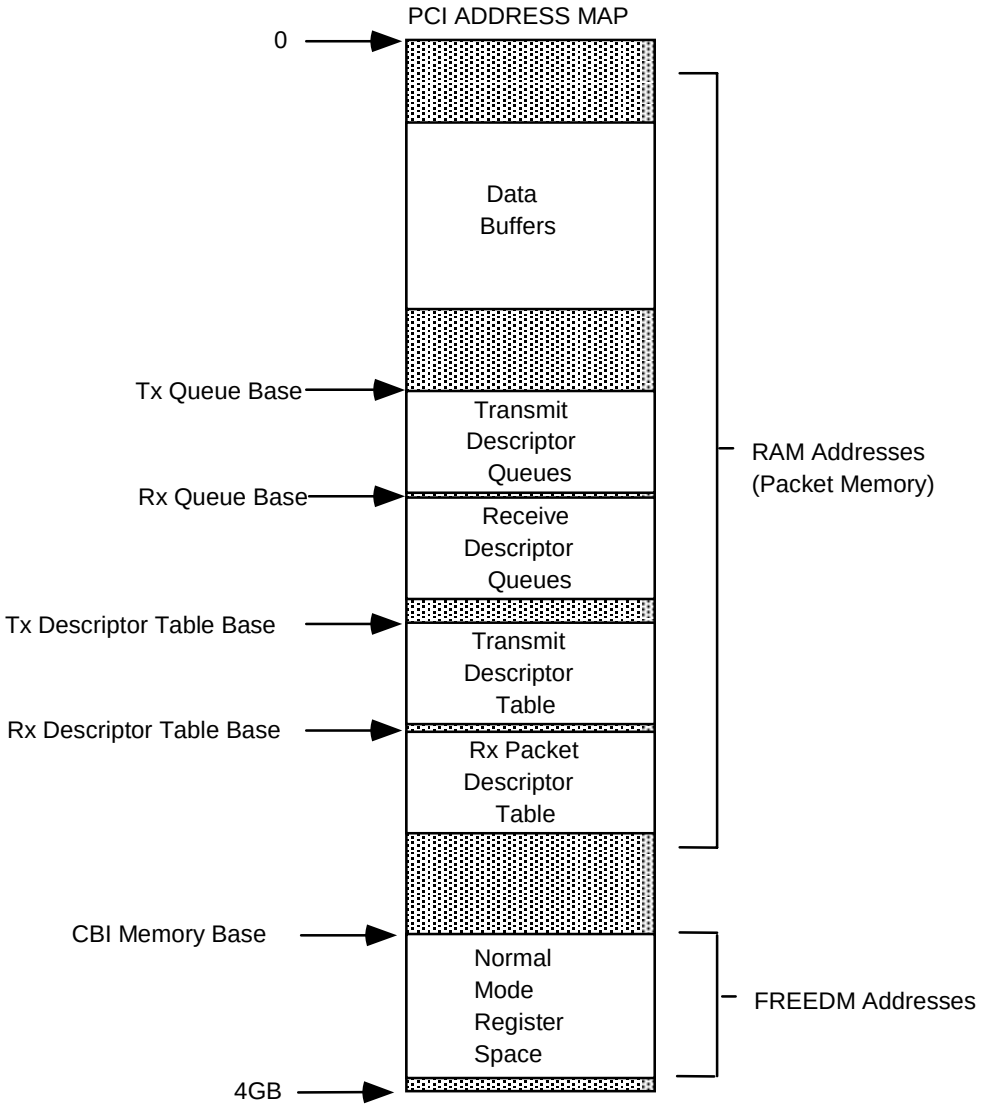
- Transmit Descriptor Table
- Receive Descriptor Table
- Transmit Queue Space
- Receive Queue Space
- Normal Mode Register Space

The data structures within packet memory are accessed by software running on the host processor, or by the FREEDM-32. The software specifies the location of these data structures by writing base addresses into the appropriate FREEDM-32 registers, before activating the FREEDM-32.

The data Buffers are filled with the data received by the FREEDM-32, or contain transmit data, which is read by the FREEDM-32. The descriptor tables and the queues are required to manage these buffers.

The Normal Mode Register space is accessed by the software running on the host processor to manage and control operation of a FREEDM-32 device. This register space is located in the FREEDM-32 and is mapped into the PCI address space by the software running on the host processor during the boot-up sequence.

Figure 4 - PCI Address Map



The PCI Configuration Space does not reside in the PCI address map, but it is a requirement for all PCI devices. The Configuration Space is a block of 256 contiguous bytes that reside in the PCI device (the FREEDM-32 in this case), and is accessed by the host processor in a PCI bus Configuration Read (or

Write) transaction, rather than a Memory Read (or Write) transaction. Access to this configuration space is system specific and a thorough discussion of it can be found in the PCI specification [4].

A description of the software running on the host processor can be found in the document "FREEDM-32 Software Reference Design" [6].

3.4 T1 Octal Framers

T1 framing for the 32 T1 data streams is provided via four PM4388 **T**1 **OCT**a**L** framers (TOCTL). The TOCTL is a feature-rich device for use primarily in systems carrying data over DS1 facilities. Each of the eight framers within a TOCTL is independently software configurable, allowing feature selection without changes to external wiring.

On the receive side, each of eight independent framers can be configured to frame to either of the common DS1 signal formats: (SF, ESF) or to be bypassed (unframed mode). The TOCTL detects and indicates the presence of YELLOW and AIS patterns and also integrates YELLOW, RED, and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, out-of-frame events, and changes of frame alignment is provided. The TOCTL also detects the presence of in-band loopback codes, ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link. The HDLC messages are terminated in a 128 byte FIFO. An elastic store that optionally supports slip buffering and adaptation to back plane timing is provided, as is a signaling extractor that supports signaling de-bounce, signaling freezing and interrupt on signaling state change on a per-DS0 basis. The TOCTL also supports idle code substitution and detection, digital milliwatt code insertion, data extraction, trunk conditioning, data sign and magnitude inversion, and pattern generation or detection on a per-DS0 basis.

On the transmit side, the TOCTL generates framing for SF or ESF DS1 formats, or framing can be optionally disabled. The TOCTL supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion, zero-code suppression, and pattern generation or detection on a per-DS0 basis.

The TOCTL can also generate in-band loopback codes, ESF bit oriented codes, and transmit HDLC messages on the ESF data link. The HDLC messages are generated from a 128 byte FIFO.

The TOCTL can generate a low jitter transmit clock, and also provides jitter attenuation in the receive path.

It should be noted that the TOCTL device operates on unipolar data only: B8ZS substitution and line code violation monitoring, if required, must be processed by the T1 LIU, in this case the QDSX.

Further information on the TOCTL can be found in the long form datasheet [1].

Note: The TOCTL is not necessarily a replacement for two PM4344 TQUAD devices because the TOCTL is optimized for data applications. No additional glue logic is required to interface TOCTL's to the FREEDM-32 and so, we recommended that the TOCTL, not the TQUAD, be used with the FREEDM-32.

3.5 T3 Line Interface

The T3 line interface is provided by the TDK 78P7200 line interface transceiver IC, along with transformers and a few passive components.

The receiver has a very wide dynamic range and accepts B3ZS-encoded bipolar inputs; it provides CMOS logic level clock, positive and negative data and low-level signal detect outputs. An on-chip equalizer improves the intersymbol interference tolerance on the receive path.

The transmitter converts CMOS logic level clock, positive and negative data input signals into a bipolar signal with the appropriate pulse shape for T3 transmission.

3.6 M13 Multiplex

The M13 multiplex function is provided by the PM8313 D3MX M13 Multiplexer. It is configured in this design to support asynchronous multiplexing and demultiplexing of 28 DS1s into a DS3 signal.

Receive DS3 framing is provided by the DS3 FRMR Framer Block. The FRMR accepts either a B3ZS encoded bipolar, or a unipolar signal compatible with M23 and C-bit parity applications. The FRMR frames to a DS3 signal with a maximum average reframe time of 1.5 ms in the presence of a 10^{-3} bit error rate. The FRMR indicates line code violations, loss of signal, framing bit errors, parity errors, C-bit parity errors, and far end block errors (FEBE). The FRMR detects far end receive failure (X-bits set to 0), the alarm indication signal (AIS), and the idle signal. The FRMR is an off-line framer, indicating both out of frame (OOF) and change of frame alignment (COFA) events. The error events (FER, CBIT PARITY ERROR, FEBE, etc.) are still indicated while the framer is OOF, based on the previous frame alignment.

The C-bit parity far end alarm channel (FEAC) and path maintenance data link are supported. Bit oriented codes in the FEAC channel are detected by the

RBOC Bit-Oriented Code Receiver Block. If enabled, the RBOC generates an interrupt when a valid code has been received. The path maintenance data link is terminated using either the RFDL Data Link Receiver Block or an external HDLC receiver. The RFDL supports polled, interrupt driven, and DMA servicing.

DS3 error event accumulation is provided by the DS3 PMON Performance Monitor Block. The PMON accumulates framing bit errors, line code violations, excessive zeros occurrences, parity errors, C-bit parity errors, and far end block errors. Error accumulation continues even while the off-line framer is indicating OOF. The counters should be polled once per second, and are sized so as not to saturate at a 10^{-3} bit error rate. Transfer of count values to holding registers is initiated through the microprocessor interface.

DS3 transmit framing insertion is provided by the DS3 TRAN Transmitter Block. It outputs either a B3ZS encoded bipolar signal, or a unipolar signal. The DS3 TRAN inserts the X, P, M, C, and F bits into the outgoing DS3 stream. The DS3 TRAN block inserts far end receive failure, AIS, and the idle signal under the control of external inputs, or internal register bits. Diagnostic features are provided to allow the generation of line code violation error events, parity error events, framing bit error events, and when enabled for the C-bit parity application, C-bit parity error events, and far end block error events. External inputs allow substitution of the overhead bits or the source of the AIS signal, idle signal or far end receive failure indication.

When configured for the C-bit parity application, bit oriented codes in the FEAC channel are inserted by the XBOC Bit-Oriented Code Transmitter Block. The FEAC code is controlled by an internal register. The path maintenance data link is inserted using the XFDL Data Link Transmitter Block or an external HDLC transmitter. The XFDL supports polled, interrupt driven, and DMA servicing.

The demultiplexing and multiplexing of seven 6312 kbit/s data streams into and out of the DS3 is performed by the MX23 M23 Multiplexer Block. The MX23 contains FIFOs and performs bit stuffing for the rate adaptation of the DS2s. The C-bits are set appropriately, with the option of inserting DS2 loopback requests. The MX23 may be configured to generate an interrupt upon the detection of loopback requests in the received DS3. AIS may be inserted in the any of the 6312 kbit/s tributaries in both directions. C-bit parity is supported by using a 6.3062723 MHz clock, which corresponds to a stuffing ratio of 100%.

Framing to the demultiplexed 6312 kbit/s data streams is provided by the DS2 FRMR Framer. It supports both DS2 (ANSI TI.107) and CCITT Recommendation G.747 frame formats. The maximum average reframe time is 7 ms for DS2 and 1ms for G.747. In DS2 mode, it detects far end receive failure and accumulates M-bit and F-bit errors. In G.747 mode, it detects remote alarm and accumulates

framing word errors and parity errors. The DS2 FRMR is an off-line framer, indication both OOF and COFA events. Error events (FERF, MERR, FERR, PERR, RAI, framing word errors) are still indicated while the DS2 framer is indicating OOF, based on the previous alignment.

The multiplexing and demultiplexing of the low speed tributaries into and out of a 6312 Kbit/s data stream is performed by seven MX12 M12 Multiplexers. Each of the MX12 blocks may be independently configured to multiplex and demultiplex four 1544 Kbit/s DS1s into and out of a DS2 formatted signal or to multiplex and demultiplex three 2048 Kbit/s signals into and out of a G.747 formatted signal. Each MX12 may be independently bypassed so an external DS2 may by multiplexed and demultiplexed directly into and out of the DS3. The MX12 contains FIFOs and performs bit stuffing to accommodate the tributary frequency deviations. The C-bits are set appropriately, with the option of inserting DS1 loopback requests. The MX12 block may be configured to generate an interrupt upon the detection of loopback requests in the received DS2. AIS may be inserted in any of the low speed tributaries in both directions.

Further information on the D3MX can be found in the long form datasheet [2].

3.7 On-board Microprocessor

The Motorola 68340 is used to monitor and control the TOCTL and D3MX devices. It provides the following features:

- 16-bit data bus
- Interrupt controller
- Address decoder
- Timer
- Serial interface

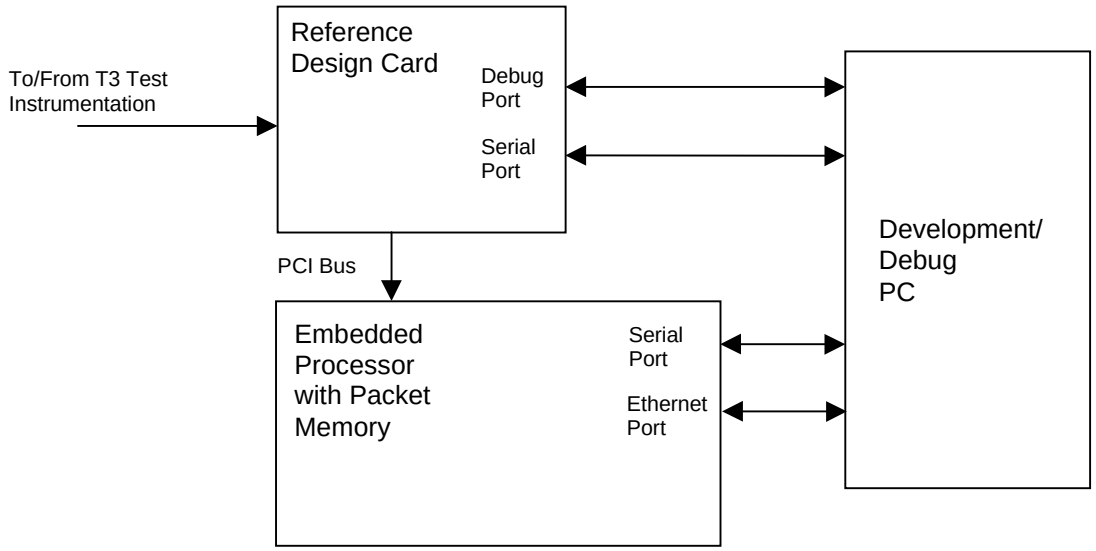
The 68340 is commonly used in many host applications. Its main advantage is that it requires a very small number of external components to be operational. The components include clock circuitry, RAM, ROM, and a serial interface (RS232). It also has an abundance of third-party software support, such as real-time operating systems and C-compilers. In addition, the 68340, has a built-in background debug function, which greatly simplifies the code debugging operation.

4 IMPLEMENTATION DESCRIPTION

4.1 System Testbed Description

The reference design card is connected to the test system as shown in figure 5. The channelized T3 interface is attached to external instrumentation. The instrumentation can source data into the receive link of the reference design card and the data is returned on the transmit link after loopback through the packet memory, or loopback at the line interface.

Figure 5 - System Testbed Block Diagram



Alternatively, the host processor and packet memory can source the transmit data. The diagnostic loopback mode of the devices can be used to loopback the transmit data to the receive path.

The serial port of the reference design card allows the development/debug PC to monitor the status of the TOCTL and D3MX chips. This port is also used to program registers for initialization, software reset and diagnostics.

The debug port of the reference design card allows the development/debug PC to load software and to monitor the status of the software running on the on-board microprocessor. Software can be downloaded through the debug port or provided via the ROM. This port is required during the software development cycle, and is not required for normal operation of the reference design card.

The serial port of the host processor is used to monitor and control the operation of the FREEDM-32 and the host processor via the development/debug PC.

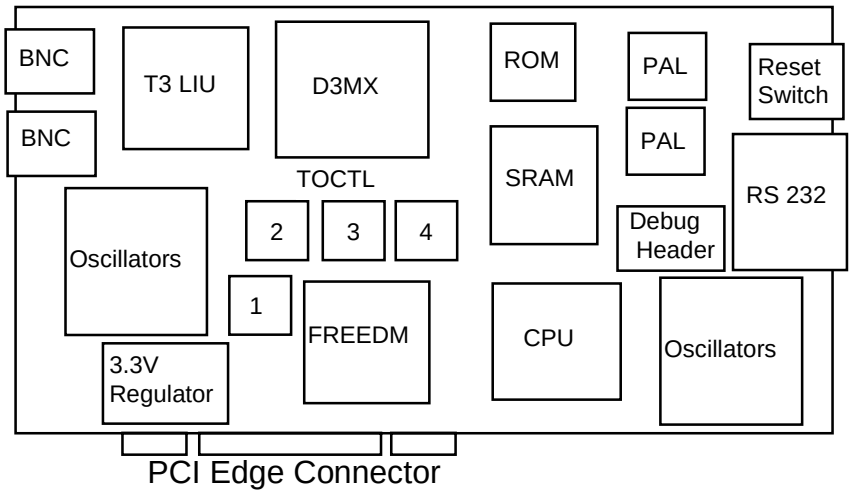
The processor's Ethernet port is provided to download software into the host processor more quickly than can be achieved via the serial port.

4.2 Card Size and Component Placement

The card size conforms to the constraints for a PCI add-in card as specified in the PCI specification.

The card floor plan is shown in figure 6.

Figure 6 - Card Floorplan



4.3 LED Description

There is one LED block, U1, on the reference design card. The LED is used to indicate the status of the D3MX inputs and the status of power on the board. Figure 7 shows the LED and its labels. Table 1 explains the function of each LED.

Figure 7 - LED U1 Description

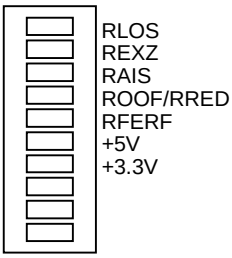


Table 1 - LED U1 Description

Label	Function
RLOS	Receive loss of signal. The LED turns on when the dual rail NRZ format stream is selected and 175 successive zeros are detected on the RPOS and RNEG inputs. The LED turns off when the ones' density is greater than 33% for 175±1 bit periods on the RPOS and RNEG inputs.
REXZ	Receive excessive zero indication. When the presence of 3 or more consecutive zeroes are detected in the receive DS-3 stream, the LED turns on.
RAIS	Receive alarm indication signal. Indicates the presence of AIS in the DS-3 stream.
ROOF/RRED	Receive out-of-frame/receive RED alarm. If the REDO bit in the Master Alarm Enable register is 0, this LED indicates an out-of-frame condition. When REDO bit is set to 1, the LED indicates out-of-frame or DS-3 loss of signal.
RFERF	Receive far end receive failure signal. This LED indicates the value of the internal FERF state.
+5V	This provides indication of the +5V voltage source. The LED is on if +5V power is available.
+3.3V	This provides indication of the +3.3V voltage source. The LED is on if +3.3V power is available.

4.4 Jumper Description

There are two jumpers, J1 and J2, located on the reference design card. J1 selects the timing for the D3MX. J2 selects the Line Buildout (LBO) pulse shaper for the DS-3 line interface.

Timing for the D3MX can be either loop-timed or externally timed. By shorting J1, the recovered DS-3 receive clock is used and the D3MX is loop-timed. If J1 is left open, the on board 44.736MHz crystal oscillator is used to externally clock the D3MX.

The LBO pulse shaper can be configured for transmission over different cable lengths. Shorting pins 1 and 2 of J2, labeled LBO LO, grounds the LBO pin. This is used for applications with cable lengths of 225 feet and longer. Shorting pins 2 and 3 of J2, labeled LBO HIGH, pulls the LBO pin to +5V. This is used for applications with cable lengths shorter than 225 feet.

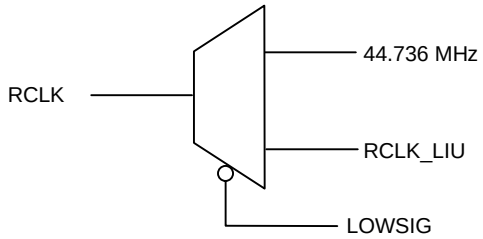
4.5 Timing Distribution

The reference design card employs crystal oscillators to provide stable clock timing for the TOCTL and D3MX.

The TOCTL requires a 37.056 MHz clock at the XCLK/VCLK input. A 1.544 MHz oscillator is used for the CTCLK and CECLK inputs of the TOCTL.

Timing for the D3MX is derived from either the line interface or an external 44.736 MHz oscillator. This is manually selectable. An alternative to using manually selectable timing is to use a multiplexer driven clock. Figure 8 shows an alternate clocking design which automatically switches to external timing when LOWSIG is active.

Figure 8 - RCLK from DS-3 Line Interface



4.6 Transmission Line Impedance Control

A measure of when impedance should be controlled is the transmission electrical length (TEL). When the trace length is greater than ¼ of the TEL, impedance should be controlled. The TEL is the length of transmission line represented by

one rise or fall time. For CMOS technology, the average rise/fall time is 1.5 ns. Electromagnetic energy travels at a velocity of 5.8 inches per ns.

$$TEL = rise\_time * 5.8 \frac{inches}{ns}$$

The TEL for the reference design card is 8.7 inches and ¼ of the TEL is 2.2 inches. The trace layout on the reference design is therefore not critical if all clock and data traces are less than 2.2 inches. However, it is still good engineering practice to keep transmission lines at appropriate impedance and with minimum crosstalk at interfaces.

Sources of impedance mismatches are changes in trace width, trace stubs and power plane discontinuities. Impedance mismatches cause reflections on the line, which may cause overshoot and undershoot malfunctions. By keeping the clock lines on the same signal plane, impedance of the transmission line is not changed. Also, by keeping the routing of the signal to the shortest distance possible, variations in the copper trace are kept to a minimum to reduce the possibility of impedance changes on the line. All critical traces that travel to more than one pin are connected in series to eliminate stubs.

Another method of controlling impedance is the use of termination resistors. Termination resistors absorb the energy travelling on a transmission line. Energy not absorbed appears as reflections.

4.7 Decoupling, Bypassing and Bulk Capacitors

Decoupling capacitors provide localized switching current required by the power pins they connect to. Bypassing capacitors remove unwanted power supply noise before it can enter sensitive areas. Bulk capacitors are used to maintain constant dc voltage and provide switching currents required by all components.

In order for local decoupling capacitors to be effective, they must provide the least impedance at the switching frequency of the IC; otherwise, they will not discharge at all because the switching current will come from other lower impedance paths. Therefore, one must choose a decoupling capacitor that has a resonant frequency (where it has the lowest impedance) same as (or close to) the frequency of the switching, and place the decoupling capacitor as close to the power pin as possible to reduce trace inductance. In addition, the local decoupling capacitor must be large enough to provide the instantaneous current with tolerable voltage drop. The decoupling capacitance, required per VDD pin, could be calculated using the following formula:

$C = I \Delta t / \Delta V$, where

C = total capacitance in Farads

I = instantaneous switching current in Amps

Δt = the time duration of the switching current

ΔV = maximum allowed voltage drop on VDD supply

Instantaneous current (I) depends on the capacitive load of each output. The duration of the switching current depends on the capacitive load. The digital signals of the reference design card uses approximately 75 Ohm traces. When an output switches initially, it sees a 75 Ohm characteristic impedance and its output series resistance. As the load charges up exponentially, the amount of current required decreases until it reaches a steady state. To calculate the largest current demand of an output, one must know the output impedance. However, for CMOS device, the output impedance changes as the output changes. As an approximation, a D3MX output will require 50 mA of switching current for charging a 50 pF load from 0 to 5 volts in 5ns.

Using this figure, for a VDD pin supplying 4 outputs, each of which requires 50 mA for 5 ns, and a maximum allowable voltage spike of 100 mV, the capacitance required is: 4 * 50mA * 5ns / 100mV = 0.01 uF.
A 0.01 uF capacitor can be used in this case. That capacitor is placed across VDD and VSS pins.

4.8 PCI Interface

The reference design card supports a 32-bit PCI local bus interface. The PCI edge connector is a universal type allowing it to be plugged into a motherboard that supports either the 5V or the 3.3V signaling environments.

A 3.3V supply is provided to the TOCTL and FREEDM-32 by regulation of the 5V supply at the PCI edge connector.

4.9 Firmware Description

The firmware in the ROM enables the reading and writing to registers. This enables the TOCTL and D3MX devices to be reset, initialized and monitored for errors. Please refer to document [9] for more information.

4.10 Schematic Notes

The following is a detailed description of the key functional components shown in the schematics. The actual schematics are included in Appendix A.

4.10.1 Sheet 1: Root Drawing

This sheet provides a block view of the interface signals between each block. The transmit/receive signals are available at the line interfaces within the T3 line interface block. The transmit/receive data streams are terminated within the FREEDM-32 block. The following notes are provided:

- The reset signal from the microprocessor is routed to each TOCTL and D3MX device. The FREEDM-32 is reset via the PCI bus, whenever the system is reset, or whenever the FREEDM-32 is reset under software control.
- An on-board microprocessor block provides an interface to program each of the TOCTL and D3MX registers. It also provides a separate interrupt line for each TOCTL and the D3MX.
- The FREEDM-32 is programmed via an host processor at the PCI Interface.
- A JTAG chain connects the FREEDM-32, the TOCTL's and the MC68340.
- The Timing block provides a separate clock trace to each device that requires a clock (i.e. the D3MX and TOCTL's). This minimizes the adverse effects of reflections on the traces. When a device requires the same clock on multiple pins and the pins are closely spaced then only one trace is used to supply the clock signal.

4.10.2 Sheet 2: T3 Line Interface

This sheet provides an interface to the T3 port using the TDK78P7200 DS-3 Line Interface Transceiver. Resistors and capacitors are connected as outlined in the manufacturer’s datasheet for a DS-3 interface.

- The LOWSIGB output is used to gate the receive signals, RPOS and RNEG, whenever the received line signal level is below the threshold - such as when the cable is disconnected from the connector. This prevents upstream circuitry from falsely locking onto data when the receive signal is invalid.
- Jumper J2 at the LBO pin is for the transmitter line build out control. The jumper should set LBO LO for cable of 225' or longer, or LBO HIGH for short cable.
- A 75 ohm controlled impedance trace and driver is provided on the RCLK output.

- 75 ohm controlled impedance traces are used for transmit and receive signals.

- Ferrite beads and de-coupling capacitors are provided on power pins to reduce the effects of noise from the power supply.

4.10.3 Sheet 3: M13 Multiplex - D3MX

This sheet provides an M13 multiplexer using the PM8313 (D3MX).

- The quad 2-input multiplexer shown as U2, and the jumper J1, enable the transmit data to be either loop-timed (J1 shorted) or timed via the on-board oscillator (J1 open).

- The 44.736 MHz timing is provided via a 75ohm controlled impedance trace.

- Transmit and receive signals from the T3 line interface are provided via 75 ohm controlled impedance traces.

- An 8-bit line driver, shown as U4 in the schematic, drives an LED array based on D3MX signal pins RLOS, REXZ, RAIS, ROOF/RRED and RFERF. Unused inputs are tied to ground to prevent LED flickering.

- Capacitors of 0.01uF are used on all power pins for de-coupling the power supply noise.

4.10.4 Sheet 4,5: T1 Framers - TOCTL

These sheets provide T1 framing for 32 T1 data streams using four PM4388 (TOCTL) devices.

- Capacitors of 0.01uF are used on all power pins for de-coupling the power supply noise.

- ALE pin must be pulled high.

- TOCTL #4, labeled U12, only uses four of the eight available framers. All unused inputs are grounded for lower power consumption.

4.10.5 Sheet 6: FREEDM-32 and PCI Bus Interface

This sheet provides the frame relay processor using the PM7364 (FREEDM-32).

- The PCI Interface is run to a card edge connector. The 3.3V power pins at the edge connector are not used since the commonly available motherboards do not provide power to the 3.3V pins and/or do not provide a 3.3V connector (or combined 5V/3.3V connector) on the motherboard. Instead, the power supply is provided by regulation of +5V as described on sheet 7.

4.10.6 Sheet 7: Power Supply

This sheet contains the 3.3V and the 5V power supplies for the reference design board. It also includes the 0.01uF de-coupling capacitors for the FREEDM-32.

- The PCI connector, P1, supplies the +5V (VDD) and GND. This supply is routed directly to all parts requiring +5V power.

- VDD is supplied to the regulator LT1528, shown as U14 on the schematic, which provides +3.3V power for the TOCTL devices.

- U14 also provides a regulated +3.3V supply that is used to power the FREEDM-32.

4.10.7 Sheet 8: Timing

This sheet provides timing to the TOCTL's, and D3MX.

- The 8-bit line drivers shown as U6 and U7 drive separate impedance controlled traces (75 ohm) to each of the TOCTL and D3MX device pins.

- The 44.736 MHz oscillator (Y1) provides the T3_CLK signal which indirectly connects to the TICLK pin of the D3MX (This clock is bypassed when J1 is set for loop-timed operation). The transmit input clock pin (TICLK) provides timing for the transmit direction of the T3 interface.

- The 37.056 MHz oscillator (Y2) provides the XCLK signal. This connects via separate impedance controlled traces to the XCLK pins of the four TOCTL devices. This clock provides a timing reference for the devices and is used for jitter attenuation.

- The 1.544 MHz oscillator Y3 provides the T1_CLK signal. This connects via separate impedance controlled traces to each of the four TOCTL devices. Each trace is routed to CTCLK and CECLK pins of a TOCTL in series to minimize the adverse effects of reflections. This oscillator supplies each TOCTL with the common transmit clock and common egress clock.

4.10.8 Sheet 9: On-board Microprocessor - MC68340

This sheet contains a 25MHz MC68340 microprocessor, a serial interface for user control and monitoring, a reset circuit, and a debug connector for software development. The following notes are provided for this sheet:

- MAX202 (U22) is used for the RS232 interface. A 3.6864MHz oscillator shown as Y5 is used for the RS232 interface.
- The reset circuit, controlled by switch, SW1, resets the MC68340 and provides RSTB to reset all other devices.
- Background Debug Monitor (BDM) connector, J6, is used for software development. Note that pin BKPTB must be pulled-up to VCC (through 10K). It is recommended that pin BERRB be pulled up also in a similar fashion. CLKOUT from the MC68340 needs to be connected to a test point to be used by the BDM connector. XFC pin of the MC68340 needs to be de-coupled with 0.1uF to ground.

Other details on the MC68340:

- XTAL must be left open if external oscillator used for SYSCLK, which is the case in this reference design.
- VCCSYN needs to be pulled up to VCC.
- All unused inputs are pulled up through 10K.
- De-coupling capacitors of 0.01uF are used for each power pin of the MC68340.

4.10.9 Sheet 10: Microprocessor Decode Logic

This sheet contains decode logic for the MC68340 that is necessary to interface to the SRAM, the EPROM, the four TOCTL's and the D3MX. The following notes are provided for this sheet:

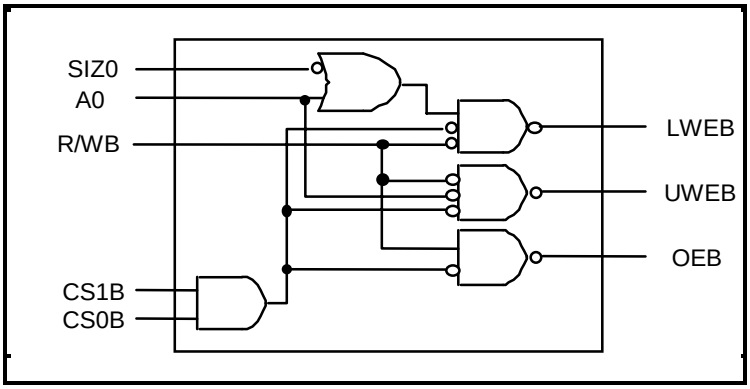
- Address pins A0 through A17 of the MC68340 address bus is connected to external circuitry. The line drivers provided by U18 serve to minimize loading of the MC68340 address pins A0 through A15. These provide a capacitive load that is well within the tolerable limit of 100pF for the MC68340. The propagation delay for signals passed through the line drivers is within the maximum of 10ns for address valid to address strobe (AS) asserted, or for address valid to chip select (CS0, CS1, CS2, CS3) asserted. U18 drives 16

address pins of the SRAM. U19 drives A0 through A10 which are connected to the four TOCTLs and A0 through A8 on one D3MX.

- The data pins D8 through D15 of the MC68340 are extended to the four TOCTLs and the D3MX via the 8-bit transceiver shown as U25. These same data pins from U23, combined with the D0 through to D7 data pins, are extended to the SRAM and EPROM.

- The 128 Kword of SRAM consisting of U16 and U17 is driven for read or write access by decode logic within a 22V10 PAL shown as U21. Figure 9 shows the decode logic based on the MC68340 signals provided to the PAL.

Figure 9 - Logic of Signals Provided to SRAM



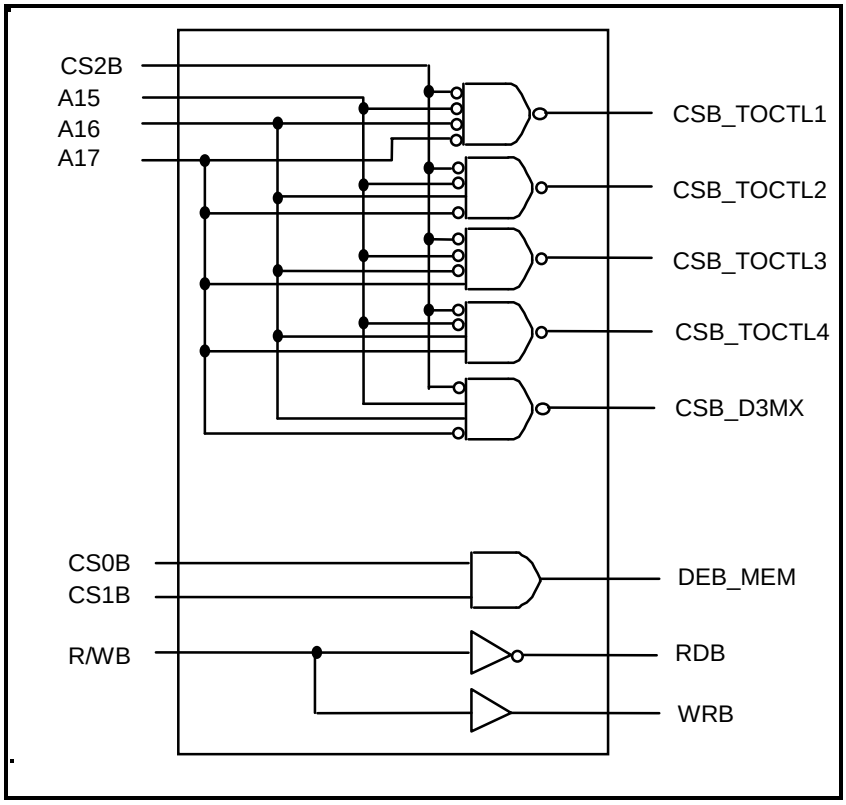
Note: CS1B and CS0B are AND'ed together (i.e. either CS0B or CS1B asserted) since the MC68340 always asserts CS0B during code download into SRAM using the background debug monitor, while it asserts CS1B during normal SRAM accesses. This applies to the case where only the SRAM is being used (typically during code development). If the EPROM is used (which is selected by CS0B), then this AND gate should be removed, and only CS1B should be used here.

- CS0B of the MC68340 provides an active low chip select to the EPROM shown as U15.

- CS2B of the MC68340 provide an active low chip select to the four TOCTL's, and the D3MX using the decode logic shown in figure 10. The decode logic is implemented by the 22V10 PAL shown as U24 in the schematic. The RDB and WRB signals are also derived from the R/WB signal.

- The decode logic of the PAL in figure 10 also provides an output enable to the data transceiver U23 connected to the SRAM and EPROM. CS2B is used as the output enable to the data transceiver U25.

Figure 10 - Decode Logic Provided by U24



- Wait states are required during read accesses to TOCTL and D3MX devices. The datasheet specifies a maximum propagation delay of 80ns, which implies that 1 wait state is necessary to interface the MC68340 with each of these. The wait state is programmed via a register within the MC68340 such that whenever the CS2B is active there is one wait state inserted.

- Sample VHDL code for the two 22V10 PALs is included in Appendix B.

5 GLOSSARY

Bit Stuffing	A process in data communications protocols where a string of "one" bits in the data payload is broken by an inserted "zero". The idea of inserting the zero is to ensure that no flag control character is found in the user payload.
CRC	Cyclic Redundancy Check: Check sums generated from recursive algorithms that can be used to determine the integrity of data by a receiver. Certain CRC algorithms allows the receiver to detect as well as correct certain number of bit errors.
DLCI	Data Link Connection Identifier (DLCI): The frame relay virtual circuit number corresponding to a particular destination which is part of the frame relay header and is usually ten bits long. The DLCI is typically associated with a particular PVC on the network.
DS-0	Digital Service, level 0: There are 24 DS-0 channels in a DS-1. Each DS-0 has a bandwidth of 64 Kbit/s.
DS-1	Digital Service, level 1: It is 1.544 Mbit/s in North America. In channelized mode, each DS-1 consists of 24 DS-0 channels. In unchannelized mode, each DS-1 has a full-duplex bandwidth of 1.544 Mbit/s.
DS-3	Digital Service, level 3: DS-3 is equivalent to 28 DS-1 channels. It operates at 44.736 Mbit/s.
DSLAM	Digital Subscriber Loop Access Multiplexer.
FCS	Frame Check Sequence: Bits added to the end of a frame for error detection. In bit-oriented protocols, a frame check sequence is a 16-bit field added to the end of a frame that contains transmission error-checking information.
Flag	In synchronous transmission, a flag is a pattern of "01111110" used to mark the beginning and end of a frame.
FRAD	Frame Relay Access Device.

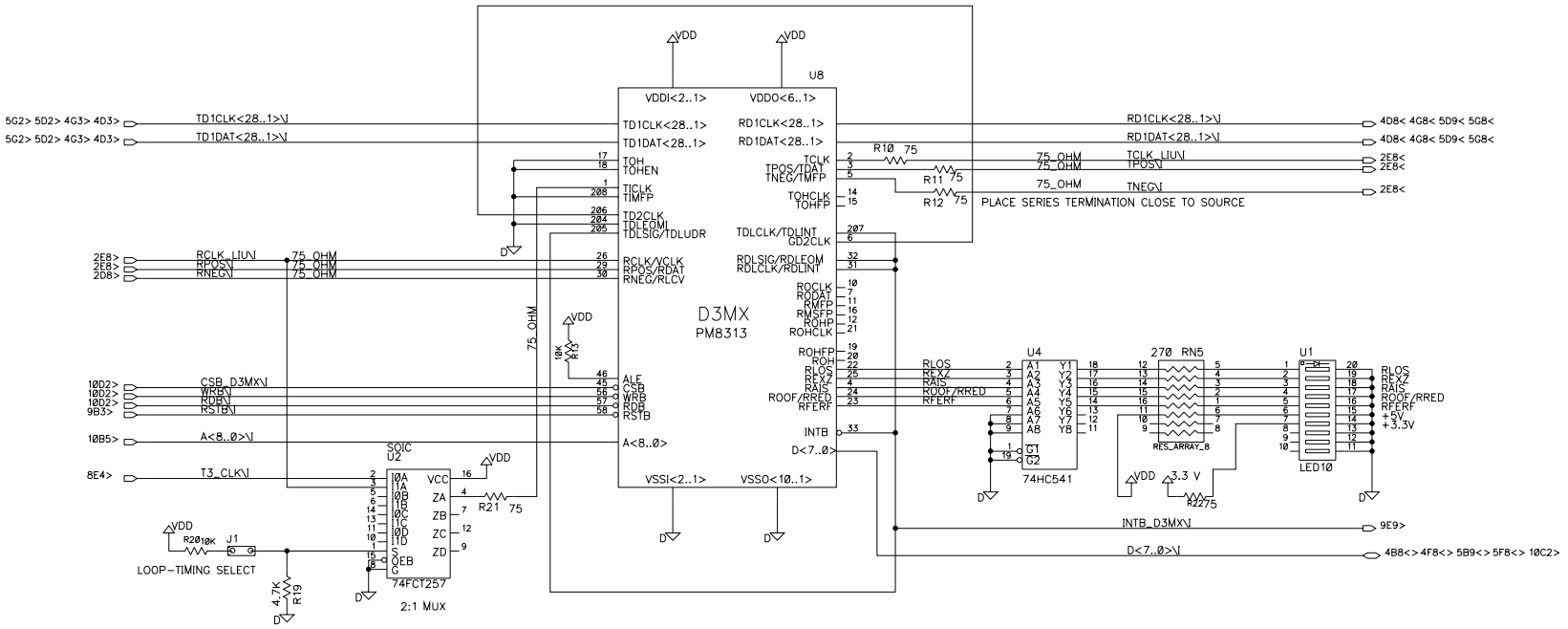
Frame	A frame is also referred to as a "packet" and is a logical transmission unit. A frame consists of a group of data bits in a specific format. Generally, a flag is used at each end of the frame to delimit the start and end of the frame.
Frame Relay	The term "frame relay" is used in multiple contexts and can be used to refer to a switching technology, an interface standard or a set of data services.
Full-Duplex	Refers to simultaneous transmission in two directions.
FUNI	Frame Relay User Network Interface
HDLC	High Level Data Link Control: A standard bit-oriented protocol developed by ITU.
HSSI	High Speed Serial Interface
ISP	Internet Service Provider:
Multiplexer	Electronic equipment which allows two or more signals to pass over one communication circuit.
NAP	Network Access Point:
OSI	Open System Interconnect: An ISO publication that defines seven independent layers of communication protocols. Each layer enhances the communication services of the layer just below it and shields the layer above it from the implementation details of the lower layer.
OSI Model	The only internationally accepted framework of standards for communication between different systems made by different vendors. The OSI model organizes the communications process into the following seven layers: Layer 1 - Physical Layer Layer 2 - Data Link Layer Layer 3 - Network Layer Layer 4 - Transport Layer Layer 5 - Session Layer Layer 6 - Presentation Layer Layer 7 - Application Layer
Packet	A packet is also referred to as a "frame" and is a logical transmission unit.
PCI	Peripheral Component Interconnect

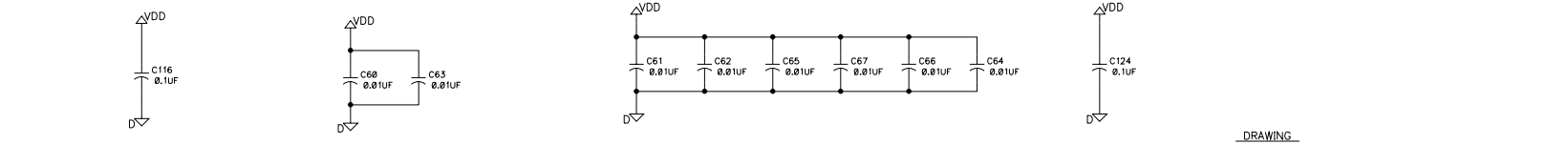
POP	Point of Presence: In telecommunication, POP refers to the physical place within a LATA where a long distance carrier interfaces with the network of the local exchange carrier.
UNI	User Network Interface: The physical and electrical demarcation point between the user and the public network service provider.

6 APPENDIX A: SCHEMATICS, LAYOUT

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

M13 MULTIPLEXER/DEMULTIPLEXER





DECOUPLING CAPS FOR FCT257

DECOUPLING CAPS FOR VDDI

DECOUPLING CAPS FOR VDDO

DECOUPLING CAPS FOR 541

DRAWING

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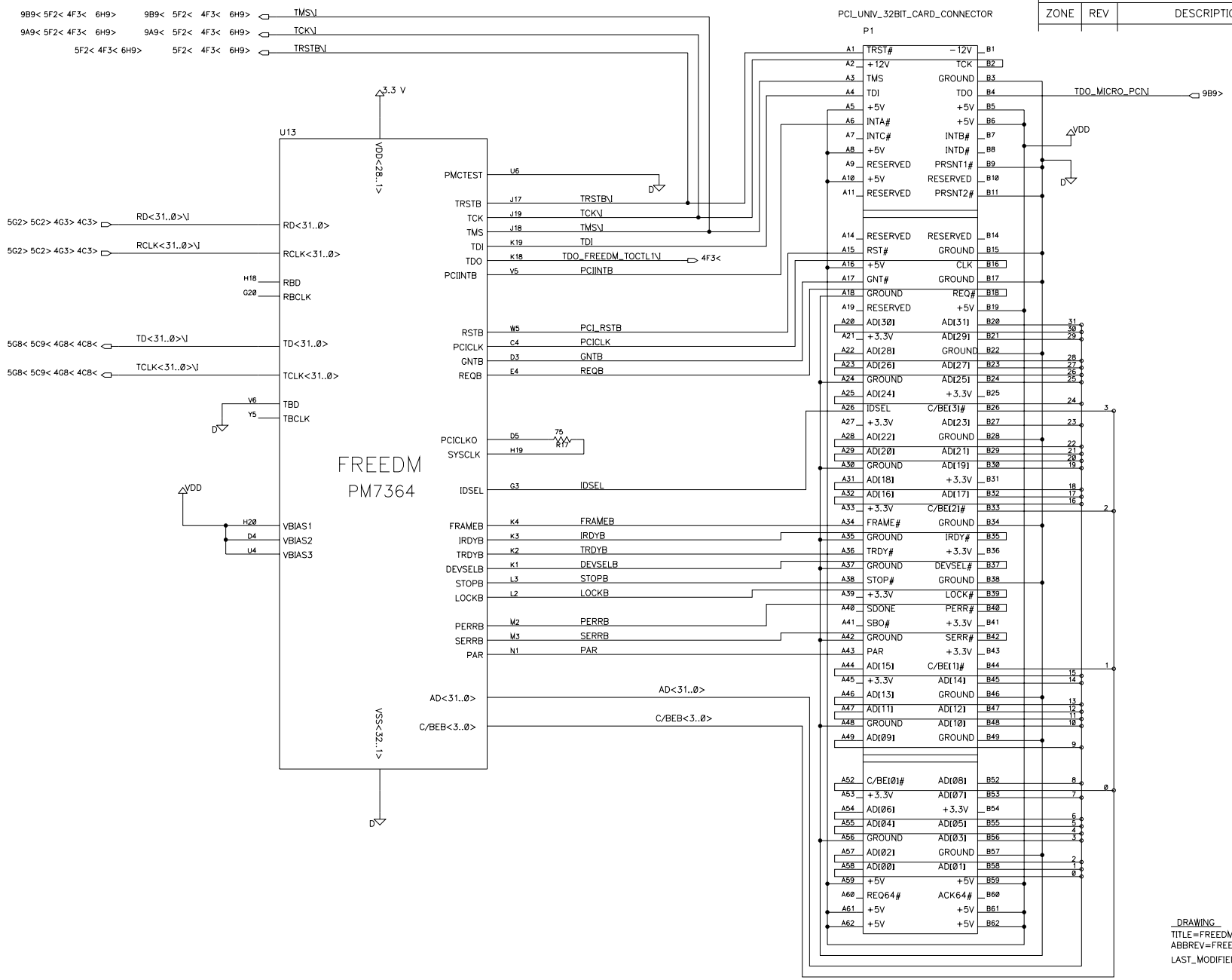
ABBREV=D3MX
LAST_MODIFIED=Tue Oct 27 11:06:14 1998

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980942 *PRELIMINARY*	ISSUE: 1.0
TITLE: CABGA TOCTL REFERENCE DESIGN D3MX	DATE: SEPT. 15, 98
ENGINEER: WARREN TAM	PAGE: 3 OF 10



NOTE

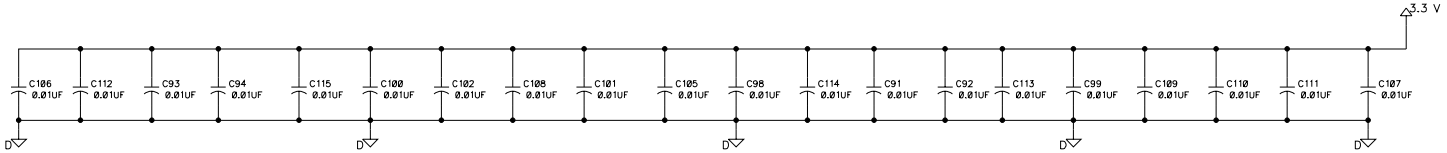
CHECK THE LATEST PCI SPEC FOR
COMPONENT AND LAYOUT RESTRICTIONS

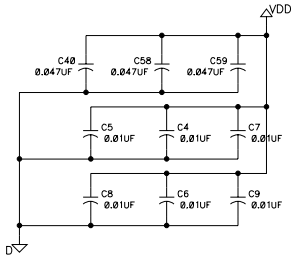
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980942 *PRELIMINARY*	ISSUE: 1.0
TITLE: CABGA TOCTL REFERENCE DESIGN FREEDM & PCI CONNECTOR	DATE: SEPT. 15, 98
ENGINEER: WARREN TAM	PAGE: 6 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

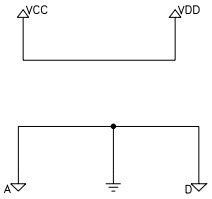
DECOUPLING CAPS FOR FREEDM VDD



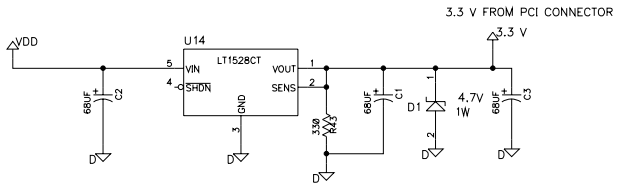


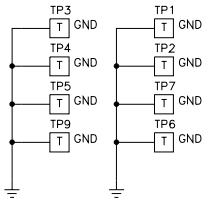
NOTE:

THE FOLLOWING DECOUPLING CAPS ARE USED FOR PCI BUS POWER RAIL. THEY SHOULD BE PLACED IN SUCH A WAY THAT AT LEAST AN AVERAGE OF Ø.Ø1UF PER VDD PIN IS ACHIEVED.



SINGLE GROUND PLANE USED





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ENGINEER: WARREN TAM	PAGE: 7 OF 10

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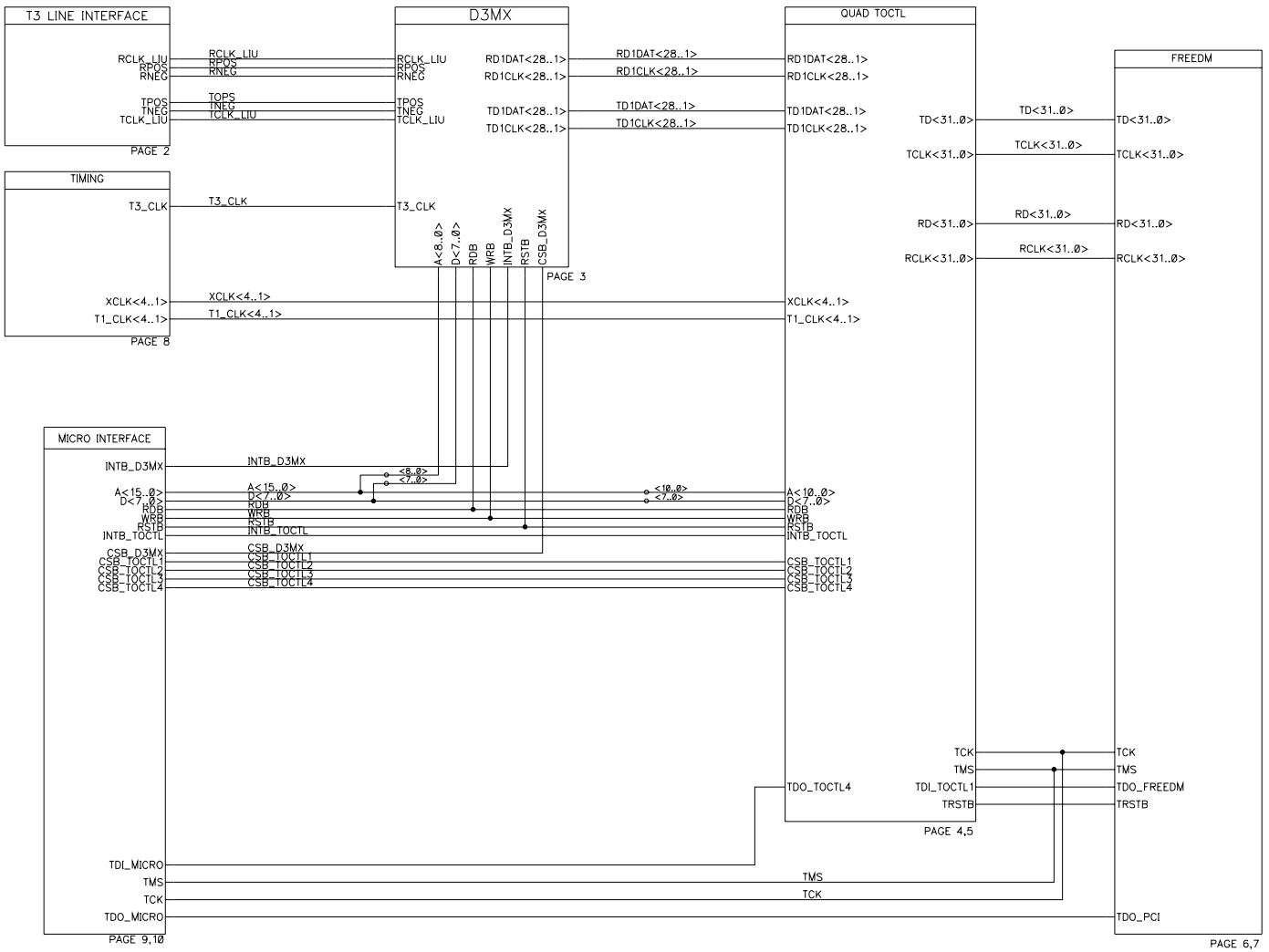

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PMC-Sierra, Inc.

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ENGINEER: WARREN TAM	PAGE: 1 OF 10

MICROPROCESSOR CIRCUIT

REVISIONS				
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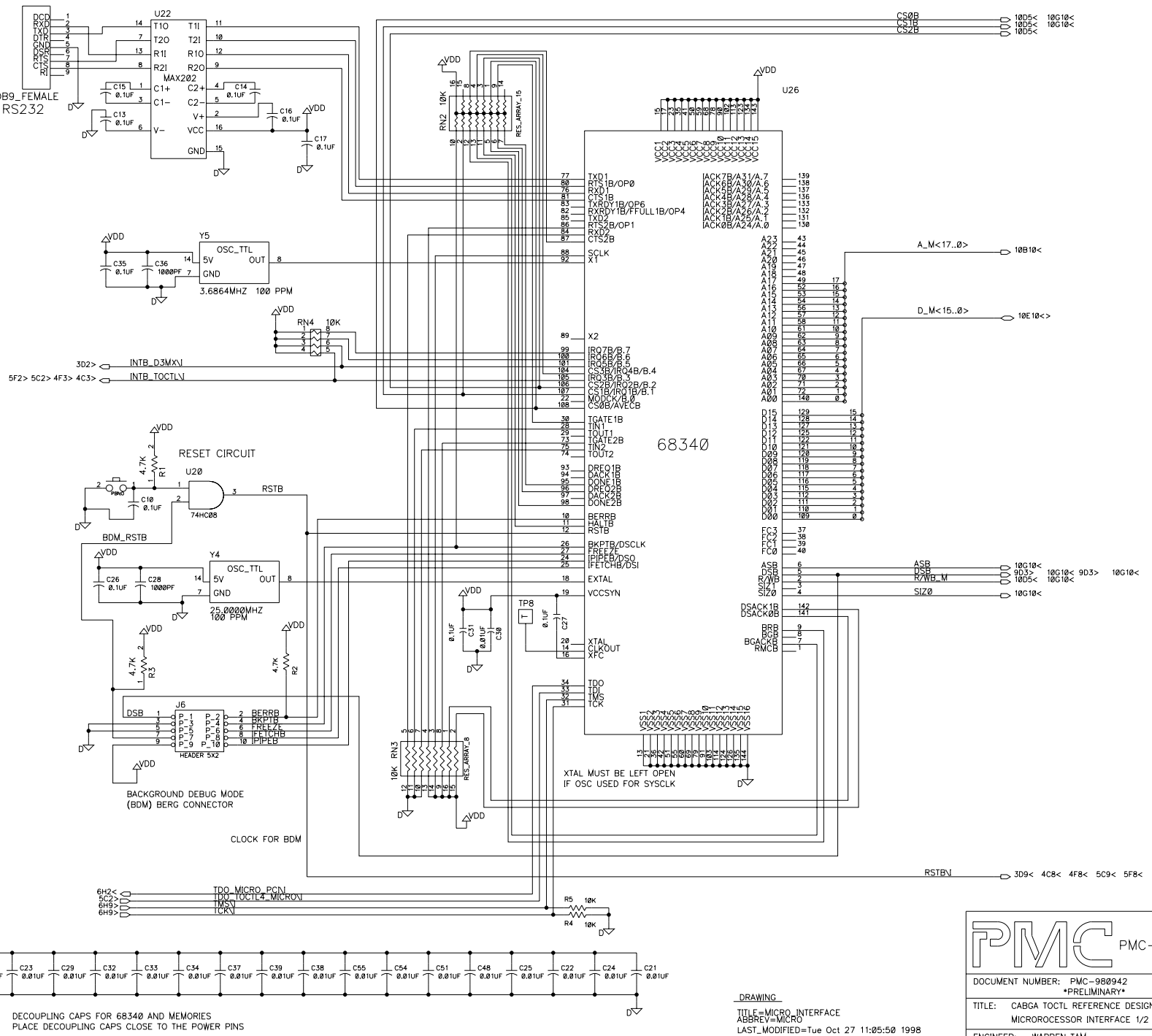

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PMC-Sierra, Inc.

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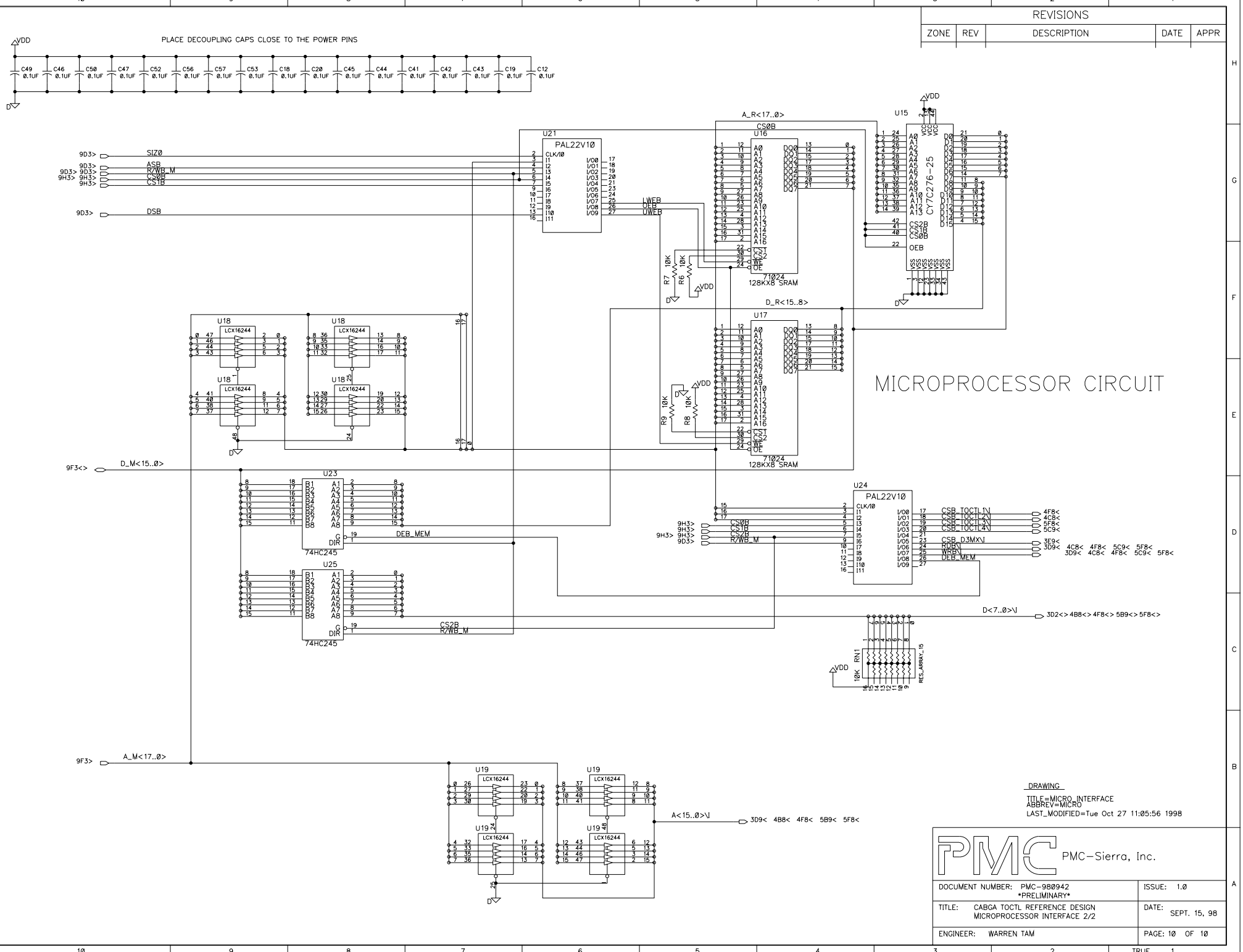
ENGINEER: WARREN TAM	PAGE: 9 OF 10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C50 0.1UF
C47 0.1UF
C52 0.1UF
C56 0.1UF
C57 0.1UF
C53 0.1UF
C18 0.1UF
C20 0.1UF
C45 0.1UF
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C43 0.1UF
C19 0.1UF
C12 0.1UF
MICROPROCESSOR CIRCUIT
U21
PAL22V10
U15
CY7C276-25
U16
U17
71024
128KX8 SRAM
U18
LCX16244
U23
U25
74HC245
U24
PAL22V10
U19
LCX16244
RN1
RES_ARRAY_15
10K
R6
R7
R8
R9
SIZ0
ASB
R/WB_M
CS0B
CS1B
DSB
LWEB
OEB
UWEB
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CS2B
R/WB_M
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PMC-Sierra, Inc.
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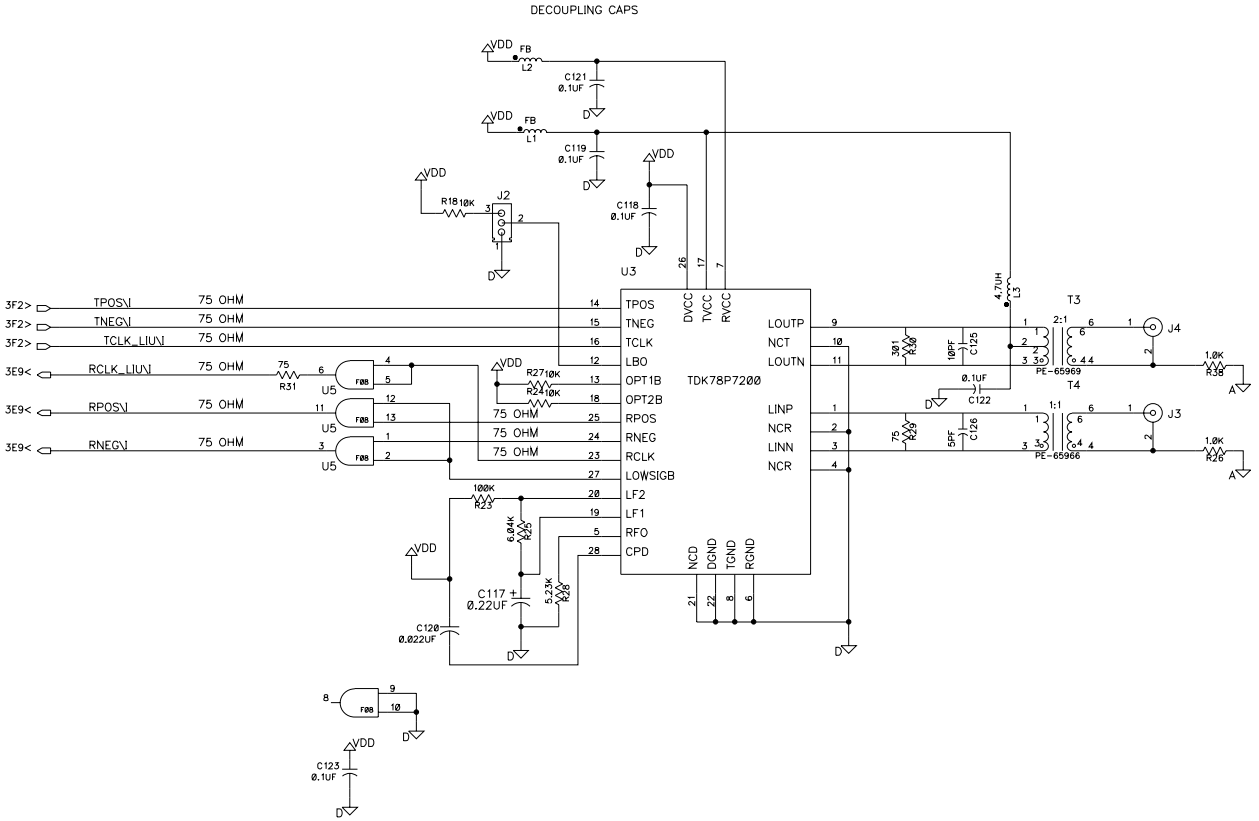
ISSUE: 1.0
TITLE: CABGA TOCTL REFERENCE DESIGN
MICROPROCESSOR INTERFACE 2/2
DATE: SEPT. 15, 98
ENGINEER: WARREN TAM
PAGE: 10 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

T3 LINE INTERFACE



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PMC-Sierra, Inc.

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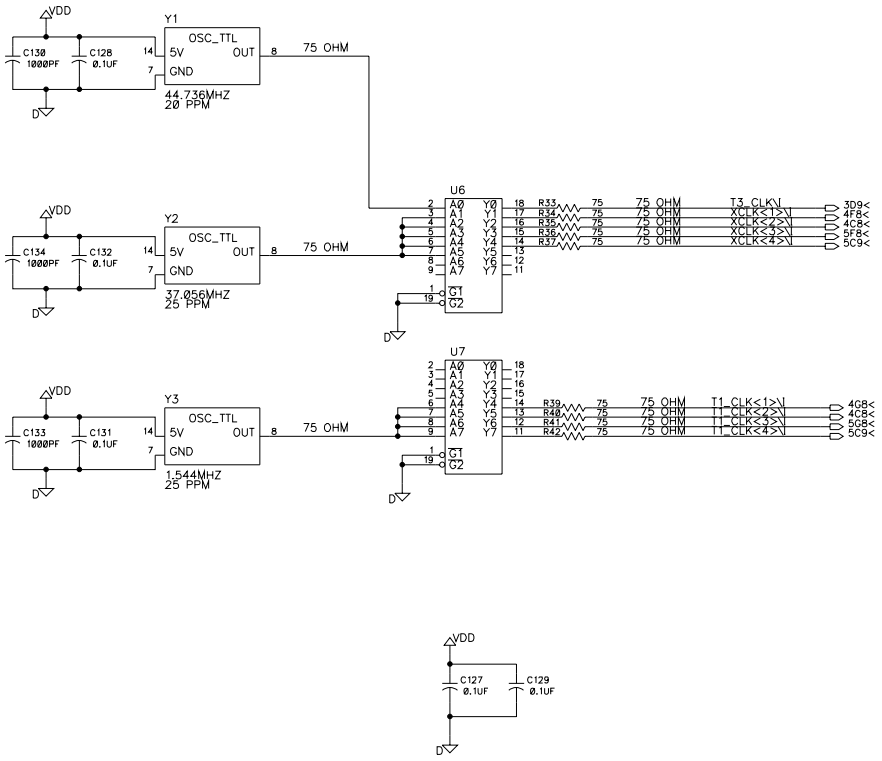
TITLE: CABGA TOCTL REFERENCE DESIGN T3_LINE_INTERFACE	DATE: SEPT. 15, 98
ENGINEER: WARREN TAM	PAGE: 2 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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PMC-Sierra, Inc.

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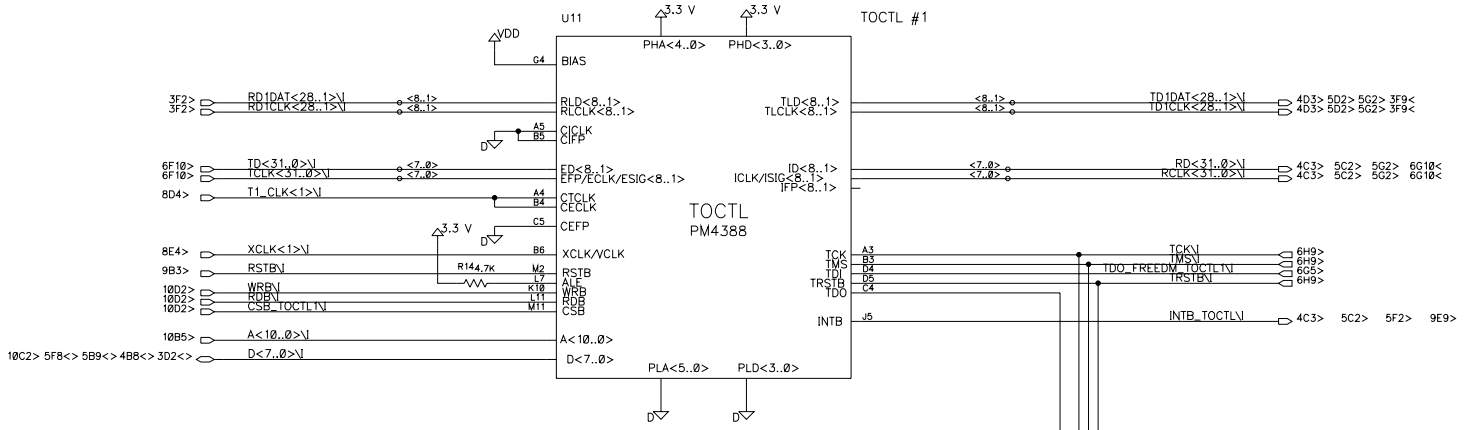
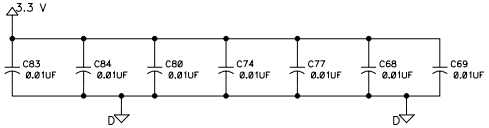
TITLE: CABGA TOCTL REFERENCE DESIGN TIMING	DATE: SEPT. 15, 98
ENGINEER: WARREN TAM	PAGE: 8 OF 10

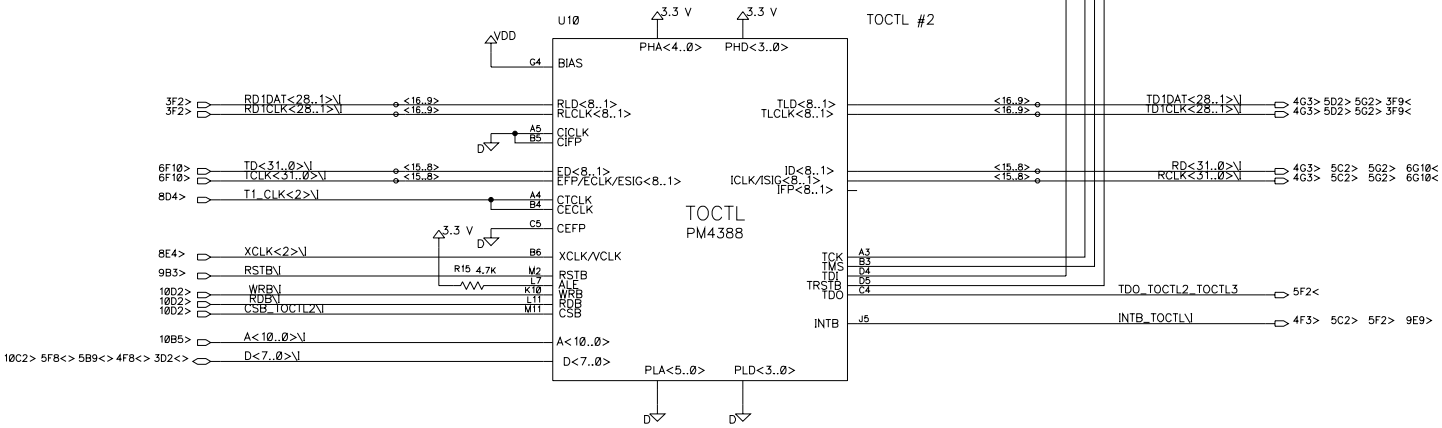
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

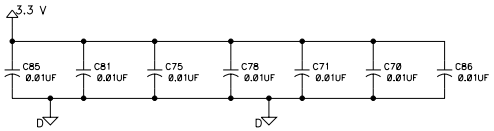
OCTAL T1 FRAMER





NOTE: PLACE ALL DECOUPLING CAPS NEAR POWER PINS





NOTE: PLACE ALL DECOUPLING CAPS NEAR POWER PINS

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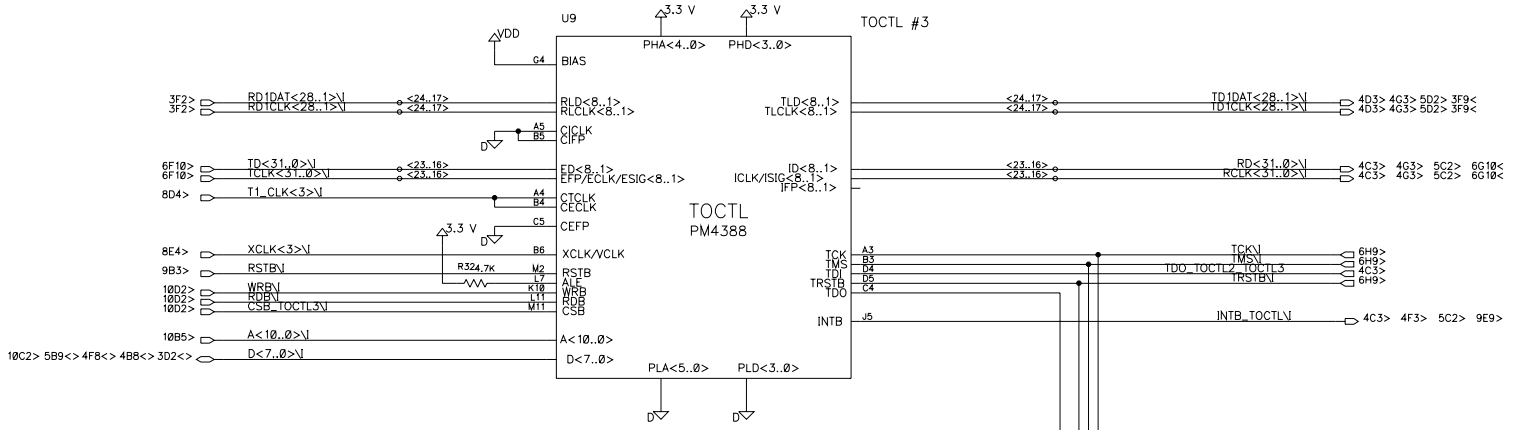
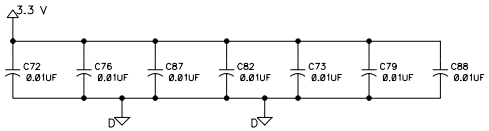
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980942 *PRELIMINARY*	ISSUE: 1.0
TITLE: CABGA TOCTL REFERENCE DESIGN QUAD TOCTLS 1/2	DATE: SEPT. 15, 98
ENGINEER: WARREN TAM	PAGE: 4 OF 10

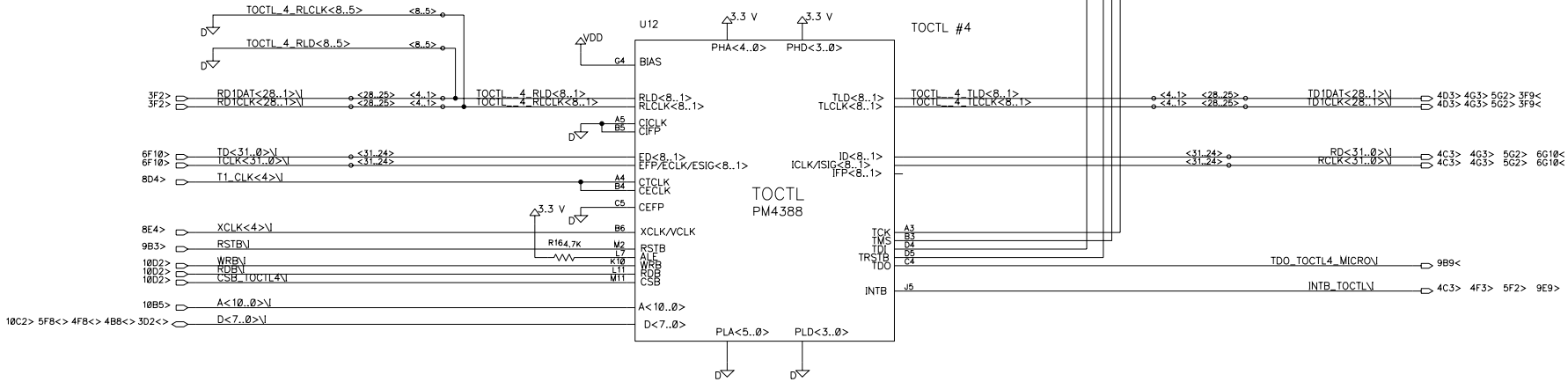
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

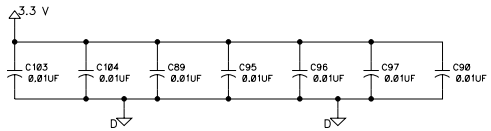
OCTAL T1 FRAMER





NOTE: PLACE ALL DECOUPLING CAPS NEAR POWER PINS





NOTE: PLACE ALL DECOUPLING CAPS NEAR POWER PINS

DRAWING

TITLE=TOCTL_BLOCK
ABBREV=TOCTL
LAST_MODIFIED=Tue Oct 27 11:06:10 1998

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7 APPENDIX B: PAL VHDL CODE

7.1 U21 Chip Selects for SRAM

There are two versions of VHDL code for U21. One is for operation from the EPROM and one is for operation from the debug port.

7.1.1 Operation from EPROM

```
-- CABGA TOCTL w\ FREEDM-32 reference design ver1.0
-- 22V10 PAL U21 for operation from ROM
--
-- Function:
--      logic for chip selects for SRAM for operation from ROM
-- Author:
--      Warren Tam
-- History:
--      Sept 25, 1998    Created.
-- Description:
--      Generates Chip selects for SRAM for operation from ROM
--

USE work.rtlpkg.all;
USE work.cypress.all;

ENTITY u21_pal IS
PORT   (
siz0, a0, asb, rwb, cs0b, cs1b, dsb: IN BIT;
lweb, oeb, uweb: OUT BIT);

ATTRIBUTE order_code of u21_pal:ENTITY is "PAL22V10H-5JC";
ATTRIBUTE part_name of u21_pal:ENTITY IS "C22V10";

ATTRIBUTE pin_numbers of u21_pal:ENTITY IS
      "siz0:2  " &
      "a0:3  " &
      "asb:4  " &
      "rwb:5     " &
      "cs0b:6     " &
      "cs1b:7     " &
      "dsb:13     " &
      "lweb:25     " &
      "oeb:26     " &
      "uweb:27     " ;
END u21_pal;

ARCHITECTURE behavior OF u21_pal IS

--

BEGIN
      lweb <= not(((not siz0)or(a0))and(not cs1b)and(not rwb));
```

```
      oeb  <= not ( rwb and (not cs1b));
      uweb  <= not ((not rwb) and (not a0) and (not cs1b));
END behavior;
```

7.1.2 Operation from Debug Port

```
-- CABGA TOCTL w\ FREEDM-32 reference design ver1.0
-- 22V10 PAL U21 for operation with debug port
--
-- Function:
--      logic for chip selects for SRAM
-- Author:
--      Warren Tam
-- History:
--      Sept 25, 1998    Created.
-- Description:
--      Generates Chip selects for SRAM for operation from the debug port
--

USE work.rtlpkg.all;
USE work.cypress.all;

ENTITY u21_pal IS
PORT   (
siz0, a0, asb, rwb, cs0b, cs1b, dsb: IN BIT;
lweb, oeb, uweb: OUT BIT);

ATTRIBUTE order_code of u21_pal:ENTITY is "PAL22V10H-5JC";
ATTRIBUTE part_name of u21_pal:ENTITY IS "C22V10";

ATTRIBUTE pin_numbers of u21_pal:ENTITY IS
      "siz0:2  " &
      "a0:3  " &
      "asb:4  " &
      "rwb:5     " &
      "cs0b:6     " &
      "cs1b:7     " &
      "dsb:13     " &
      "lweb:25     " &
      "oeb:26     " &
      "uweb:27     " ;
END u21_pal;

ARCHITECTURE behavior OF u21_pal IS

--

BEGIN
      lweb <= not(((not siz0)or(a0))and(not(cs1b and cs0b))and(not rwb));
      oeb  <= not ( rwb and (not (cs1b and cs0b)));
      uweb  <= not ((not rwb) and (not a0) and (not (cs1b and cs0b)));
END behavior;
```

7.2 U24 Chip Selects for TOCTL and D3MX

```
-- CABGA TOCTL w/ FREEDM-32 reference design ver1.0
-- 22V10 PAL U24
--
-- Function:
--      logic for chip selects for TOCTL and D3MX
-- Author:
--      Warren Tam
-- History:
--      Sept 25, 1998    Created.
-- Description:
--      Generates Chip selects, read and write for TOCTL and D3MX
--

USE work.rtlpkg.all;
USE work.cypress.all;

ENTITY u24_pal IS
PORT   (
a15, a16, a17, cs0b, cs1b, cs2b, rwb: IN BIT;
csb_toctl1, csb_toctl2, csb_toctl3, csb_toctl4, csb_d3mx, rdb, wrb, deb_mem:
OUT BIT);

ATTRIBUTE order_code of u24_pal:ENTITY is "PAL22V10H-5JC";
ATTRIBUTE part_name of u24_pal:ENTITY IS "C22V10";

ATTRIBUTE pin_numbers of u24_pal:ENTITY IS
      "a15:2  " &
      "a16:3  " &
      "a17:4  " &
      "cs0b:5     " &
      "cs1b:6     " &
      "cs2b:7     " &
      "rwb:9     " &
      "csb_toctl1:17     " &
      "csb_toctl2:18     " &
      "csb_toctl3:19     " &
      "csb_toctl4:20     " &
      "csb_d3mx:23     " &
      "rdb:24     " &
      "wrb:25     " &
      "deb_mem:26     " ;
END u24_pal;

ARCHITECTURE behavior OF u24_pal IS

--

BEGIN
      wrb <= rwb;
      rdb <= NOT rwb;
      deb_mem <= cs0b AND cs1b;
      csb_toctl1 <= not ((not cs2b) AND (not a15) AND (not a16) AND (not
a17));
```

```
      csb_toctl2 <= not ((not cs2b) AND (not a15) AND (    a16) AND (not
a17));
      csb_toctl3 <= not ((not cs2b) AND (not a15) AND (not a16) AND (
a17));
      csb_toctl4 <= not ((not cs2b) AND (not a15) AND (    a16) AND (
a17));
      csb_d3mx   <= not ((not cs2b) AND (    a15) AND (    a16) AND (not
a17));
END behavior;
```

8 APPENDIX C: BILL OF MATERIALS

Item	Description	Vendor Part No.	Reference Designator	QTY
1	128K BY 8 STATIC RAM	FAI.ELECTRONICS IDT71024S15TY	U16, U17	2
2	QUAD 2 INPUT AND GATE (SOIC –14)	DIGI-KEY 74F08SC-ND	U5	1
3	QUAD 2 INPUT MUX (SOIC-16)	DIGI-KEY PI74FCT257ATS-ND	U2	1
4	NON-INV OCTAL BUFFER/LINE DRIVER (SOIC-20)	DIGI-KEY PI74FCT541ATS-ND	U6, U7	2
5	16 BIT BIDIRECTIONAL TRANSCEIVER (48 SSOP)	DIGI-KEY 74LCX16244MEA-ND	U18, U19	2
6	QUAD 2 INPUT AND GATE (SOIC-14)	DIGI-KEY MM74HC08M-ND	U20	1
7	OCTAL TRI STATE BUS TRANSCEIVER (SOIC-20)	DIGI-KEY MM74HC245AWM-ND	U23, U25	2
8	OCTAL TRI STATE BUFFER	DIGI-KEY MM74HC541N-ND	U4	1
9	BNC CONNECTOR (RIGHT ANGLE)	DIGI-KEY ARF1065-ND	J3, J4	2
10	CAPACITOR-0.001UF, 50V, NPO_805	DIGI-KEY PCC102CGCT-ND	C28, C36, C130, C133, C134	5
11	CAPACITOR-0.01UF, 50V, X7R_603	DIGI-KEY PCC103BVCT-ND	C4-C9, C11, C21-C25, C29, C30, C32-C34, C37-C39, C48, C51, C54, C55, C60-C115	80
12	CAPACITOR-0.022UF, 50V, X7R_805	DIGI-KEY PCC223BGCT-ND	C120	1
13	CAPACITOR-0.047UF, 50V, X7R_1206	DIGI-KEY PCC473BCT-ND	C40, C58, C59	3
14	CAPACITOR-0.1UF, 50V, X7R_805	NEWARK 96F8740	C10, C12-C20, C26, C27, C31, C35, C41-C47, C49, C50, C52, C53, C56, C57, C116, C118, C119, C121-C124, C127-C129, C131, C132	39
15	CAPACITOR-0.22UF, 35V, TANT TEH	DIGI-KEY PCT6224CT-ND	C117	1
16	CAPACITOR-10PF, 50V, NPO_805	DIGI-KEY PCC100CNCT-ND	C125	1
17	CAPACITOR-5PF, 50V, NPO_805	DIGI-KEY PCC050CNCT-ND	C126	1

18	CAPACITOR-68UF, 6.3V, TANT TEH	DIGI-KEY PCT1686CT-ND	C1-C3	3
19	CYPRESS 16K X 16 PROM	ARROW-ELECTRONICS CY7C276-25J-CCYPRESS REPROGRAMMABLE	U15	1
20	D3MX (M13 MULTIPLEXER)	PM8313	U8	1
21	DB9 FEMALE CONNECTOR	DIGI-KEY A2100-ND	J5	1
22	DIODEZENER_SMD-4.7V, 1W	DIGI-KEY ZM4732ACT-ND	D1	1
23	FREEDM-32 (FRAME RELAY PROTOCOL ENGINER AND DATA LINK MANAGER)	PM7364	U13	1
24	1 X 2 JUMPER	DIGI-KEY S1011-36-ND	J1	1
25	2 X 5 JUMPER	DIGI-KEY S2012-05-ND	J6	1
26	1 X 3 JUMPER	DIGI-KEY S1011-36-ND	J2	1
27	INDUCTOR-4.7UH	DIGI-KEY PCD1236CT-ND	L3	1
28	INDUCTOR-FB, 50, FAIR RITE	FAIR RITE 2743019447	L1, L2	2
29	RED LED10, 25MA, 2.1V	DIGI-KEY LT1066-ND	U1	1
30	3A LOW DROPOUT LINEAR TECHNOLOGY REGULATOR	ARROW-ELECTRONICS LT1528CQ-LINEAR TECHNOLOGY	U14	1
31	RS232 TRANSCEIVER MAX202 (SOIC-16)	DIGI-KEY MAX202CSE-ND	U22	1
32	MC68340 MOTOROLA CPU	FAI-ELECTRONICS MC68340FE25E	U26	1
33	OSC_TTL DIP-1.544MHZ, 25 PPM, CHA	CONNOR WINFIELD HC13R8	Y3	1
34	OSC_TTL DIP-25.0000MHZ, 100 PPMA	DIGI-KEY CTX176-ND	Y4	1
35	OSC_TTL DIP-3.6864MHZ, 100 PPM, A	DIGI-KEY CTX154-ND	Y5	1
36	OSC_TTL DIP-37.056MHZ, 25 PPM, CA	CONNOR WINFIELD HC13R8	Y2	1
37	OSC_TTL_DIP-44.736MHZ, 20 PPM, CA	CONNOR WINFIELD HC54R8	Y1	1
38	PAL	FAI-ELECTRONICS PALCE22V10H-5JC	U21, U24	2
39	RESET SWITCH	DIGI-KEY CKN4002-ND	SW1	1
40	1:1 LINE TRANSFORMER FOR T3 RECEIVE	SAGER ELECTRICAL SUPPLY PE65966	T4	1

41	1:2 LINE TRANSFORMER FOR T3 TRANSMIT	SAGER ELECTRICAL SUPPLY PE65969	T3	1
42	RESISTOR-1.0K, 5%, 805	DIGI-KEY P1.0KACT-ND	R26, R38	2
43	RESISTOR-100K, 5%, 805	DIGI-KEY P100KACT-ND	R23	1
44	RESISTOR-10K, 5%, 805	DIGI-KEY P10KACT-ND	R4-R9, R13, R18, R20, R24, R27	11
45	RESISTOR-301, 1%, 805	DIGI-KEY P301CCT-ND	R30	1
46	RESISTOR-330, 5%, 805	DIGI-KEY P330ACT-ND	R43	1
47	RESISTOR-4.7K, 5%, 603	DIGI-KEY P4.7KGCT-ND	R14-R16, R32	4
48	RESISTOR-4.7K, 5%, 805	DIGI-KEY P4.7KACT-ND	R1-R3, R19	4
49	RESISTOR-5.23K, 1%, 805	DIGI-KEY P5.23KCCT-ND	R28	1
50	RESISTOR-6.04K, 1%, 805	DIGI-KEY P6.04KCCT-ND	R25	1
51	RESISTOR-75, 5%, 805	DIGI-KEY P75ACT-ND	R10-R12, R17, R21, R22, R29, R31, R33-R37, R39-R42	17
52	RES_ARRAY_15_SMD-10K	DIGI-KEY 766-161-R10K-ND	RN1, RN2	2
53	RES_ARRAY_4_SMD-10K	DIGI-KEY Y4103CT-ND	RN4	1
54	RES_ARRAY_8_SMD-10K	DIGI-KEY 766-163-R10K-ND	RN3	1
55	RES_ARRAY_8_SMD-270	DIGI-KEY 766-163-R270-ND	RN5	1
56	TDK78P7200_PLCC-BASE	TDK78P7200-IH	U3	1
57	TOCTL (OCTAL T1 FRAMER)	PM4388 CABGA_128	U9-U12	4

NOTES

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