PM5351

S/UNI™ 155-TETRA

S/UNI-TETRA

S/UNI-TETRA REFERENCE DESIGN WITH WAN CLOCKING

REFERENCE DESIGN

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PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
3	January 2000	Added WAN clocking implementation suggestion. Added Design Consideration Section. Revised filtering recommendation
2	Dec 1998	Revised power filtering recommendation
1	Sept 1998	Document created.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

The PM5351 S/UNI-TETRA standard product is a Quad SATURN User Network Interface with SONET/SDH processing, ATM and Packet mapping functions at the STS-3c (STM-1) 155.52 Mbit/s rate. The S/UNI-TETRA is intended for use in equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interface (UNI), ATM Network-Network Interfaces (NNI), and Packet over Sonet (POS) interfaces. The POS interface can be used to support several packet based protocols, including the Point-to-Point Protocol (PPP). The S/UNI-TETRA may find application at either end of switch-to-switch links or switch-to-terminal links, both in public network (WAN) and private network (LAN) situations.

The S/UNI-TETRA reference design provides a physical interface implementation of a SONET/SDH line card for both ATM and POS applications. It provides four optical interfaces at OC-3 rates and a system side interface of 25MHz to 50MHz for a 16-bit wide bus. For WAN applications, this reference design provides an example implementation of a Digital PLL for satisfying Bellcore Stratum 3 Clock synchronization requirements.

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2 FEATURES

- Provides four OC-3 rate 155.52 Mbits/s SONET/SDH Physical Layer Ports
- Provides a Utopia Level 2, 50 MHz, 16-bit ATM Multi-PHY System Interface
- Provides a POS-PHY Level 2, 50 MHz, 16-bit Packet Over Sonet Multi-PHY System Interface
- Contains an on-board microcontroller to provide WAN clocking requirements related to wander transfer, holdover and long time stability when using external VCXO
- Provides Dropside Loopback for Diagnostic Purposes
- Provides a software package for demonstration and evaluation of the S/UNI-TETRA reference board

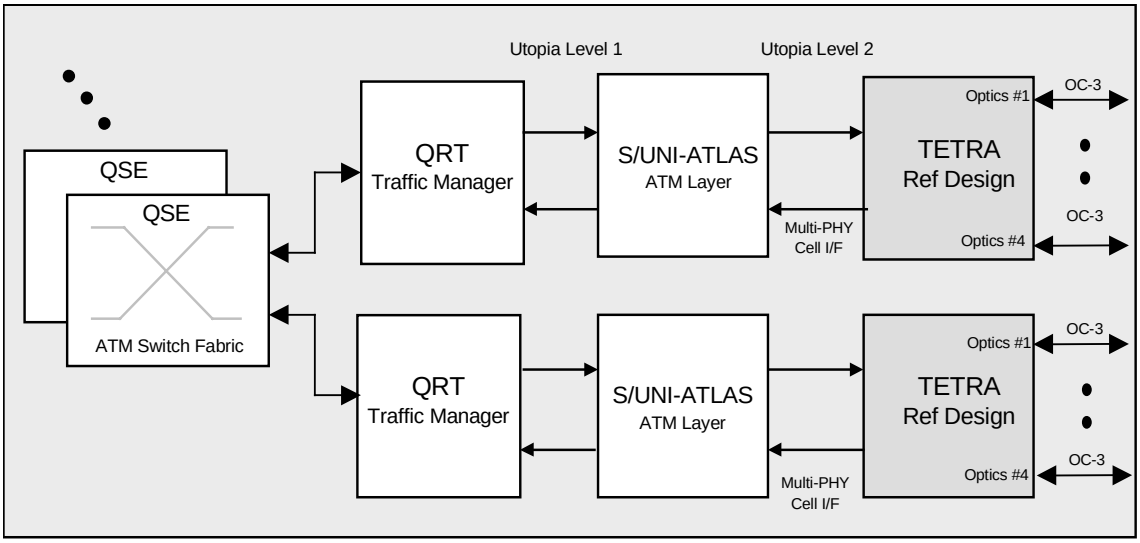
3 APPLICATIONS

The S/UNI-TETRA reference design demonstrates the physical interface implementation for both ATM or POS applications. The list below shows the networking equipment that can incorporate the S/UNI-TETRA device:

- WAN and Edge ATM switches physical Interface
- LAN switches and hubs physical Interface
- Packet switches and hubs physical interface

In an ATM application, the S/UNI-TETRA reference designs interfaces to four OC-3 rate SONET/SDH signal on the line side. On the drop side, the S/UNI-TETRA interfaces directly with ATM layer processors and switching or adaptation functions using a Utopia Level 2 compliant synchronous FIFO style interface. Figure 1 shows an example of the S/UNI-TETRA reference design in a complete ATM switching design using PMC-Sierra's ATM chipsets.

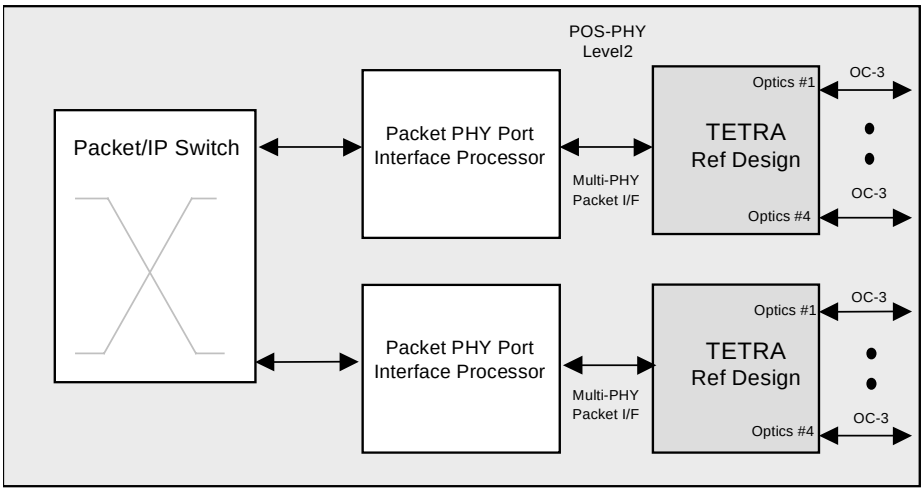
Figure 1 : S/UNI-TETRA RD with PMC-Sierra ATM Chipsets



In a Packet Over Sonet application, using PPP protocol, the S/UNI-TETRA reference design interfaces to a OC-3 rate SONET/SDH signal on the line side. On the drop side, the S/UNI-TETRA reference design interfaces directly with a PPP link layer processor using a 256 byte synchronous FIFO interface over

which packets are transferred. Figure 2 shows the S/UNI-TETRA reference design in a POS application.

Figure 2 : S/UNI-TETRA Ref Design with POS Link Layer Device



4 DESIGN OVERVIEW

The S/UNI-TETRA reference design consists of a S/UNI-TETRA device and four optical transceivers in a four port optical physical interface for either Asynchronous Transfer Mode (ATM) or Packet Over Sonet (POS) applications. The S/UNI-TETRA reference design contains an on-board microcontroller, Motorola 68332, and related WAN circuitry to perform WAN synchronization using the S/UNI-TETRA's WANS block. The dropside Loopback function is provided by an on-board FPGA. The S/UNI-TETRA reference design is capable of a maximum bandwidth of approximately 622 Mbps and can be used as an ATM or POS line card.

The S/UNI-TETRA reference design provides a dual-mode physical layer interface to upper link layer devices. For ATM application, the S/UNI-TETRA reference design supports the Utopia level 2 ATM PHY to ATM Layer specification. Since the S/UNI-TETRA is a quad PHY chip, the PHY interface can be configured as multi-PHY address polling at 50 MHz over a 16 bit bus.

For Packet over Sonet, the S/UNI-TETRA reference design supports POS-PHY level 2 standard for interfacing to a packet link layer device. The S/UNI-TETRA reference design connects to an upper POS layer device using a 16 bit wide data bus running at 50MHz. The S/UNI-TETRA supports both byte and packet level transfer modes as defined in the POS-PHY Level II specification.

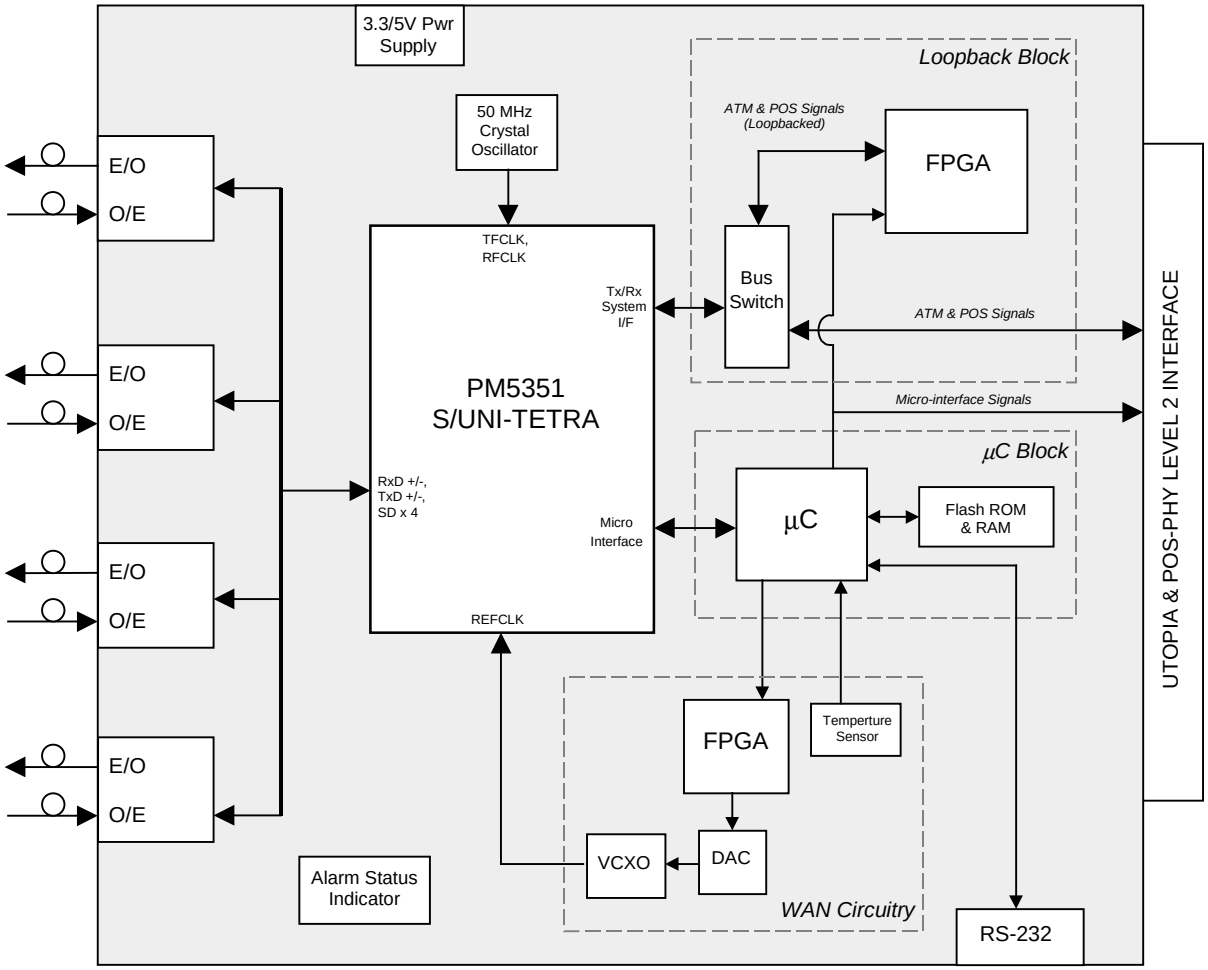
The S/UNI-TETRA reference design also implements a WAN synchronization circuit that meets Bellcore GR-253-CORE SONET Stratum 3 or lower NE clocking requirements. The WAN circuitry generates a reference clock that satisfies wander transfer, long term and holdover stability according to the Bellcore specification by utilizing the S/UNI-TETRA's WANS block.

The loopback feature allows the receive data to be looped back to the transmit stream at the drop side. This allows the evaluation of both the line side and drop side interface. An external Field Programmable Gate Array (FPGA) implements the loopback feature and provides a microprocessor interface to the 68322 microcontroller. This FPGA also provides transmit data reclocking. The FPGA reclocks the transmit data and control signals to meet the setup and hold times of the S/UNI-TETRA device.

The S/UNI-TETRA reference design can be run either as a stand-alone evaluation platform or interfaced to other S/UNI reference designs. As a stand-alone board, the S/UNI-TETRA reference design allows access to on-chip registers, performs WAN clocking function, and performs system side loopback feature for both ATM and POS. When interfaced to other reference boards, cell

and packet generation functions are provided by these external boards for further demonstration and evaluation of the S/UNI-TETRA device.

5 BLOCK DIAGRAM

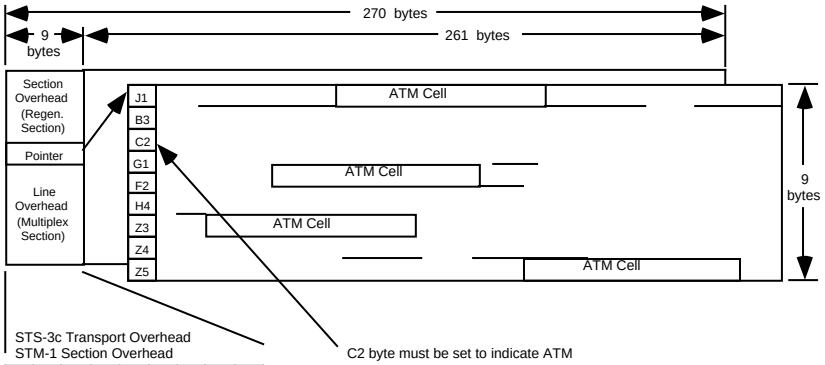


6 FUNCTIONAL DESCRIPTION

6.1 S/UNI-TETRA

The PM5351 S/UNI-TETRA SATURN User Network Interface is a monolithic integrated circuit that implements four channel SONET/SDH processing, ATM mapping and Packet over SONET mapping functions at the STS-3c (STM-1) 155.52 Mbit/s rate. Figure 3 shows the overhead of a STS-3c frame.

Figure 3 : STS-3c Frame



A1	A1	A1	A2	A2	A2	J0	Z0	Z0
B1			E1			F1		
D1			D2			D3		
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2	K1			K2		
D4			D5			D6		
D7			D8			D9		
D10			D11			D12		
S1	Z1	Z1	Z2	Z2	M1	E2		

The S/UNI-TETRA receives the SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section, line, and path overhead. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3) while accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (M1, G1) are also accumulated. The S/UNI-TETRA interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell or POS packet payload.

When used to implement an ATM UNI or NNI, the S/UNI-TETRA frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled. The ATM cells that are passed are written to a four cell FIFO buffer. The received cells are read from the FIFO using a generic 16 wide Utopia level 2 compliant datapath interface. Counts of

received ATM cell headers that are errored and uncorrectable and also those that are errored and correctable are accumulated independently for performance monitoring purposes. For the transmit stream, ATM cells are written to an internal four cell FIFO using a generic 16-bit wide datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell. The S/UNI-TETRA provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

When used to implement Packet transmission over a SONET/SDH link, the S/UNI-TETRA extracts Packet over SONET (POS) frames from the SONET/SDH synchronous payload envelope. Frames are verified for correct construction and size. The Control Escape characters are removed. The error check sequence is optionally verified for correctness and the extracted packet is placed in a received FIFO. The received packets are read from the FIFO through the drop side interface. Valid and errored packet counts are provided for performance monitoring. The S/UNI-TETRA Packet over SONET implementation is flexible enough to support several link layer protocols, including HDLC, PPP and Frame Relay. For the transmit stream, the S/UNI-TETRA inserts POS frames into the SONET/SDH synchronous payload envelope. Packets to be transmitted are written into a 256-byte FIFO through the System Interface. POS Frames are built by inserting the flags, Control Escape characters and the FCS fields. Either the CRC-CCITT or CRC-32 can be computed and added to the frame. Several counters are provided for performance monitoring.

No line rate clocks are required directly by the S/UNI-TETRA as it synthesizes the transmit clock and recovers the receive clock using a 19.44 MHz reference clock. Normally the S/UNI-TETRA outputs only a differential PECL line data (TXD+/-). Optionally, the S/UNI-TETRA can output a differential transmit line rate clock (TXC+/-). The S/UNI-TETRA also provides a WAN Synchronization controller that can be used to control an external VCXO in order to fully meet Bellcore GR-253-CORE jitter, wander, holdover and stability requirements. Details of the S/UNI-TETRA can be found in the S/UNI-TETRA datasheet, PMC-971028.

6.2 Optical Line Interface

The S/UNI-TETRA reference design provides four optical line interfaces at the 155.52 Mbit/s OC-3 rate. The line interface consists of four optical data links (ODL) and a termination scheme for the PECL signals into and out from the four S/UNI-TETRA transmit and receive signal pairs. The suggested termination scheme is discussed in the design consideration section.

In normal operation, the S/UNI-TETRA performs clock recovery and serial to parallel conversion on the incoming data stream. In a loss of signal condition, indicated on each of the four SD pins, the S/UNI-TETRA will squelch the receive data and the clock recovery unit and will switch to the reference clock (19.44MHz) to keep the recovered clock in range. This technique guarantees that the S/UNI-TETRA will generate an LOS indication when the ODL loses the incoming optical signal.

For this reference design, 3.3V ODL transceivers are used to reduce power consumption and match PECL level signals.

6.3 Microcontroller Block

The S/UNI-TETRA reference design uses the 32-bit Motorola 68332 microcontroller running at 16.7MHz as its on-board processor. The microcontroller block contains separate flash ROM and RAM for program data storage and run-time program execution. The S/UNI-TETRA registers are accessed through a 10-bit address and a 8-bit data bus microprocessor interface by the 68322.

The microcontroller can be accessed through either the RS-232 port or the Background Debugging Mode (BDM) connector on the reference board. The RS-232 port allows the access to the serial port on the 68332. The RS-232 port can be connected to a serial COM port on a PC by using a DB9 to DB9 cable. The firmware for the reference design resides in the FLASH ROM. A user can use any VT100 terminal emulation program to interface to the firmware and access the hardware on the reference board. The serial port terminal should be set to 9600 Baud, 8 data bits, no parity, and 1 stop bit.

The microcontroller also provides additional control to external adapter cards through the Utopia/POS-PHY interface connector. This allows the microcontroller to access external devices.

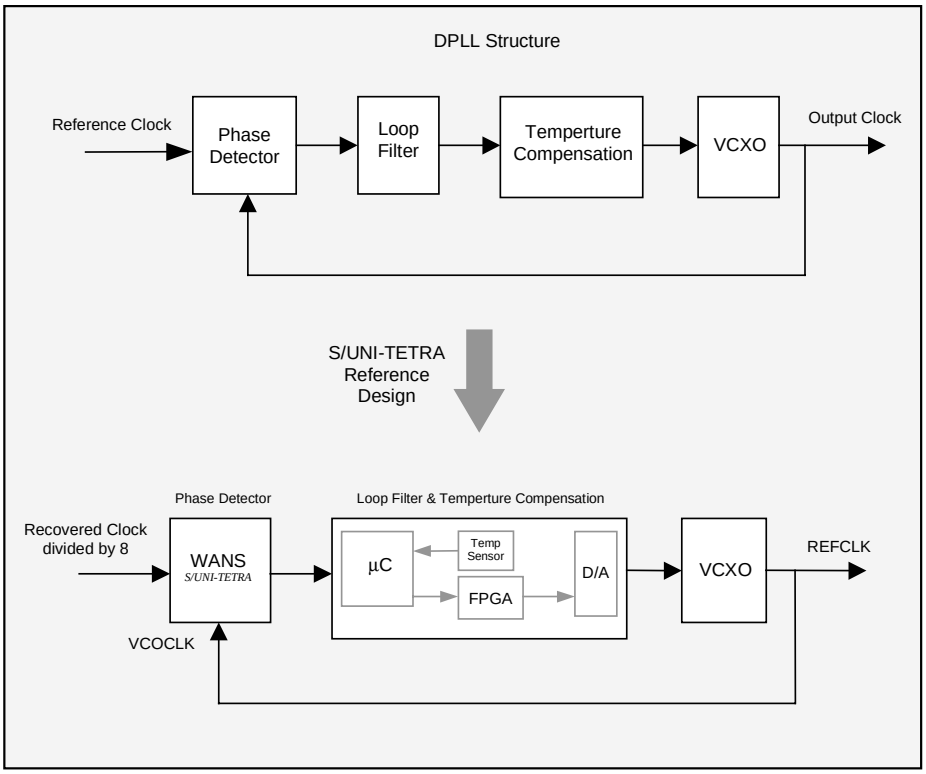
6.4 WAN Circuitry Block

Note: Due to the complexity and the nature of the design, WAN clocking is shown as a reference only and will not be supported by the PMC Applications Department

The WAN Circuitry Block consists of a VCXO, a DAC, and a temperature sensor. The WAN circuitry utilizes the S/UNI-TETRA's WANS phase comparator function block. Together with the WANS block, the S/UNI-TETRA reference design provides a complete digital PLL clocking design for generating a stratum level 3 clock that satisfies wander, jitter transfer, long term and holdover stability. It can provide a timing reference for a SONET network element (NE), such as an Add-Drop Multiplexer (ADM), a Service Access Multiplexer (SAM), or an Enterprise ro Edge Switch. The circuitry is designed to meet the requirements for the line timing mode of SONET NE as specified in GR-235-CORE Issue 2.

The general block structure of a digital PLL and the block diagram of the PLL implementation on the S/UNI-TETRA can be seen in Figure 5 below.

Figure 4 : Digital PLL Block Diagram

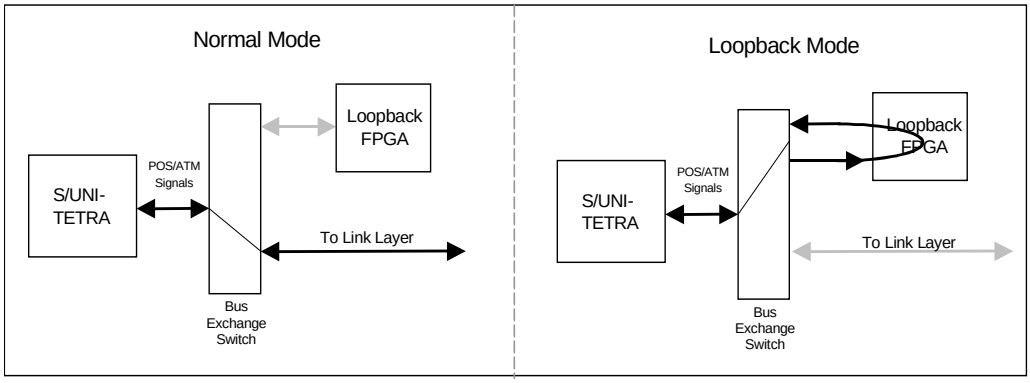


The WANS block derives a 31 bit phase value based on the phase relationship between the recovered clock, RCLK and the VCXO clock, VCOCLK. The digital PLL algorithm is performed by the FPGA on-board to reduce microprocessor load. The PLL algorithm can also be entirely implemented in software using the 68322 microcontroller. Together with the DAC and temperature sensor, the WAN circuitry block provides temperature and VCXO linearity compensation. Section 9 describes the operation of the PLL algorithm.

6.5 System Side Loopback

The Loopback block consists of a FPGA and a bus exchange switch. The Bus exchange switch allows the S/UNI-TETRA's system side to be either connected to an external FPGA for loopback functionality or to a link layer interface board. The bus exchange switch adds minimum delay and presents low capacitance and impedance to the line. The loopback setup is as shown in Figure 6 below.

Figure 5 : Loopback Diagram



In normal mode, the S/UNI-TETRA's Dropside data and control signals are connected to the system interface connector. In loopback mode, the receive data and control signals are input into and loopbacked out of the FPGA as transmit signals. The FPGA supports both ATM and POS loopbacks. The loopback block supports multi-PHY direct status addressing mode with each PHY having a separate cell/packet available signals for receive interface(DRCA/DRPA).

In loopback mode, the FPGA polls for both receive and transmit cells/packets available signals. The FPGA starts to receive and transmit cells/packets only when a PHY received data is available. This eliminates the need to implement a FIFO inside the FPGA.

6.6 External Connector

The S/UNI-TETRA reference design contains two Molex connectors for interfacing to a link layer board. The Molex connectors have been measured with a network analyzer and showed adequate results for running at 50MHz.

The first connector is used for microprocessor communication between the two microcontroller on the S/UNI-TETRA reference and an in-house motherboard. It supplies both 3.3V and 5V power supply to the S/UNI-TETRA board. It is also used for the FIFO clock signals for both the Utopia and POS-PHY interface. The second connector is used for interfacing Utopia and POS-PHY data and control signals.

Table 1 : Interface Connector One

Pin Name	Type	Pin No.	Function
SCK	Input / Output	D17	Serial Clock. Clock for the microcontroller's QSPI module
MISO	Input / Output	D19	Master In Slave Out. Serial Data for the microcontroller's QSPI module.
MOSI	Input / Output	D18	Master Out Slave In. Serial Data for the microcontroller's QSPI module.
CS_MICRO	Input / Output	D20	Chip select for communication between the microcontrollers on the S/UNI-TETRA and a motherboard.
M/S_MICRO	Input	D21	Signal to indicate if the MB1503 is the master or slave for the QSM bus. For M_MICRO = 0, the micro on the TETRA board is the master. For M_MICRO = 1, the motherboard acts as the master.
INTB_TETRA	Output	D27	Interrupt signal from the S/UNI-TETRA device
RFCLK-	Output	D35	Negative differential receive clock signal. This signal, along with RFCLK+ comprise the differential RFCLK clock signal sent across the connector. RFCLK is to be used as a reference to sample RDAT.

Pin Name	Type	Pin No.	Function
RFCLK+	Output	D36	Positive differential receive clock signal. This signal, along with RFCLK- comprise the differential RFCLK clock signal sent across the connector. RFCLK is to be used as a reference to sample RDAT.
TFCLK+	Input	D39	Positive differential transmit clock signal. This signal, along with TFCLK+ comprise the differential TFCLK clock signal sent across the connector. TFCLK is used as a reference to sample TDAT.
TFCLK-	Input	D40	Negative differential transmit clock signal. This signal, along with TFCLK- comprise the differential TFCLK clock signal sent across the connector. TFCLK is used as a reference to sample TDAT.
RMOD	Output	A39	POS-PHY: Receive Modulo This signal indicates the number of bytes carried by the RDAT bus
RVAL	Output	A40	POS-PHY: Receive Data Valid This signal indicates the validity of the receive data signal
NC	NC	A20 - A38, B17 - B30, C1 - C30, D1 - D16, D20 - D22, D28 - D34, D37, D38	Not Connected.
+ 5V	Input	A1, A2, B1, B2	+ 5 Volt supply

Pin Name	Type	Pin No.	Function
+ 3.3V	Input	A3-A9, B3-B9,	+ 3.3 Volt supply
GND	Input	A10 - A19, B10 - B16, B31 - B40, C31 - C40	Ground

Table 2 : Interface Connector Two

Pin Name	Type	Pin No.	Function
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Output	A1 D1 A2 D2 A3 D3 A4 D4 A5 D5 A6 D6 A7 D7 A8 D8	UTOPIA: Receive Cell Data Bus This bus carries the ATM cell octets that are read from the selected receive FIFO. POS-PHY: Receive Packet Data Bus This bus carries Packets that are read from the selected receive FIFO
RPRTY	Output	A9	Receive bus parity. The receive parity signal indicates the parity of the RDAT bus.

Pin Name	Type	Pin No.	Function
DRCA[1] DRCA[2] DRCA[3] DRCA[4] DRPA[1] DRPA[2] DRPA[3] DRPA[4]	Output	A10 A11 A12 A13 A10 A11 A12 A13	UTOPIA: Direct Receive Cell Available These signals indicate available cells to be transferred across the UTOPIA bus. POS-PHY: Direct Receive Packet Available These signals indicate available packet to be transferred across the POS-PHY bus.
RADDR[0] RADDR[1] RADDR[2] RADDR[3] RADDR[4]	Input	D9 D10 D11 D12 D13	Receive PHY port address. These signals are used to select the PHY port to be read from or polled.
RENB	Input	A14	Receive Multi-Phy Write Enable. The RENB signal is an active low input which is used to initiate reads from the receive FIFOs.
RCA PRPA	Output	A15 A15	UTOPIA: Receive Multi-PHY Cell Available This signal indicates an available cell during receive PHY port polling POS-PHY: Polled multi-PHY Receive Packet Available. This signal indicates when data is available in the polled receive FIFO.
RSOC RSOP	Output	D14 D14	UTOPIA: Receive Start of Cell This signal marks the start of cell on the RDAT bus. POS-PHY: Receive Start of Packet This signal marks the start of packet on the RDAT bus.
RERR	Output	D15	POS-PHY: Receive Error This signal indicates that the current packet has been aborted.
REOP	Output	D16	POS-PHY: Receive End of Packet This signal marks the end of packet on the RDAT bus
TENB	Input	A27	Utopia and POS-PHY: Transmit Multi-Phy Write Enable. The TENB signal is an active low input which is used to initiate writes to the transmit FIFOs

Pin Name	Type	Pin No.	Function
TCA	Output	D26	Utopia: Transmit cell available signal This signal is used to indicate available cell FIFO space by polled PHY ports.
PTPA		D26	POS-PHY: Polled Transmit multi-PHY Packet Available. This signal transitions to high when a programmable minimum number of bytes is available in the polled transmit FIFO.
TSOC	Input	A28	Utopia: Transmit Start of Cell The transmit start of cell signal marks the start of cell on the TDAT bus.
TSOP		A28	POS-PHY: Transmit Start of Packet This signal indicates the first word of a packet.
TADDR[0] TADDR[1] TADDR[2] TADDR[3] TADDR[4]	INPUT	D27 D28 D29 D30 D31	Transmit Address. The TADR[4:0] bus is used to select the port that is to be written to or being polled.
DTCA[1] DTCA[2] DTCA[3] DTCA[4]	Output	A29 A30 A31 A32	Utopia: Direct Transmit Cell Available These signals indicate available cells to be transferred across the UTOPIA.
DTPA[1] DTPA[2] DTPA[3] DTPA[4]		A29 A30 A31 A32	POS-PHY: Direct Transmit Packet Available These signals provide direct status indication of when some programmable number of bytes is available in the transmit FIFO.
TERR	Input	A22	POS-PHY: Transmit Error This signal indicates the current packet must be aborted.
TEOP	Input	A25	POS-PHY: Transmit End of Packet This signal marks the end of a packet on the TDAT bus.
STPA	Output	A25	POS-PHY: Selected multi-PHY Transmit Packet Available This signal transitions high when a predefined minimum number of bytes is available in the selected transmit FIFO.

Pin Name	Type	Pin No.	Function
TMOD	Input	A26	POS-PHY: Transmit Word Modulo This signal indicates the size of the current word.
TPRTY	INPUT	D32	Transmit bus parity. The transmit parity signal indicates the parity of the TDAT bus.
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	INPUT	A40 D40 A39 D39 A38 D38 A37 D37 A36 D36 A35 D35 A34 D34 A33 D33	Utopia: Transmit Cell Data Bus This bus carries the ATM cell octets that are written to the selected transmit FIFO. POS-PHY: Transmit Packet Data Bus This data bus carries the POS packet octets that are written to the selected transmit FIFO

7 DESIGN CONSIDERATIONS

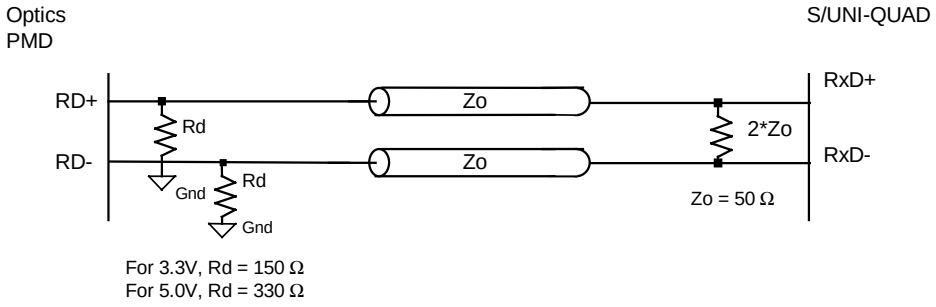
7.1 PECL INTERFACE

7.1.1 RECEIVE INPUTS

The S/UNI-TETRA's receive RxD+/- inputs are implemented as a true differential PECL receiver. The receive signals are high-speed signals and must be properly terminated to reduce reflection. Unlike previous generation S/UNI products, the S/UNI-TETRA RxD+/- pair are not self-biased to the PECL Vbb level. Given that the RxD+/- inputs have wide common mode operating voltage, the receive inputs can be directly DC-coupled from the optics.

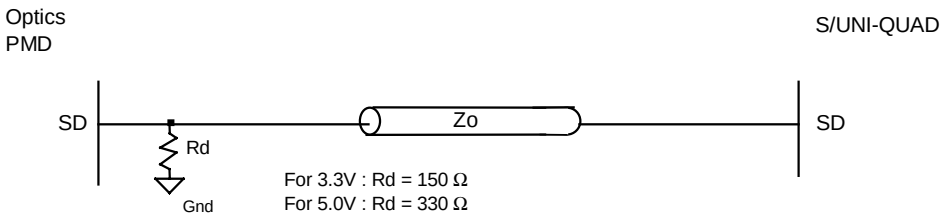
Most of the commercially avaliable optics on the market today provide PECL level RxD+/- outputs. The emitter on these PECL outputs need to be biased through a series resistor ground to provide adequate signal levels on the outputs. For 3.3V PECL drivers, a 150 Ohm series resistor is recommended. For 5V PECL drivers, a 330 Ohm series resistor is recommeded. The bias resistor location and value is shown in Figure 6. The RxD+/- differential signals require termination at the S/UNI-TETRA's input . With 50 ohm controlled impedence lines, a 100 ohm resistor connected across the RxD+/- pair can properly terminate the signal with minimum current draw.

Figure 6 : Receive RxD+/- Interface



The SD detect input can also be DC-coupled from the SD output from an Optics. Similar to the optics RxD+/-'s outputs, the optic's SD output needs a emitter biasing resistor. Since SD is a relative slow signal, termination is not required at the S/UNI-TETRA. The SD input on the S/UNI-TETRA can also be supplied from a TTL or CMOS source as long as the input signal level doesn't exceed the receiver voltage reference(3.3V or 5V).

Figure 7 : Receive SD Interface



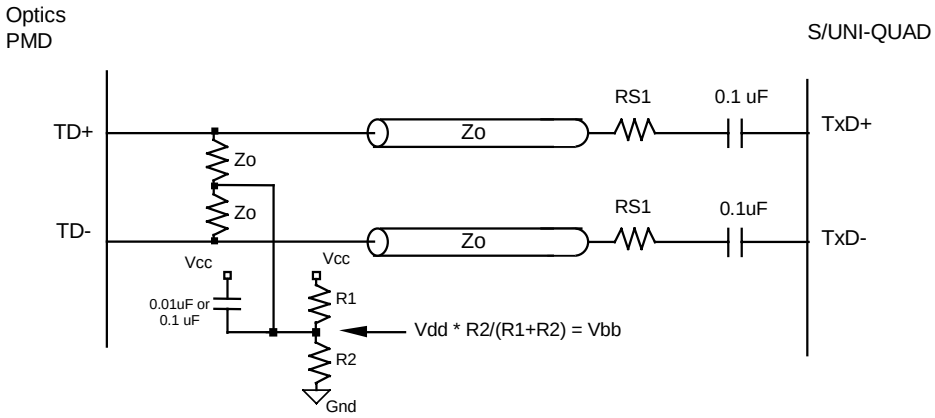
7.1.2 TRANSMIT OUTPUTS

The S/UNI-TETRA's transmit TxD+/- outputs are 3.3V CMOS rail to rail outputs. Since most of the optics have PECL level TxD+/- inputs, the TxD+/- signal from the S/UNI-TETRA needs to be converted to PECL level.

The PECL level conversion is done by first AC-coupling the TxD+/- outputs and attenuating the output voltage swing to PECL level. The PECL voltage swing is typically 800mV where as the S/UNI-TETRA outputs provide 3.3V swing. The 800mV swing can be attained by inserting a series resistor between the 50 Ohm impedance line and the AC-coupled resistor. The exact calculation of this attenuation resistor value is shown in figure 8. At the optics TxD+/- inputs, the 800mV voltage level needs to swing around the PECL bias point. For 5V PECL, the bias point is 3.7V and for 3.3V LVPECL, the bias point is 2.0V. A simple voltage divider network is shown in figure 8 for biasing the TxD+/- inputs to the PECL center point. The Vdd reference for the resistor and capacitor should be the same as the optics Vdd. Two 50 ohm resistors between the TxD+/- line and the PECL bias point provide the proper termination

The S/UNI-TETRA's transmitter and external termination circuity have been designed and throughly tested to meet Bellcore and ANSI jitter generation requirements. Using single-ended transmit output is not recommended due to duty-cycle distortion and poor jitter performance.

Figure 8 : Transmit TxD+/- Interface



Notes: Vpp is minimum input swing required by the optical PMD device.

Vbb is the switching threshold of the PMD device (typically Vdd - 1.3 volts)

Vpp is Voh - Vol (typically 800 mVolts)

Vpp = (Zo/((RS1+Rs)+Z0) * Vdd

- Vdd (S/UNI-QUAD's analog transmit power) 3.3V
- Zo (trace impedance) typically 50Ω
- Rs (TxD source impedance) typically 15-20Ω
- RS1 : ~ 158Ω

Vcc = Optics Power (5.0V or 3.3V)
For interfacing to 5.0V ODL, R1 : 237Ω , R2 : 698Ω
For interfacing to 3.3V ODL, R1 : 220Ω, R2: 330Ω

7.2 FILTERING AND DECOUPLING

High speed analog circuitry is generally sensitive to any amount of broadband noise on its power supply. The S/UNI-TETRA analog clock recovery and synthesize circuitry has been designed to meet all the stringent Bellcore/ANSI requirements on jitter generation, tolerance, and transfer. For this reason, the analog power supply rail must be well filterd and decoupled to achieve optimum jitter performance.

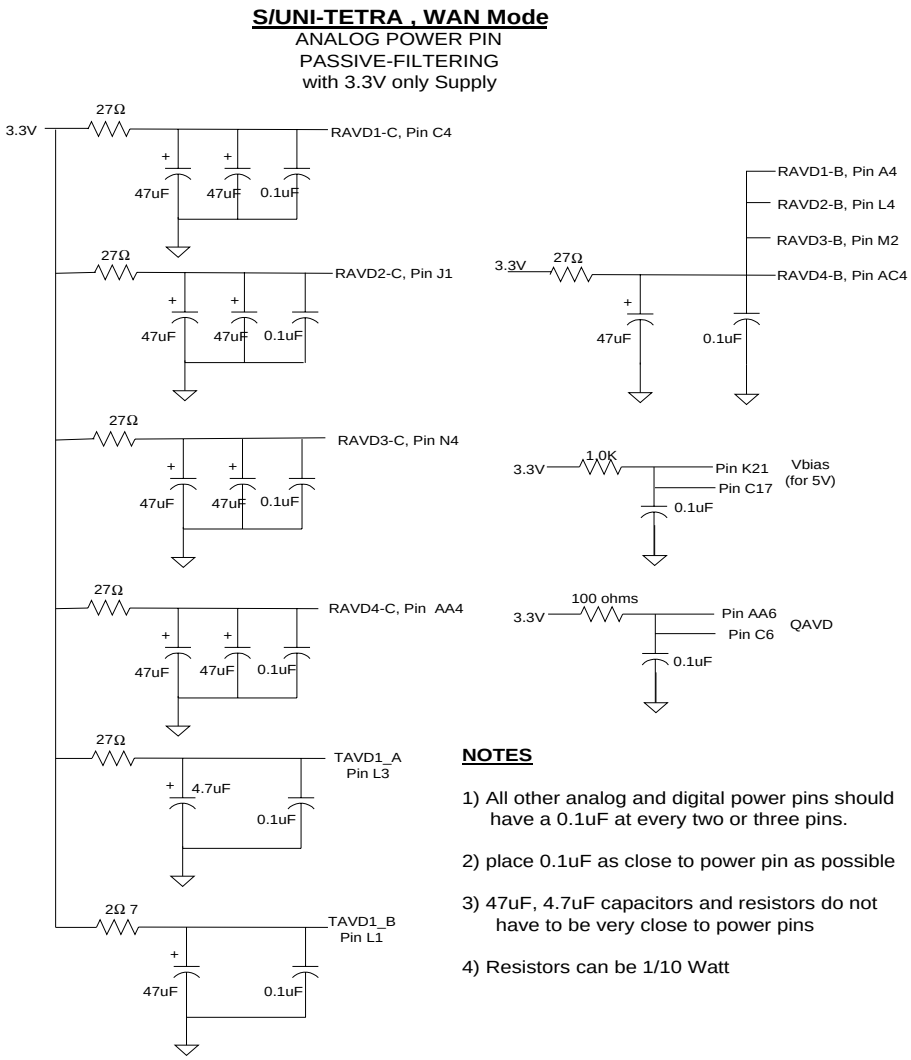
Care should be taken to reduce the noise at the CSU power pins, TAVD1_A and TAVD2_B and CRU power pins, RAVDBs and RAVDCs. Since each board design can have different noise levels on the power rail, the analog filtering circuit shown in figure 9 is recommended to ensure that the S/UNI-TETRA will be within 10% of its optimal jitter performance even when powered in a noisy environment.

The RC filtering circuitry provides a pole of around 63Hz for the purpose of filtering out low frequency noise. A single uncut ground plane can be used for all

S/UNI-TETRA board designs for both digital and analog circuitry. Ferrite beads are not recommended as a large big ferrite value will be needed to have a pole at the same frequency as an RC circuit and because LC circuity self-resonates at certain frequencies.

For the digital power pins, place 0.1µF caps near the following VDD pins: B2, B22, D9, D15, F20, J4, M20, R4, V20, Y9, Y15, AB2, and AB22. A 100 Ohm resistor should be added in series with the quiet analog pins QAVD1 and 2. This impedance will protect the device from latching-up during power up. The filtering scheme below assumes the digital and analog power pins are connected to the same 3.3V power plane since 0.1uF decoupling capacitors are shared among some digital and analog power pins.

Figure 9 : S/UNI-TETRA Analog Filtering



7.3 UNUSED INPUT PINS AND CHANNEL

All unused input pins on the S/UNI-QUAD must be tied to their inactive state. If the inputs are left floating, noise can coupled into the CMOS gates and cause the S/UNI-QUAD device to malfunction. For tying an used input to 3.3V/5V, a 4.7K Ohm pull-up resistor can be used to prevent latchup during power up.

If one of the four channels is not being used, the analog differential inputs, RxD+/-, should be also be tied to ground to avoid chattering the receiver. For any unused channel, power still needs to be supplied to the analog power pins due to S/UNI-QUAD internal power structure.

7.4 JTAG PORT

When the JTAG is unused for boundary scan, the TRSTB on the S/UNI-QUAD should be tied to RSTB. This will reset the JTAG port as the same time as system reset. TMS, TCK, and TDI should all be tied high. In addition, TCK can be optionally tied to a free-running clock to ensure that the JTAG port logic is continuously put back to the correct initial state.

7.5 ROUTING

Routing is based on the design considerations as well as manufacturability. Several suggestions are listed below:

- Allow at least 10 mil clearance between vias, traces, and pads to prevent shorts and reduce crosstalk. If possible, allow 20 mil or more clearance around vias as manufacturers may have minimum clearance requirements.

- The differential signal pairs should be of equal length so that both signals arrive at the inputs at the same time. They should also run parallel and close to one another for as long as possible so that noise will couple onto both lines and become common mode noise which is ignored by the differential inputs.

- All power and ground traces should be made as wide as possible to provide low impedance paths for the supply current as well as to allow quick noise dissipation.

- Since vias have an impedance, avoid them where possible, especially on critical traces such as TXD± and RXD±. Also where decoupling is critical, try to place capacitors at the pins (component side) and not have vias in series with the capacitors.

8 IMPLEMENTATION DESCRIPTION

The S/UNI-TETRA and S/UNI-QUAD reference designs share the same schematics as the S/UNI-TETRA/QUAD schematics mnemonic. The S/UNI-QUAD and S/UNI-TETRA devices are pin compatible and both provide SONET ATM functionality. The WANS block and Packet Over Sonet functionality on the S/UNI-TETRA/QUAD reference design schematics are implemented for the S/UNI-TETRA device. In this document, the S/UNI-TETRA schematics refer to the schematics titled “S/UNI-TETRA/QUAD reference design”.

The S/UNI-TETRA reference design schematics were captured using Cadence software, Concept Schematics Capture Tool.

8.1 ROOT DRAWING, Sheet 1

This sheet provides an overview of the major functional blocks of the S/UNI-TETRA reference design. It shows interconnections between the TETRA_BLOCK, LOOPBACK_BLOCK, SYS_INTEFACE, MICRO_BLOCK, WAN_CLOCKING, OPTICS_1, OPTICS_2, OPTICS_3, and OPTICS_4 blocks.

8.2 TETRA_BLOCK, Sheet 2 & 3

The TETRA_BLOCK shows the S/UNI-TETRA’s signals and the power circuitry. Series resistors are used to source terminate the Utopia/POS-PHY bus lines. The 51 Ohms source termination resistor together with the output impedance of the Utopia/POS-PHY bus pads matches the impedance of the trace at 75 Ohms. A 75 Ohm series end termination resistor is provided to reduce initial overshoot and undershoot due to parasitic capacitance of the input pins.

220 nF capacitors are used for the loop filter pins, CP and CN. Four LEDs are provided to display alarm status from each of the four channels in the S/UNI-TETRA. A 1K Ohm resistor is placed in series with Vbias power rail to limit the Vbias current to prevent Vbias latchup.

The digital and analog ground pins are connected to a single ground plane. Layout of the PCB must ensure that noise from the digital circuitry does not get coupled into the analog pins.

8.3 LOOPBACK_BLOCK, Sheet 4 & 5

This sheet shows the loopback function implemented for the TETRA’s Utopia/POS-PHY Level2 interface signals. P15C16212 bus exchange switches are connected to Utopia/POS-PHY signals from and to both the S/UNI-TETRA

and the loopback FPGA. These bus switches are controlled by the LB_EN signal. When in loopback, the signals driving the board connector are tied low by the resistor arrays connected through the bus switches.

The 74FCT3807 3.3V clock driver supplies receive clocks to both the S/UNI-TETRA and the board connector for the ATM/POS layer devices. The transmit clock is supplied from the board connector during regular mode. When in loopback mode, both the transmit and receive clocks are supplied by the 74FCT3807 clock driver. The FPGA operates in mixed 5/3.3V mode. The FPGA output level is at 3.3V due to Utopia/POS-PHY signals 3.3V requirement.

8.4 SYS_INTERFACE, Sheet 6 & 7

The SYS_INTERFACE block contains the board connectors and the power supply circuitry. On Sheet 5, two MOLEX 160 pins connectors are shown. Balun transformers are used to transform differential transmit and receive clock signals to single-ended signal for the S/UNI-TETRA.

Sheet 6 shows power to the reference board may be supplied either from an external power supply or through the board connectors. Solder bridges are used to select the desired power source. Fuses and transils are provided to protect the board from over-voltage and over-current.

8.5 MICRO_BLOCK, Sheet 8

The MICRO_BLOCK sheet shows the 68322 microcontroller and its external circuitry. The 68322 operates at 16.337 MHz using a 37.7KHz crystal. 1 MB (128K x 8) Flash and SRAM are provided for program storage and run-time execution. The BDM header allows the microcontroller to be ran in background debug mode for downloading the program to the FLASH and debugging purposes. The MC33064 low voltage sensing circuit put the 68322 in reset mode when the voltage supply drops below 4.5V. Three LEDs are provided for displaying board status.

8.6 WAN_CLOCKING, Sheet 9

This sheet shows the WAN clocking circuitry used to implement a local clock reference compliant to SONET Stratum 3 clock specifications. A precise power supply regulation circuitry is used for supplying power to the temperature sensor, DAC, Op-Amp, and the VCXO. The power supply regulation circuitry consists of a LMC7660 voltage doubler, and a LT1129-5 low drop voltage regulator. This ensures the power to the clocking circuitry component will have a clean and stable 5V supply.

The temperature sensor is connected to a 10-bit ADC that outputs the digitized data to the microcontroller through the SPI port. The DAC is used to supply control voltage to the VCXO. The VCXO operates nominally at 19.44 MHz. The Op-Amp is used to map 0V to 2.04V output voltage range of the DAC to the VCXO. The DAC inputs come from the FPGA.

The FPGA implements the digital filtering and the PLL algorithm for providing clocking to the board. It is controlled by the microcontroller through the data and address bus.

8.7 OPTICS_BLOCK, Sheet 10

This sheet shows the four Optical Data Link (ODL) that provides the optical to electrical (O/E) function for the S/UNI-TETRA device. The PECL signal runs on 50 Ohm controlled impedance signal lines and are properly terminated at the ODL and at the S/UNI-TETRA device.

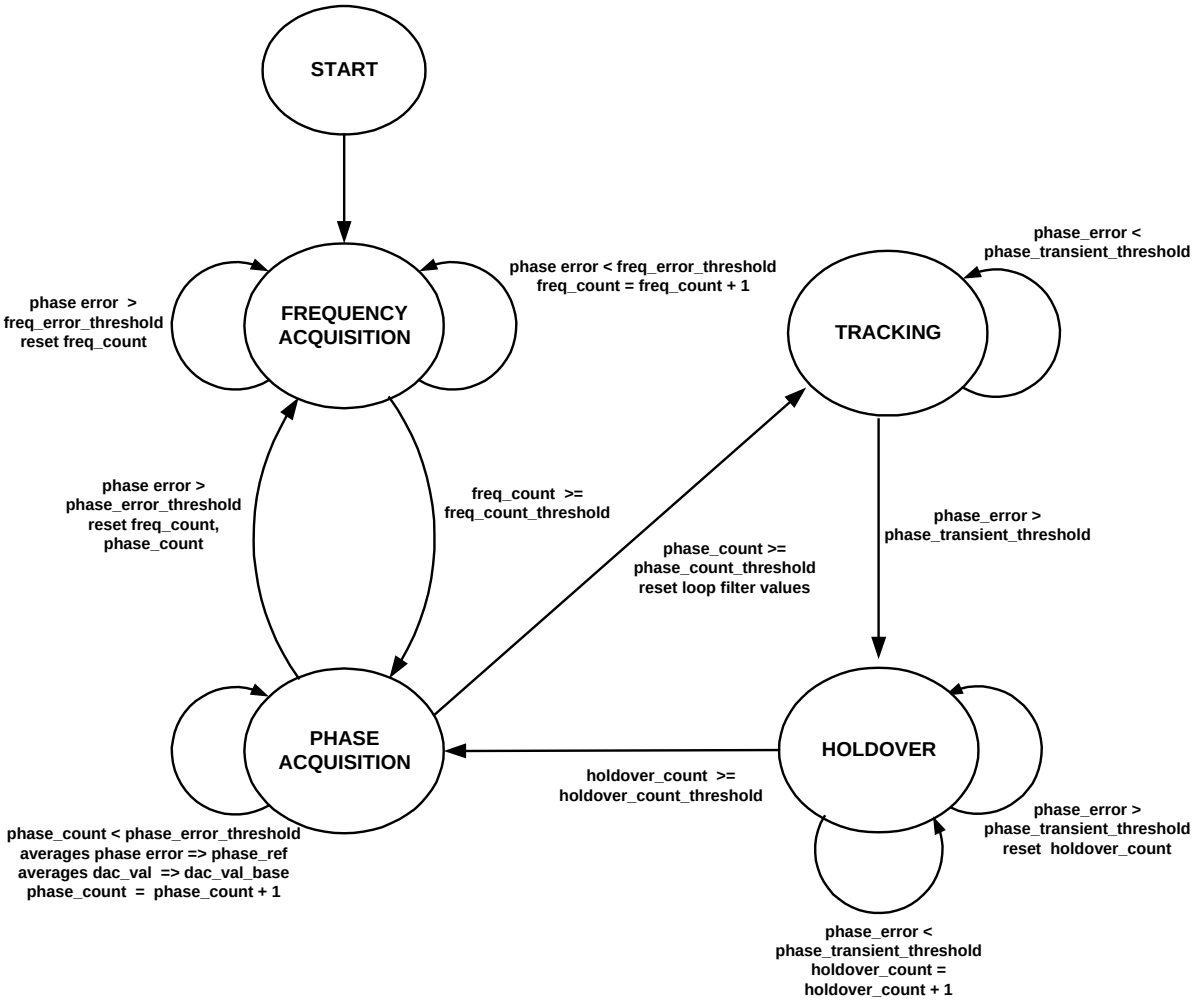
The S/UNI-TETRA device interfaces to four HP HFCT-5905 Singlemode Fiber Transceivers. The HFCT-5905 transceivers are in a 2x5 DIP package with a mini MT-RJ connector interface. The smaller footprint MT-RJ interface allows higher optical port density on a typical ATM or POS line card.

9 WAN CLOCKING PLL ALGORITHMS

This section provides an implementation suggestion for the PLL algorithm controlling the WAN clocking circuitry described in the functional description section.

Figure 10 shows the state diagram for the WAN clocking PLL algorithm. The algorithm can either be implemented in software using a microprocessor or hardware using a FPGA.

Figure 10 : PLL Algorithm State Diagram



The PLL algorithm operates within four states: Frequency acquisition, Phase acquisition, Tracking and Holdover. After initialization, the PLL algorithm enters the Frequency Acquisition State. In both the Frequency and Phase Acquisition States, the PLL adjusts the VCXO output clock to lock to the reference clock. In Frequency Acquisition State, the algorithm pulls the VCXO frequency close in with the reference clock frequency. In Phase Acquisition State, the VCXO provides a finer adjustments to the VCXO output to lock to the reference clock. Once the VCXO has locked to the reference clock, the PLL enters the Tracking state. During the Tracking state, the PLL implements a digital loop filter to maintain tracking to the reference clock. The PLL also checks to see if the reference clock is maintaining its stability. If the phase difference exceeds a preset threshold, the PLL switches to the Holdover state. The PLL can also enters the HOLDOVER states based on detected alarms (BIP-8, AIS, LOS, LOF, OOF, or SSM) or an external request. In Holdover state, the PLL keeps the VCXO output at the last locked value from the Tracking state. In the Holdover state, the PLL continues to examine the reference clock to see if it has recovered. If a good stable reference clock exists, the PLL switches back to the Phase Acquisition state. The details of each states as applicable for the TETRA WAN clocking circuity is described as below.

9.1 Frequency Acquisition

The TETRA WANS blocks implements a digital phase comparator between all four channel's recovered clocks and the REFCLK supplied by the VCXO. The results are stored in registers as a 31-bit Phase Word.

During initialization, variables are set for the operation of the PLL algorithm. To minimize the time required for the output to lock to the reference clock, a base value for the DAC, DAC_VAL_BASE, can be set to the middle of the VCXO's frequency tuning range. In Frequency Acquisition, the loop bandwidth is much wider for it to pull in the output frequency close to the reference frequency. The PLL calculates the difference between the current Phase Word and the previous Phase Word obtained from the S/UNI-TETRA WANS block and stores it as PHASE_ERROR.

Current value of the Phase Word is accumulated and averaged by the WANS block over the period specified in the WANS registers. The PHASE_ERROR is updated every 125 usec. If current Phase Word is larger than the previous one, this means that the VCXO output frequency is too high. To reduce the VCXO output frequency has to be reduced by decreasing control voltage to the DAC. The output of the DAC is buffered through the inverting Op-amp, serving as a voltage level shifter as well. If the current Phase Word is smaller than the previous one, this implies that the VCXO output frequency is too low. The VCXO frequency can be adjusted by increasing the control voltage to the VCXO.

The loop operation implemented in the Frequency Acquisition State performs frequency lock, not a phase lock because it uses phase-detector hardware as a frequency discriminator. The loop is sensitive to large frequency offsets between the VCXO and reference frequencies. For small frequency offsets, the loop is not very sensitive. When the frequency offset is smaller than the predefined threshold (FREQ_ERROR_THRESHOLD) for a predefined number of times (FREQ_COUNT_THRESHOLD), the PLL switches to the phase acquisition state.

9.2 Phase Acquisition

In Phase Acqusition State, the PLL acquires two parameters for the Tracking State. The two parameters are DAC_VAL_BASE and PHASE_REFERENCE.

DAC_VAL_BASE is obtained by averaging the DAC_VAL sent to the DAC while the PLL in the Phase Acquisition State. PHASE_REFERNECE is the average value of the Phase Word during phase acquistion. Samples of the values are taken at the same rate as in the frequency acquistion at 125us. The number of values to be averaged is shown as PHASE_COUNT_THRESHOLD. A larger number of samples improves the averaged value but requires a longer time to determine.

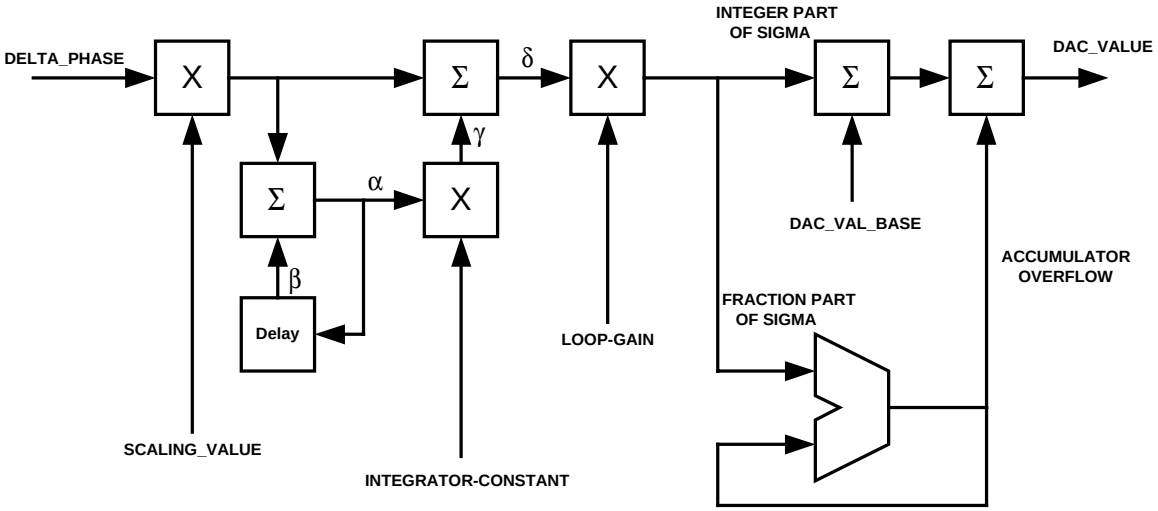
During Phase Acquisition, if the absolute value of the PHASE_ERROR exceeds PHASE_ERROR_THRESHOLD, the PLL switches back to Frequency Acquisition State. The PHASE_COUNT is reset when this occurs. The PLL enteres Tracking State when the PHASE_COUNT reaches PHASE_COUNT_THRESHOLD.

9.3 Tracking

The PLL performs phase locking and reference filtering in tracking state using a digital loop filter. The block digram for the digital loop filter is shown in figure 11.

In the tracking state, the PLL calculates the difference between the PHASE_REFERENCE derived in the Phase Acquisition State and new PHASE WORD from the TETRA's WANS block and stores as DELTA_PHASE. The loop filter is implemented as a lead-lag filter structure. The filter consists of a perfect integrator added with the scaled direct path value. The input to the loop filter, DELTA_PHASE, is scaled by the preassigned SCALING_VALUE. The ratio of the perfect accumulator path and the direct path transfer function determine the position of the transmission zero. The positional change of this transmission zero can be achieved by setting different values for the Integrator_Constant parameter.

Figure 11 : Loop Filter Block Diagram



In the lead-lag part of the filter, the value of DELTA_PHASE is added to a previous sum β and the total is stored in α. The value α is then used for the next iteration of a new α calculation. The integrator output, α, is muliplied with the INTEGRATOR_CONST by right shifting the α value by the amount specified in INTEGRATOR_CONST to obtain γ. To simply the multiplication, the INTEGRATOR_CONST is approximated by an integer value, Ki. The deriviation of Ki is shown in appendix A. Since right shifting will remove information from the α output, the DELTA_PHASE value is amplified at the input by left shifting it by the amount specified in SCALED_VALUE. All the digital values are stored as 32 bit values.

Next, the value of γ is added to the scaled value of DELTA_PHASE in order to compensate the open-loop phase. One inherent problem with this implementation is that there are two perfect integrators presented in this PLL, one in the VCXO and the other resulting from the summing of β and DELTA_PHASE. This can make the PLL unstable at various frequencies. To make the loop more stable, the effect of the second integrator formed by the sum of β and DELTA_PHASE must be minimized. This is accomplished by dividing α (right shifting) by INTEGRATOR_CONST and adding it to the DELTA_PHASE, making the effect of the second integrator only evident at very, very low frequencies. These frequencies are defined by the time required for α to accumulate to a value in the same magnitude as DELTA_PHASE. The sampling time and value of INTEGRATOR_CONST futher define the range of frequencies over which two perfect integrators exist in the loop. Above these frequencies the

loop contains only one perfect integrator as a result fo the VCXO. The sum of the scaled value of DELTA_PHASE and γ produce the value δ, which is further adjusted to result in a specific open-loop gain crossing of the 0 dB value.

The loop gain can be adjusted by setting values for LOOP_GAIN. The loop gain allows fine tuning and adjusting of the close loop transfer function. The VCXO sensitivity is the only analog value in this PLL calculation. Therefore, it allows us to accurately predict the behavior of the PLL behavior for a wide range of termperature, independent of the spread of individual VCXO sensitivity. Different batches of oscillators were tested over a wide temperature range, and it was noticed that a frequency sensitivity (Δfrequency/Δcontrol-voltage) is limited to +/-10%. A +/-20% margin is used in the calculation to provide a safety margin. The DAC temperature sensitivity is also included in this calculation. For information about PLL calculation, please refer to Appendix A.

The loop gain is adjusted by left shifting the δ value by the amount of specified in LOOP_GAIN. The idea is to create a 32 bit value word that when split into two 16 bits words, it can be used for controlloing the VCXO output. The higher word of the 32 bit long word is added with DAC_VAL_BASE as the DAC_VALUE for controlling the VCXO. PHASE_REF and DAC_VAL_BASE defined the initial condition for the behaviour of the PLL in the Tracking State. The PLL stays locked to this defined condition when in tracking.

The lower word of the 32 bit long word is passed to the Numeric Control Oscillator (NCO) routine. The lower word is masked since only the 5 most significant bits are used. The NCO routine asserts accumulator overflow bit when the accumulator overflows. The accumulator overflow bit is added to the DAC_VALUE sent to the DAC. The overflow value is used for dithering the DAC_VALUE. This process improves the accuracy of a 12 bit DAC. The output of the DAC is then filtered through a low-pass filter to obtain an optimum averaged value. The dithering allows the 12-bit DAC to improve the accuracy to the accuracy of a 17-bit DAC.

9.4 Holdover

The holdover mode is entered when excessive phase variations are detected, faults being declared, or a external request. When entering the Holdover State, the DAC_VAL_BASE will be added to the last upper word from the direct path and store as the new DAC_VAL_BASE. This value will stay as the DAC control voltage in the Holdover State. To ensure that the phase transients generated by switching to holdover does not exceed the maximum defined in the Bellcore GR-253-CORE specification, the actual phase transients are limited by the algorithm. The MTIE specification for the phase transient when entering holdover is:

Table 3 : Phase Transient MTIE specification

Observation time S (in seconds)	MTIE (nanoseconds)
S<0.014	N/A
0.014<S<0.5	7.6+(885 x S)
0.5 <S< 2.33	300+(300 x S)
2.33 < S < 64	884+(50 x S)
S > 64	N/A

In addition, there is a requirement that the initial frequency offset be less than 0.05 ppm, measured during the first minute after the 64th second.

The frequency drift rate shall be less than 5.8×10^{-6} ppm/sec. It is defined as the fractional frequency difference over the time period. The fractional frequency offset under varying temperature conditions shall be less than 4.1 ppm.

MTIE linearly increasing with observation time indicates the maximum frequency difference between an ideal clock and the observed clock.

To evaluate what relative frequency offset produces a specific MTIE value for a given observation time, we can use the following equations

$$\int_0^S \Delta\text{freq} \bullet dt = \Delta\Phi$$

$$\frac{1}{f_0} \bullet \int_0^S \Delta\text{freq} \bullet dt = \frac{\Delta\Phi}{f_0}$$

$$\Delta\text{Freq} \bullet S \bullet 10^{-6} \bullet 10^{9} = \text{MTIE}$$

In this expression, the observation time, S, is in units of seconds; MTIE is in nanoseconds; and relative frequency offset is in ppm.

Using this formula, we can calculate that to meet the GR-253-CORE requirement, the fractional frequency offset (in ppm) must be: less than 0.900 ppm for an observation time between 0.014 seconds and 0.5 seconds; less than 0.429 ppm for an observation time between 0.5 seconds and 2.33 seconds; and less than 0.064 ppm for an observation time between 2.33 seconds and 64 seconds.

The WAN synchronization PLL can change the DAC value once every 125 ms. Any phase or frequency change of the input reference clock is accumulated by the algorithm during this time and does not cause any change in the VCXO. For the current implementation with a VCXO sensitivity of approximately:

$$K_{vcxo} = \frac{8000}{3.2} Hz/V$$

and using a 12-bit DAC with DAC sensitivity of:

$$K_{DAC} = \frac{3.2\ V}{4096} / quant$$

Therefore, a single quantization step change in the DAC will create a frequency offset of approximately 2 Hz, or equivalently 0.038 ppm. If the software restricts the changes in the DAC value to a one DAC-step maximum, then even in the case of a reference clock failure and a total failure in all other methods to detect this signal fault, the VCXO will not move faster than 0.050 ppm. This is well below the limit of the GR-253-CORE specification.

Once in the holdover mode, the circuit monitors ambient temperature changes. The LM50 temperture sensor sensitivity is 10 mV/°C. The VCXO change with temperature is lower than +/-0.3 ppm/°C, so storing compensation values for the DAC in increments of 0.5°C is sufficient. The program monitors the change in temperature and calculates the correction to be added to DAC_VAL.

Finally, while in holdover, if an eligible reference source is detected, the algorithm will start the acquisition to that new source by entering the Phase Acquisition State. This process consists of the determining the new PHASE_REFERENCE value, and flushing out all accumulated values during the previous lock. Only the current DAC_VAL_BASE is kept. This method is also very useful in reducing the phase buildout during phase transients. If a phase transient is captured, then the unit will enter holdover, stay in holdover for 2 seconds and then recapture the new phase. This eliminates tracking sudden phase jumps.

10 SCHEMATICS

10.1 Bill of Materials

Table 4 : Major Components List

Ref. No	Component Description	Package Type	Quantity
U16	PMC-Sierra, Inc. PM5351 S/UNI-TETRA	SBGA304	1
U2-U5	Hewlett Packard Co. HFCT-5905	2x5 DIP Style	4
U7	National Semiconductor LM50	SOT23	1
U8	Linear Technology LTC1257	SOIC8	1
U9	National Semiconductor LMC6482	SOIC8	1
U11	National Semiconductor LMC7660 Switched Capacitor Voltage Converter	SOIC8	1
U12	Motorola MC33064	SOIC8	1
U13, U14, U20-U23	Pericom PI5C16212	TSSOP 54	6
U15	Pericom 74FCT807	SOIC20	1
U17	Motorola MC68332	PQFP 100	1
U18	Actel 42MX-09-PL84	PLCC84	1
U28	Xilinx 4020XL	PQ160	1

Ref. No	Component Description	Package Type	Quantity
U24	Atmel AT29C010A	TSOP 32	1
U25	Cypress CY62128	TSOP 32	1
U26	Linear Technology LT1181A	SOIC16	1
U27	Linear Technology LT1121CST-3.3	SOT223	1
Y1	MMD 50.00 MHz 100 ppm	4 Pins	1
Y2	For VXCO Raltron VC7220A-LZ-30-19.440-PMC For Crystal Oscillator MMD 19.44 MHz Crystal Oscillator 50 ppm	4 pin	1
D1	SGS-Thomson SMLVT3V3	SMB	1

REVISIONS				
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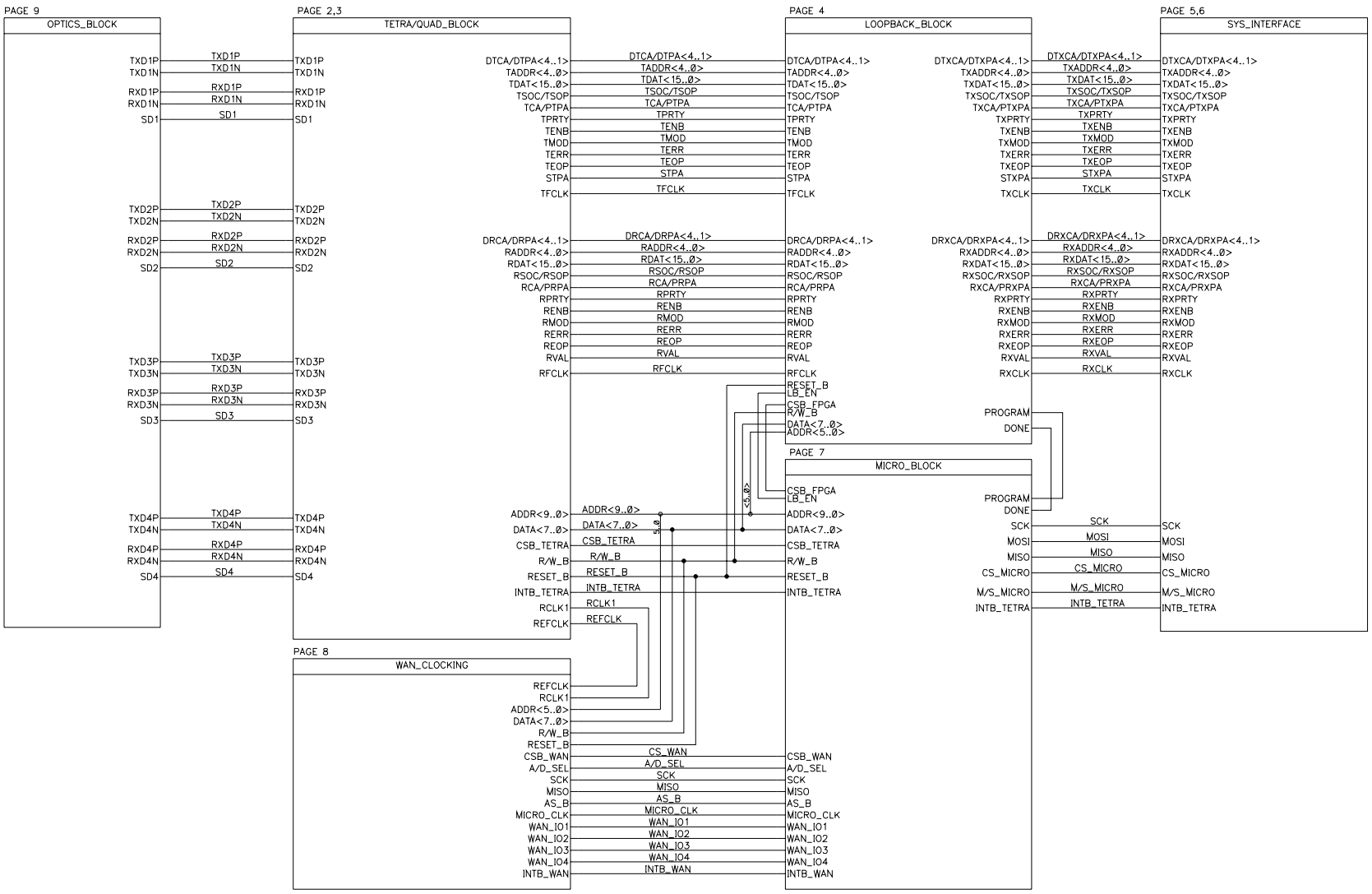

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PMC-Sierra, Inc.

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ENGINEER: PMC-SIERRA EC	PAGE: 1 OF 10

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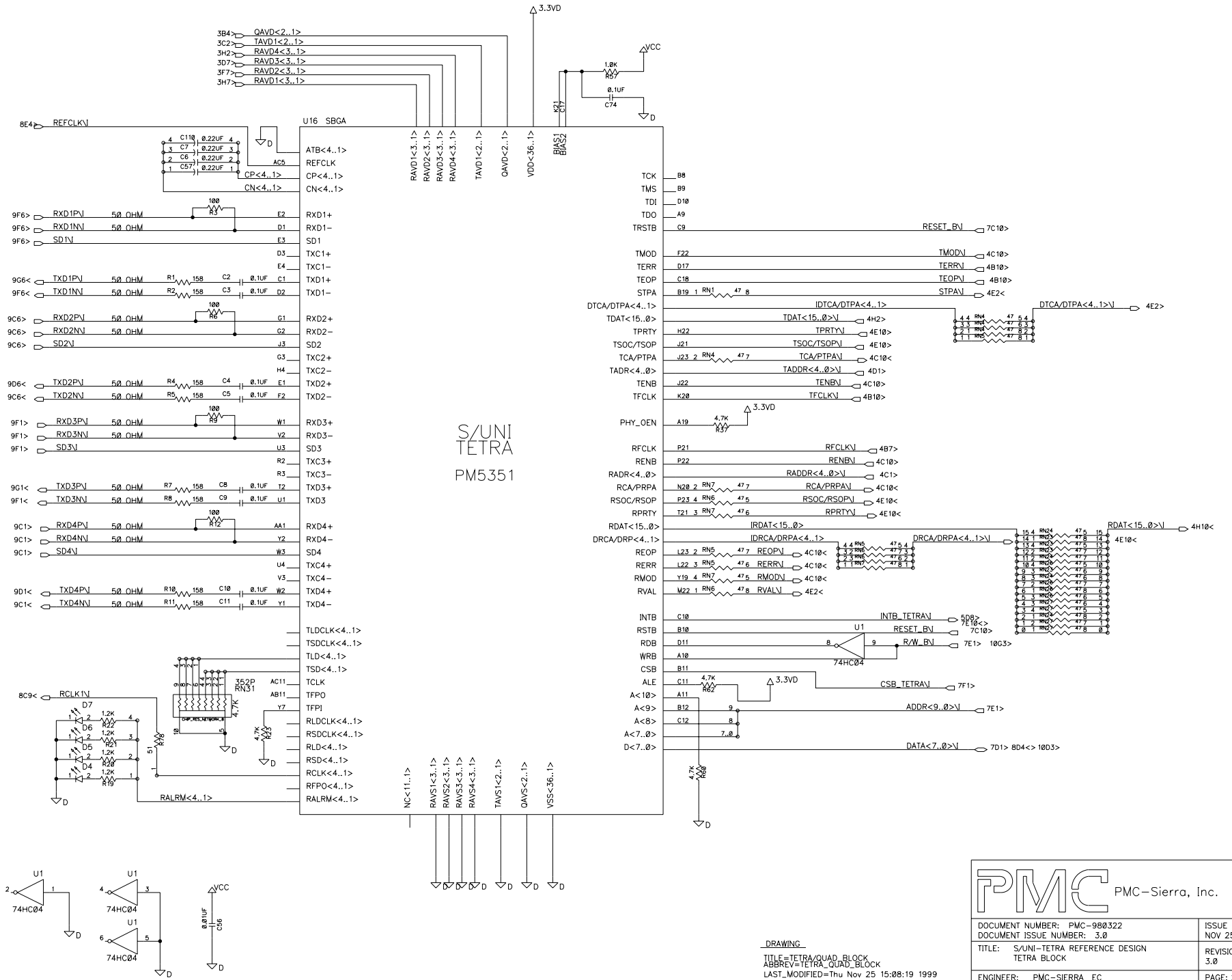

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PMC-Sierra, Inc.

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TITLE: S/UNI-TETRA REFERENCE DESIGN TETRA BLOCK	REVISION NUMBER: 3.0
ENGINEER: PMC-SIERRA EC	PAGE: 2 OF 10

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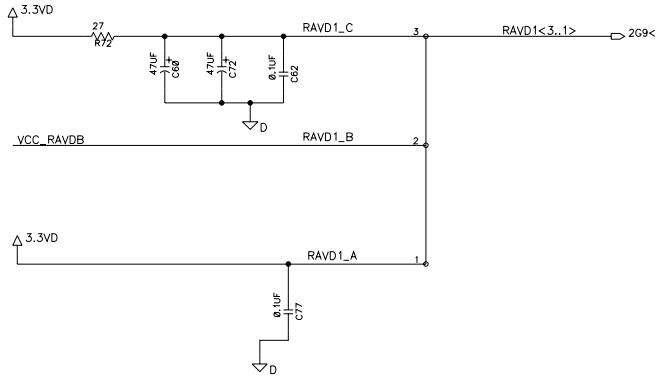

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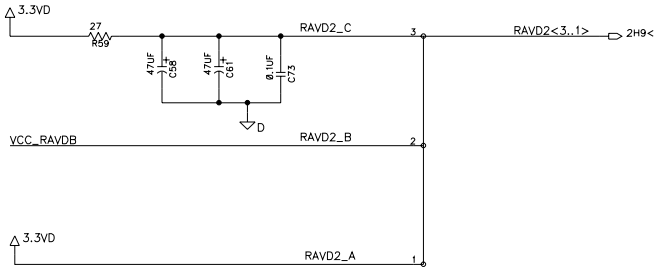

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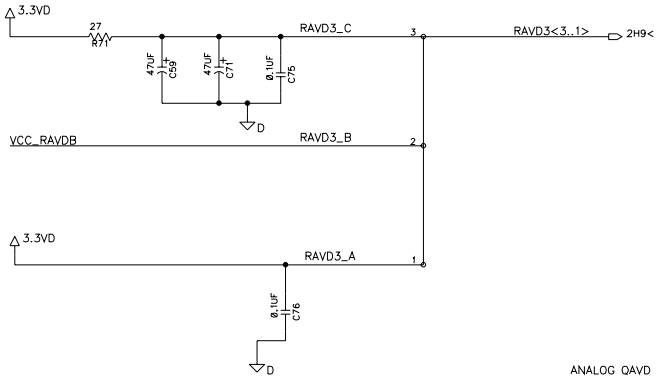

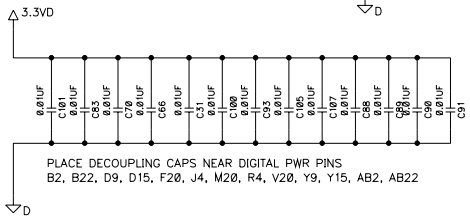

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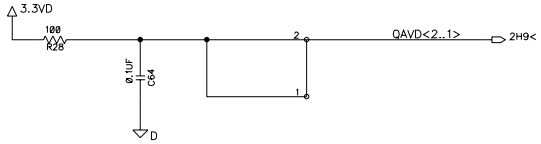

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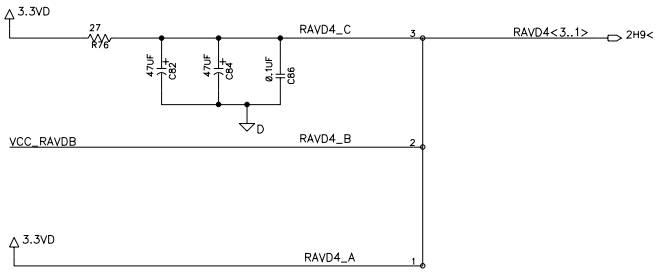
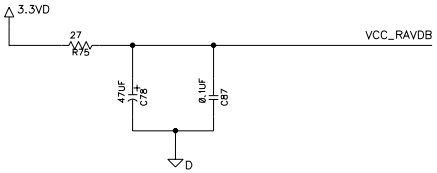
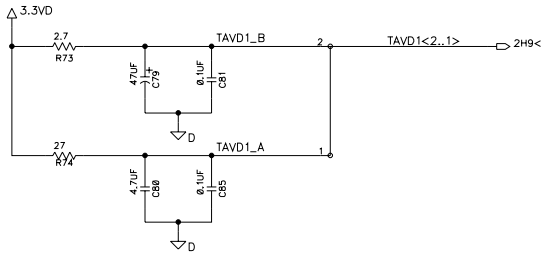




ANALOG TRANSMIT



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PMC-Sierra, Inc.

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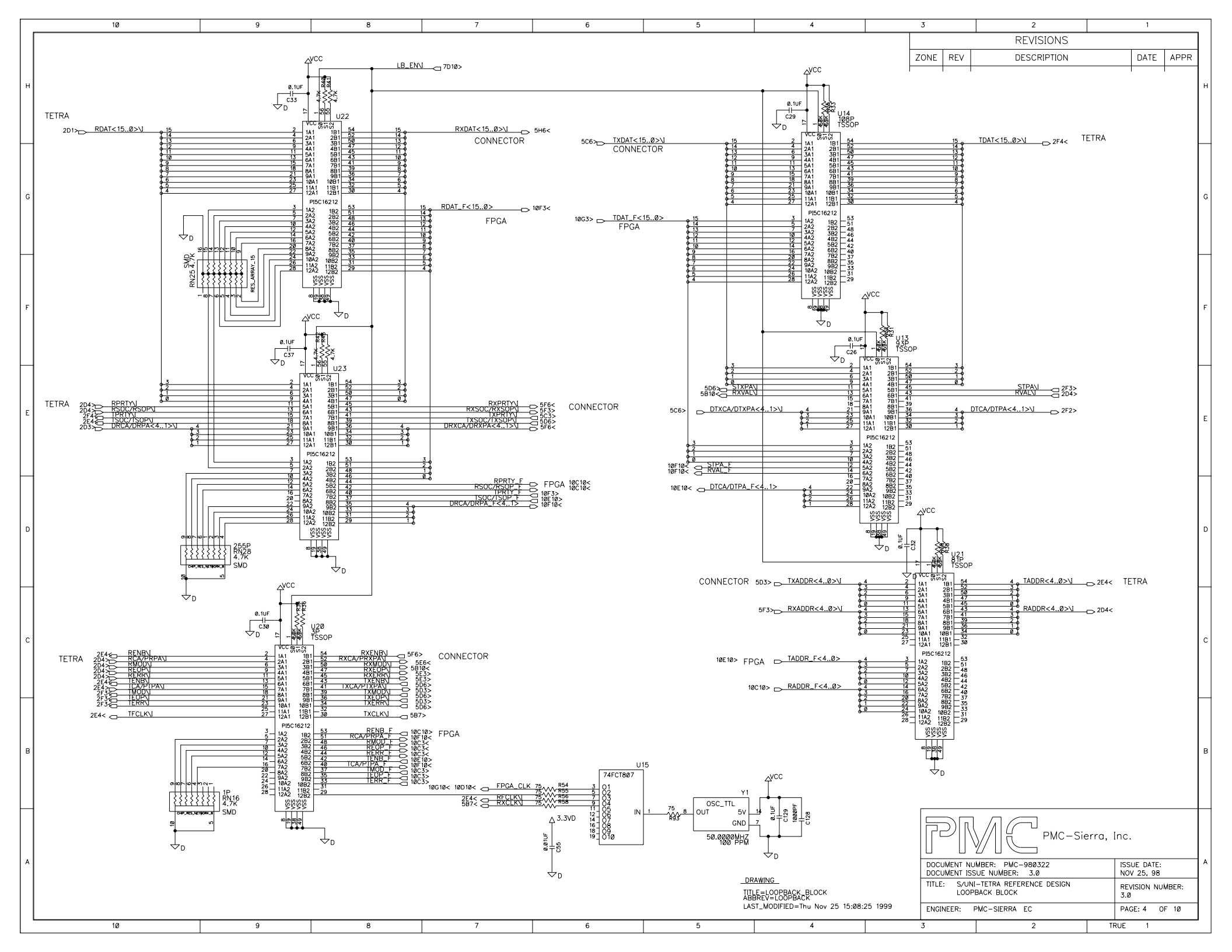
ENGINEER: PMC-SIERRA EC	PAGE: 3 OF 10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ZONE | REV | DESCRIPTION | DATE | APPR
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100 PPM
3.3VD
LB_EN\
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2D1>
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5C6>
10G3>
2F4<
2F3<
2D4<
2F2>
5D6>
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ISSUE DATE: NOV 25, 98
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REVISION NUMBER: 3.0
ENGINEER: PMC-SIERRA EC
PAGE: 4 OF 10

REVISIONS				
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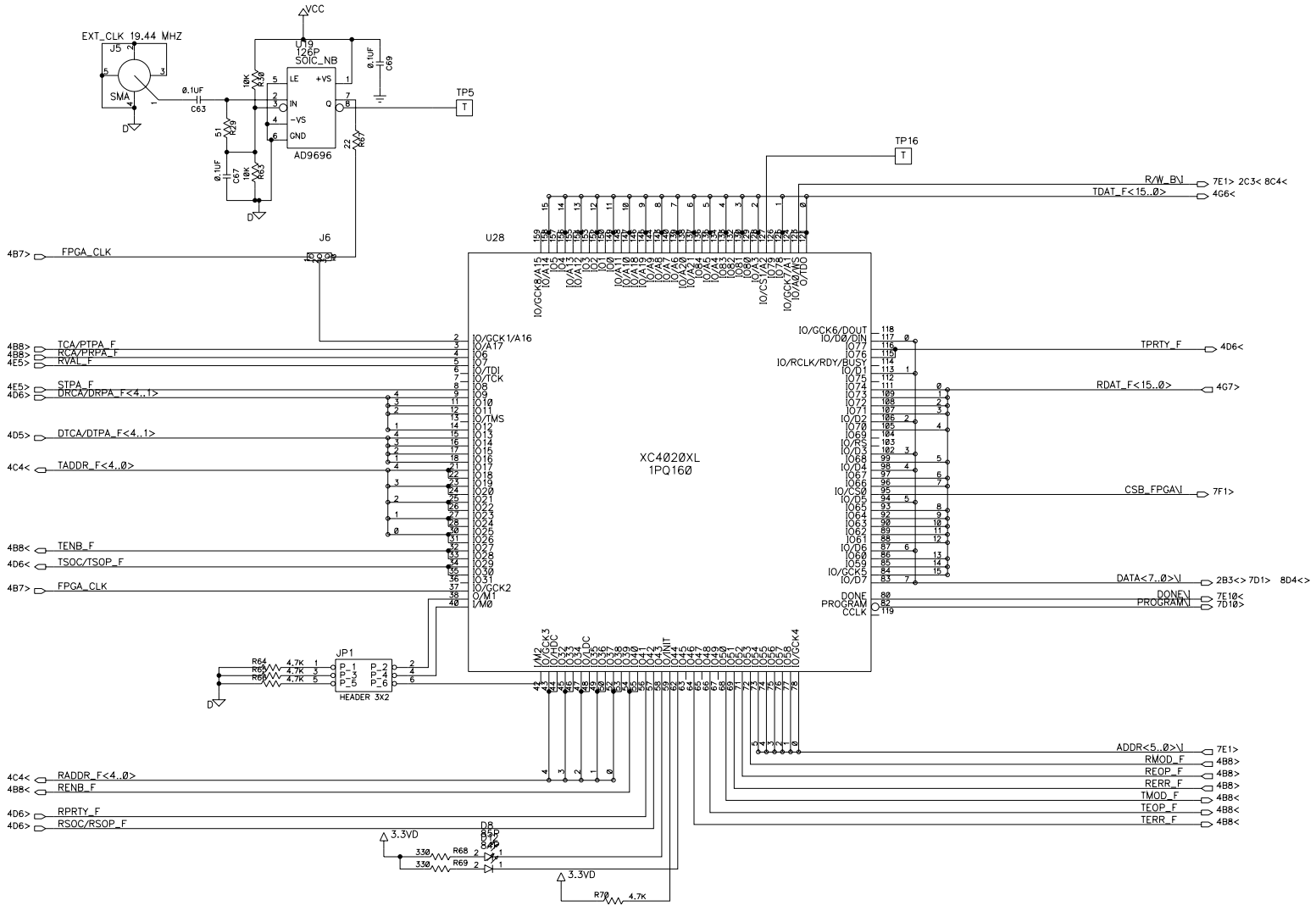

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TITLE: S/UNI-TETRA REFERENCE DESIGN LOOPBACK BLOCK	REVISION NUMBER: 3.0
ENGINEER: PMC-SIERRA EC	PAGE: 5 OF 10

REVISIONS				
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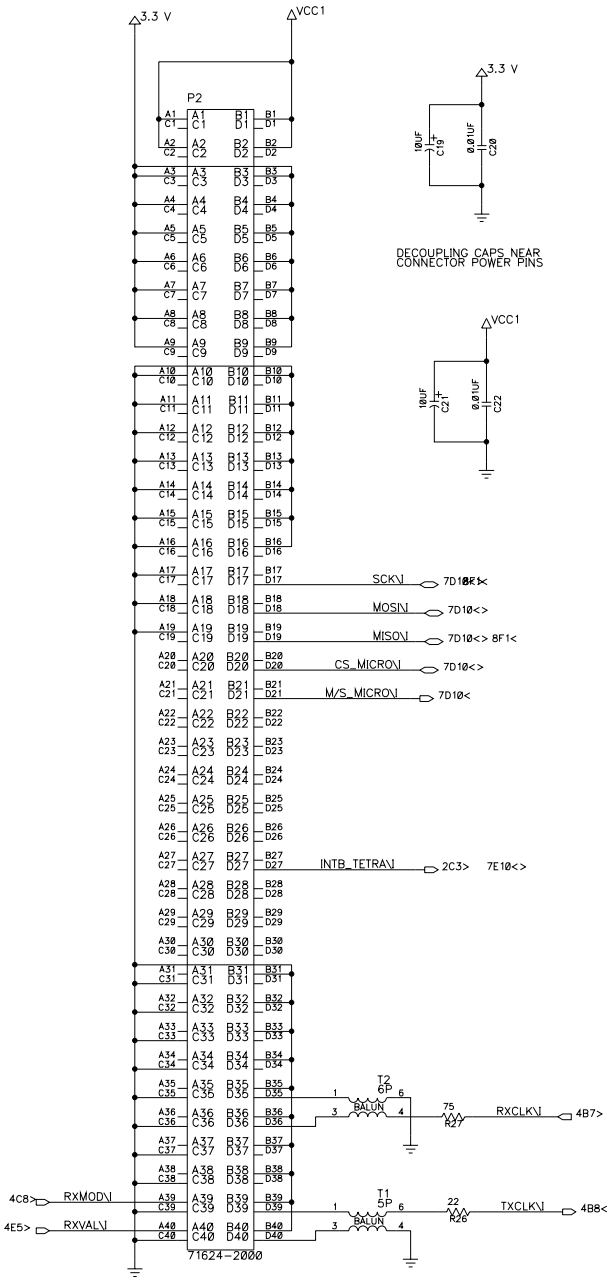

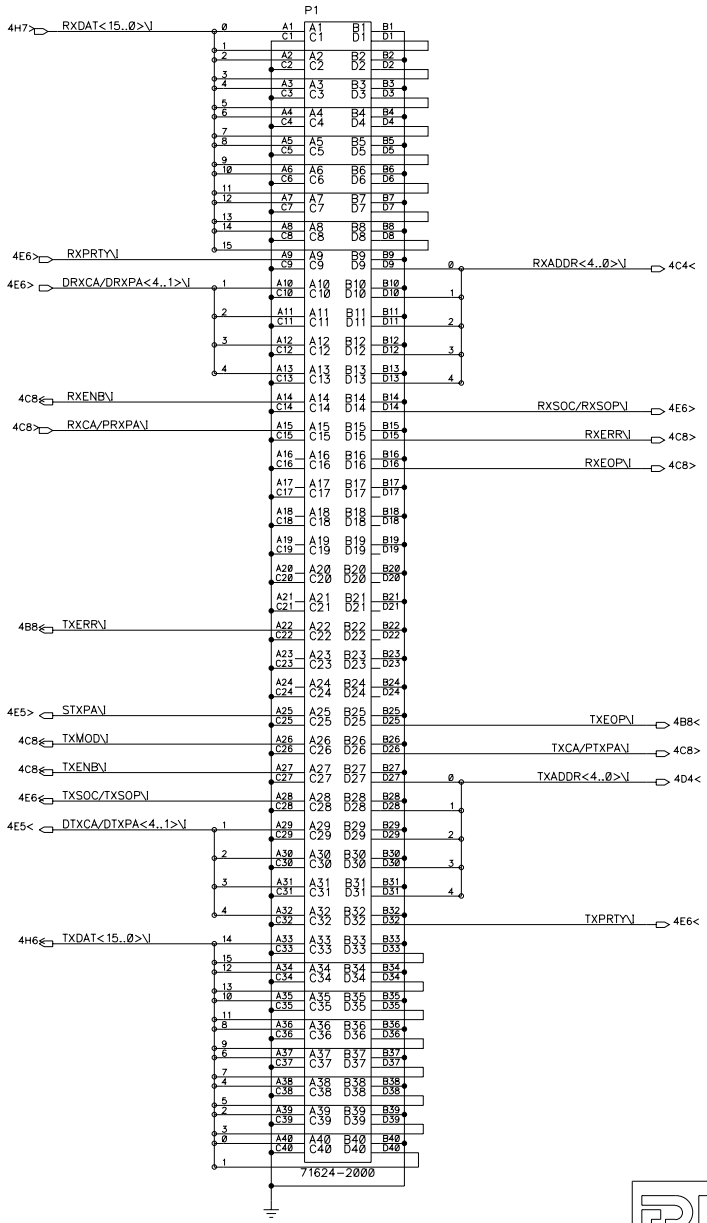

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PMC-Sierra, Inc.

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TITLE: S/UNI-TETRA REFERENCE DESIGN SYSTEM INTERFACE	REVISION NUMBER: 3.0
ENGINEER: PMC-SIERRA EC	PAGE: 6 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

ONLY ONE SET OF SOLDER BRIDGES
CONNECTED AT ANY TIME

PWR FROM EXTERNAL SUPPLY

J3
+3.3V
GND
+5V

F1 4.000A
F2 2.000A

SB1 SOLDER_BRIDGE
SB2 SOLDER_BRIDGE
SB3 SOLDER_BRIDGE
SB4 SOLDER_BRIDGE

VCC
3.3VD

D11 SMD 1W 6.2V
C14 68UF
D10 34P 270 R26
D1 80P SMLV33V3
C1 68UF
D9 33P 270 R24

D

PWR FROM MOTHERBD CONNECTOR

VCC1
F3 2.000A
SB5 SOLDER_BRIDGE
SB6 SOLDER_BRIDGE

3.3 V
F4 4.000A
SB8 SOLDER_BRIDGE
SB7 SOLDER_BRIDGE

3.3VD
TP2 T 3.3V

VCC
TP15 T 5V

TP13 T GND
TP10 T GND
TP11 T GND
TP14 T GND
TP6 T GND
TP12 T GND

TP3 T GND
TP4 T GND
TP7 T GND
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TP8 T GND
TP1 T GND

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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980322 DOCUMENT ISSUE NUMBER: 3.0	ISSUE DATE: NOV 25, 98
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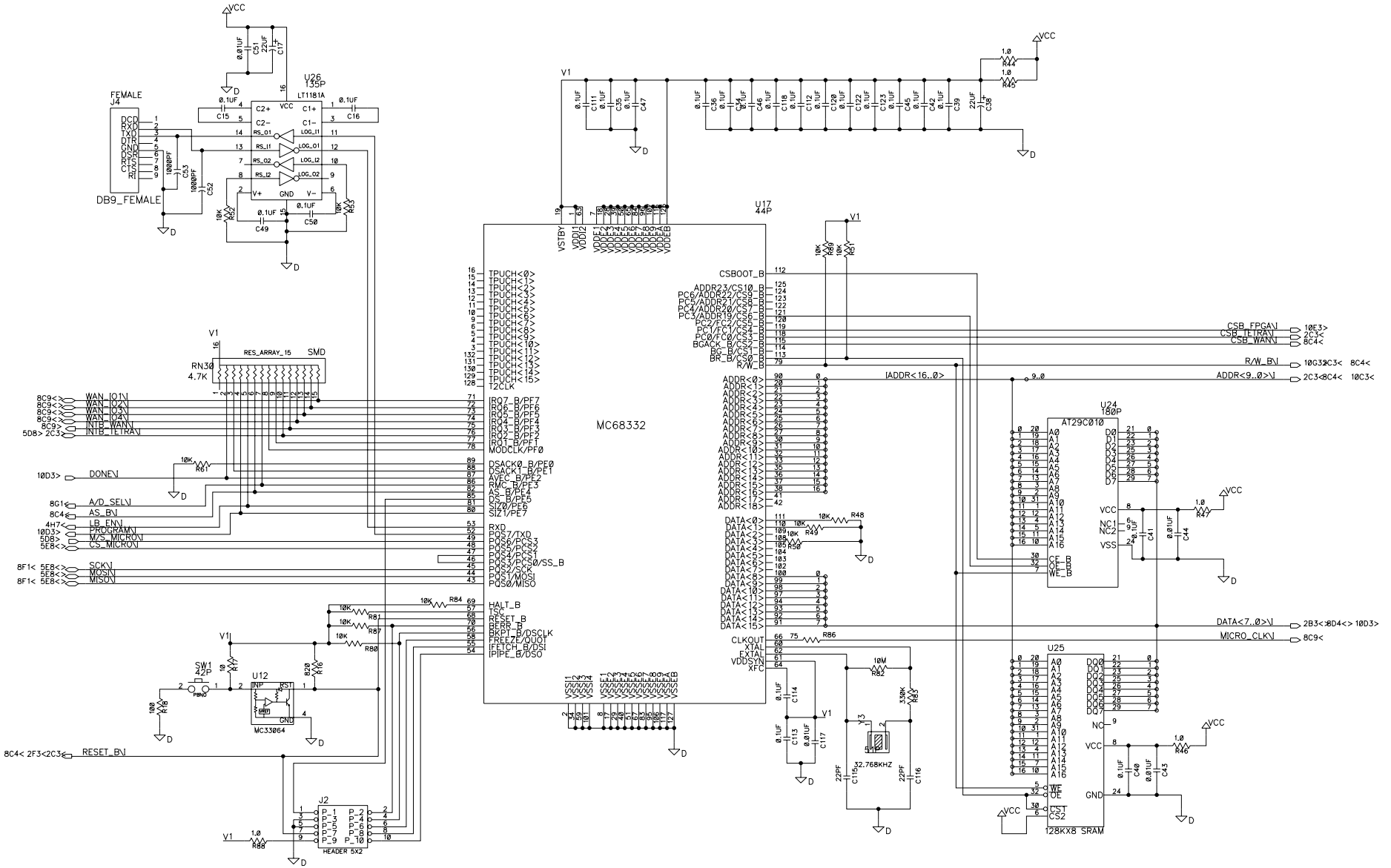
ENGINEER: PMC-SIERRA EC	PAGE: 7 OF 10



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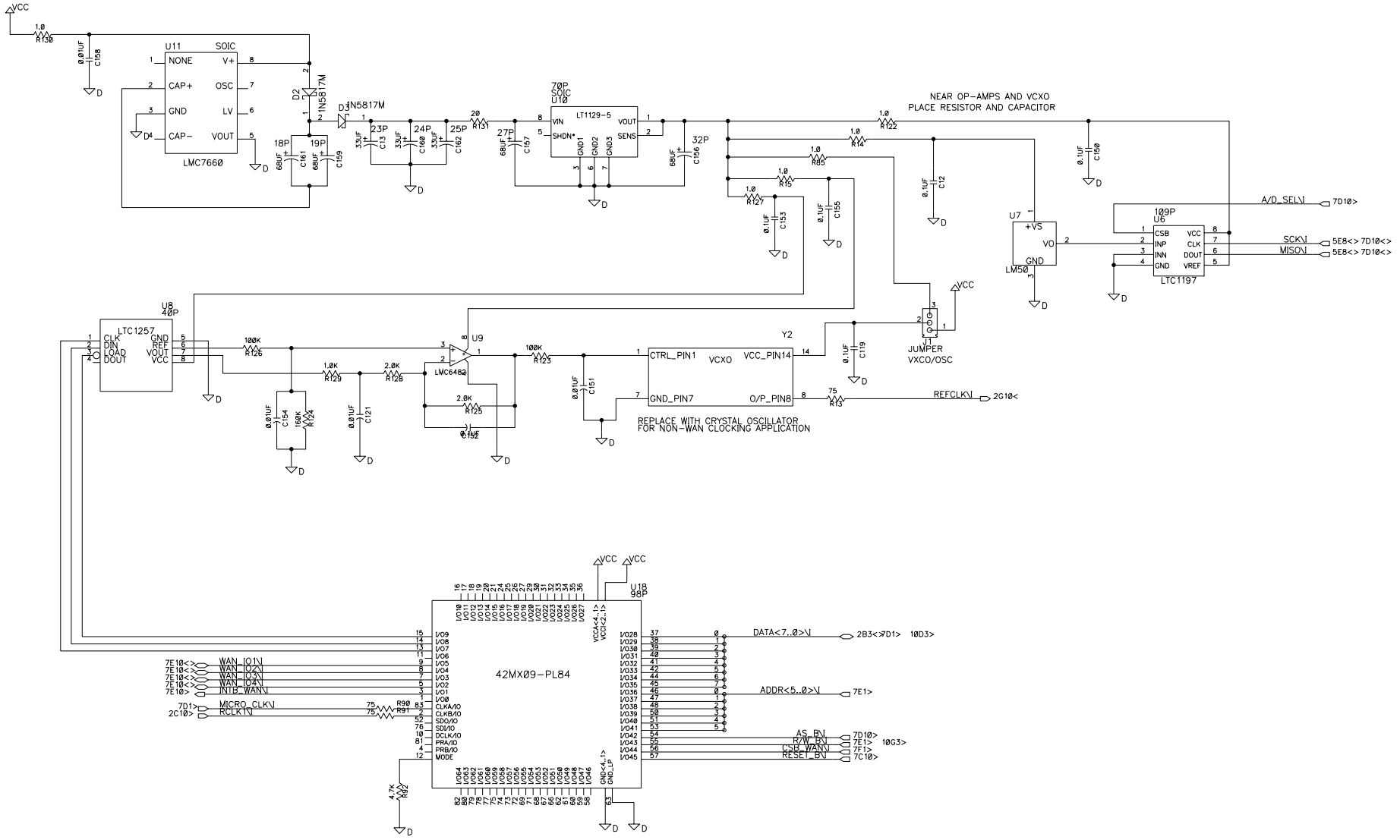

WAN CLOCKING CIRCUITRY FOR
S/UNI-TETRA REFERENCE DESIGN ONLY

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PMC-Sierra, Inc.

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TITLE: S/UNI-TETRA REFERENCE DESIGN WAN CLOCKING	REVISION NUMBER: 3.0
ENGINEER: PMC-SIERRA EC	PAGE: 9 OF 10

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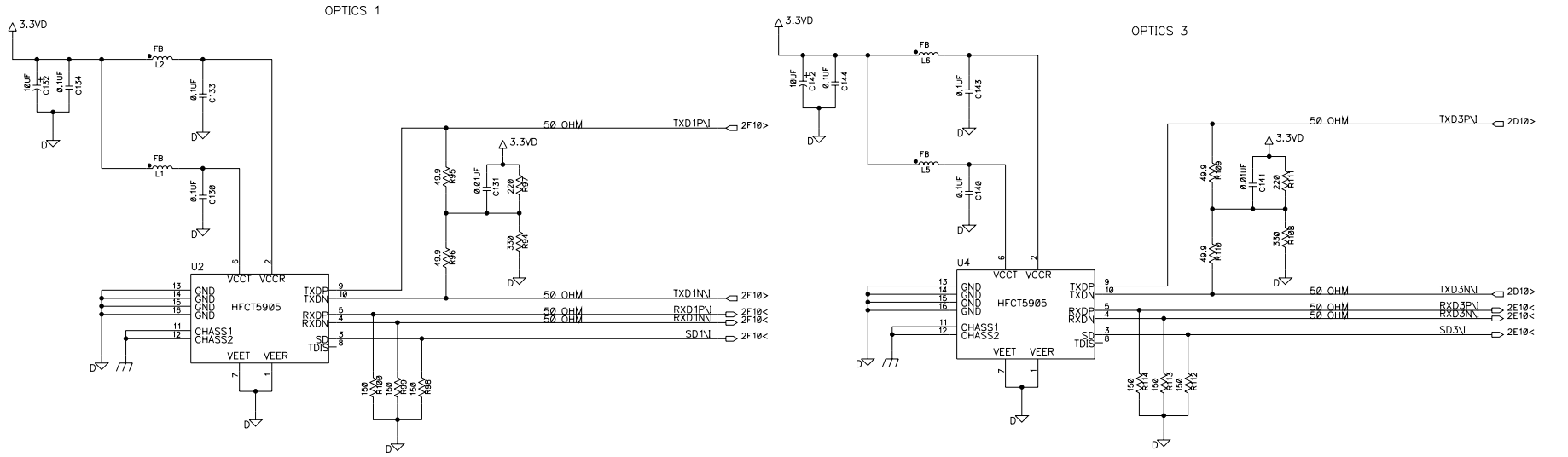

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TITLE: S/UNI-TETRA REFERENCE DESIGN OPTICS_BLOCK	REVISION NUMBER: 3.0
ENGINEER: PMC-SIERRA EC	PAGE: 10 OF 10

11 REFERENCES

- PMC-Sierra, Inc., PM5351 S/UNI-TETRA Data Sheet, Issue 2, March 1998
- Bell Communication Research – SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, December 1995

12 APPENDIX A

SWAN PLL Calculation

$n := 1, 2 .. 700$ **index for frequency**

$v_n := 10^{\frac{n - 301}{100}}$

$fs := 8 \cdot 10^3$ $TS := \frac{1}{fs}$ **Sampling interval**

$N := 512 \cdot 2$ **Averaging** $N = 1.024 \cdot 10^3$ **samples**

$T := N \cdot TS$ $T = 0.128$

$s_n := i \cdot 2 \cdot \pi \cdot 0.01 \cdot v_n$ **Complex frequency**

$z_n := \frac{1}{1 - s_n \cdot T}$ $s_n := \frac{1 - (z_n)^{-1}}{T}$

$Kpd := \frac{405}{2 \cdot \pi}$ **Phase Detector sensitivity in steps/rad**
51.84MHz/16=3.24MHz ;
3.24MHz/8KHz=405

$Kvco := \frac{2 \cdot \pi \cdot 8000}{3.2}$ **VCXO sensitivity in rad/volt**

$CO := 6480$ **Division factor in PLL** $\frac{51.84 \cdot 10^6}{8 \cdot 10^3} = 6.48 \cdot 10^3$

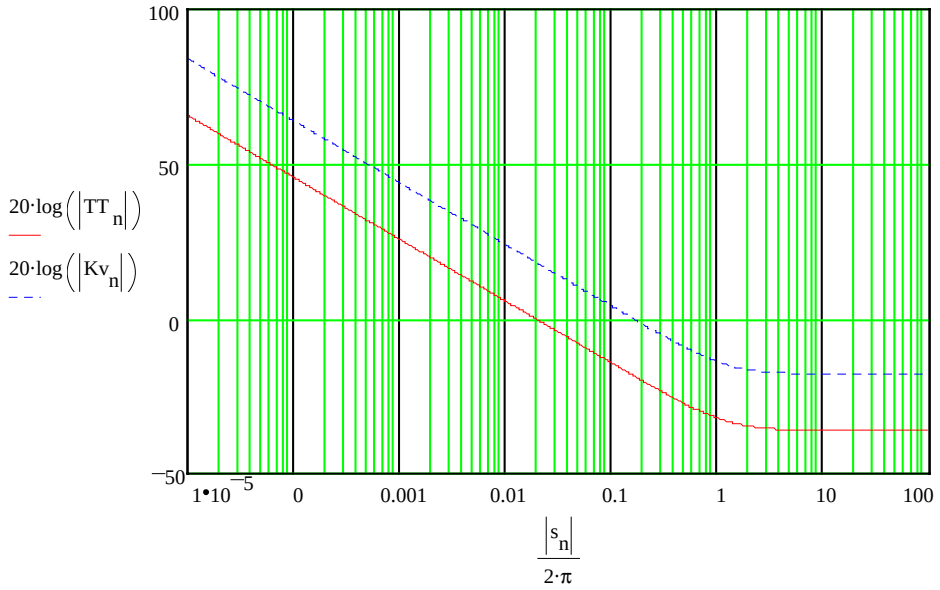
$Kdac := \frac{3.2}{2^{12}}$ **DAC sensitivity in volts/step**

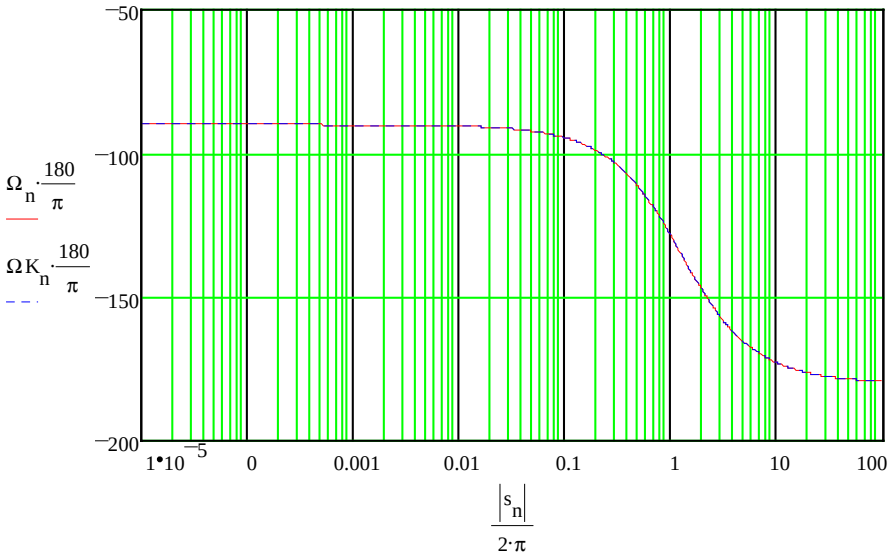
$K_n := Kpd \cdot Kvco \cdot Kdac \cdot \frac{1}{CO}$

$Kv_n := \frac{T}{z_n - 1}$

$\Omega K_n := Im(\ln(Kv_n))$

$$TT_n := Kv_n \cdot K_n \qquad \Omega_n := Im\left(\ln\left(TT_n\right)\right)$$

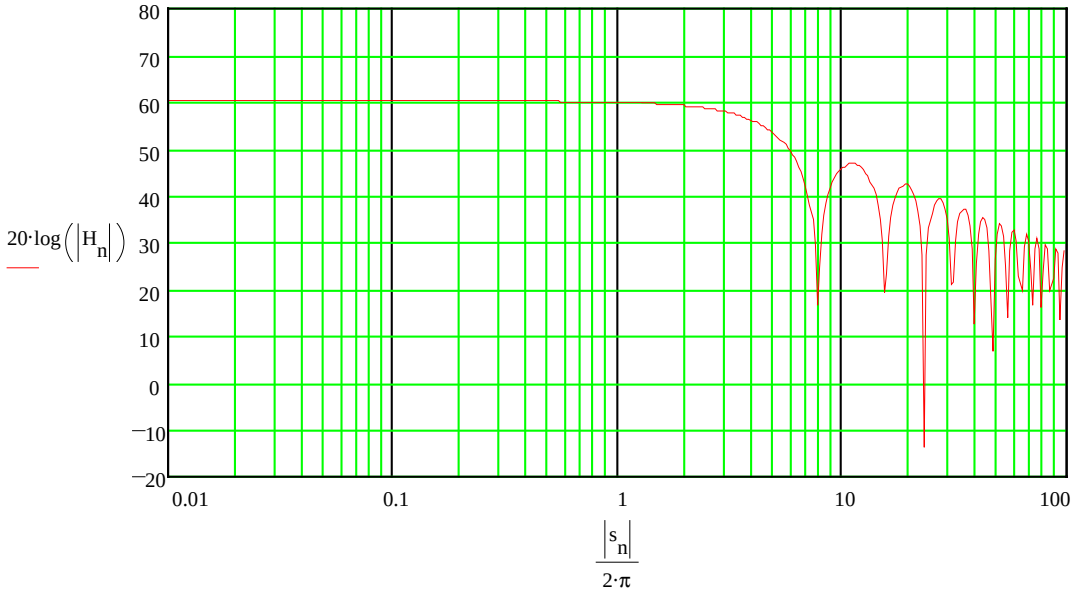




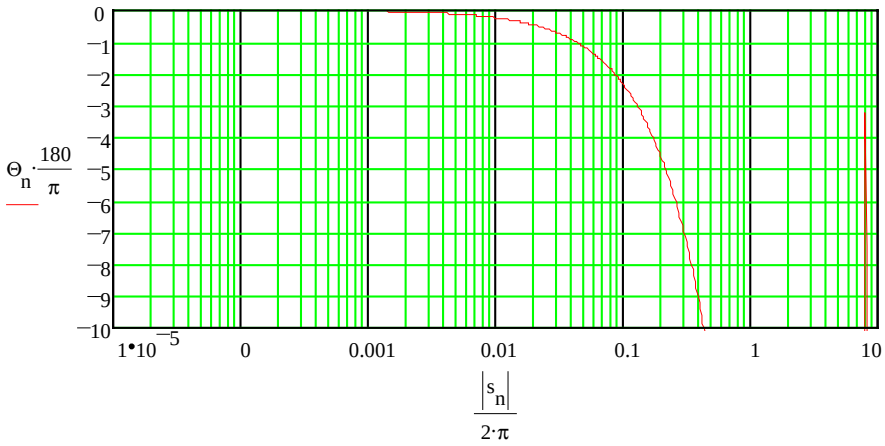
Averaging filter transfer function

$$z_n := e^{s_n \cdot TS}$$

$$H_n := 1 \cdot \left[\sum_{k=1}^{N} \left[(z_n)^{-k} \right] \right] \qquad \Theta_n := \mathrm{Im}\left(\ln\left(H_n\right)\right) \qquad HH_n := 1 \cdot \left[\sum_{k=1}^{8} \left[(z_n)^{-k} \right] \right]$$



MOVING AVERAGE FILTER



Lead-lag porton of the loop

$Fp := .002$ $\quad A := \frac{1}{2\cdot\pi\cdot Fp}$ $\quad A = 79.5774715459$

$Fz := .002$

$B := \frac{1}{2\cdot\pi\cdot Fz}$ $\quad Kp := \frac{2\cdot B - T}{2\cdot A}$ $\quad Ki := \frac{T}{A}$

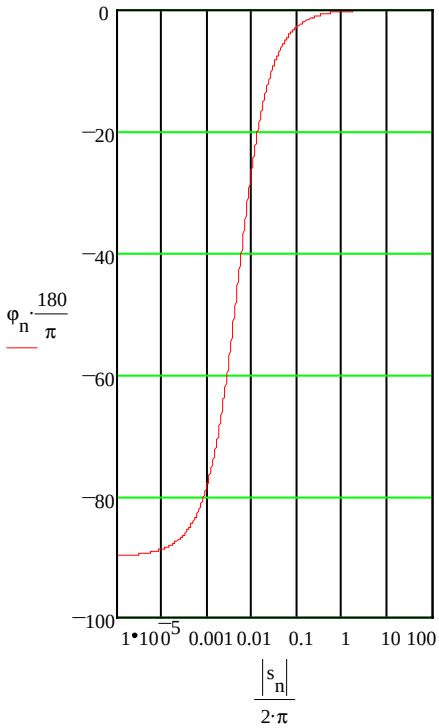
$GPZ_n := Kp + \frac{Ki\cdot z_n}{z_n - 1}$ $\quad Kp = 0.9991957523$ $\quad Ki = 0.0016084954$

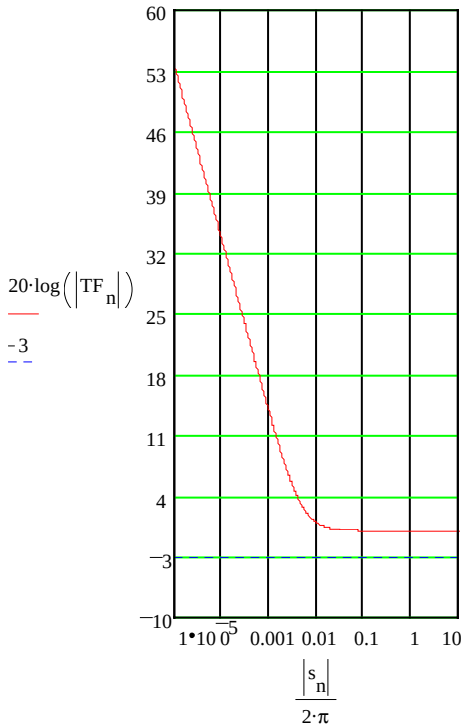
$\Omega_n := \frac{2}{T}\cdot\frac{z_n - 1}{z_n + 1}$

$Ki = 0.0016084954$ $\quad Kp := 1$ $\quad Ki := \frac{1}{2^8}$ $\quad Ki = 0.00390625$

$$TF_n := Kp + \frac{\frac{1}{1 - s_n\cdot T}\cdot Ki}{\frac{1}{1 - s_n\cdot T} - 1}$$

$\varphi_n := \mathrm{Im}\left(\ln\left(TF_n\right)\right)$





$G1 := 1$

NOTES

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