PM7364 & PM7366

PIN DIFFERENCES BETWEEN

FREEDM-32 AND FREEDM-8

PRELIMINARY INFORMATION

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CONTENTS

1 INTRODUCTION

This document highlights the different pin termination requirements between the FREEDM-32 and the FREEDM-8 devices. Although both devices have the same basic footprint, when a FREEDM-32 in used in place of a FREEDM-8 some unused pins must be correctly terminated in order for the device to function correctly.

1.1 References

[1] PMC-960113, PMC-Sierra, "Frame Relay Protocol Engine and Datalink Manager" Standard Product Datasheet, December, 1996, Issue 2
[2] PCI SIG, PCI Local Bus Specification, June 1, 1995, Version 2.1
[3] PCI Compact Specification, PCI Industrial Computers Manufacturers Group, 1995, Version 1.0
[4] PMC-970280, PMC-Sierra, "FREEDM Software Reference Design" Application Note, March, 1997, Issue 1
[5] PMC-961061, PMC-Sierra, "FREEDM PCI Bus Utilization and Latency Analysis" Application Note, February, 1997, Issue 1
[6] PMC-970281, PMC-Sierra, "FREEDM Programmer's Guide" Application Note, March, 1997, Issue 1

2 PIN DIFFERENCE TABLE

The table below shows the designations for each pin. The terminations for used FREEDM-8 pins have been highlighted. For detailed explanations of each pin please refer to the relevant pin descriptions. FREEDM-8 'X' pins can be tied high or low or left unconnected if desired.

PIN REF.	FREEDM-32 PINS	FREEDM-8 PINS	FREEDM-8 PIN TERMINATION
A20	VSS	VSS	
A19	VSS	VSS	
A18	VSS	VSS	
A17	RCLK[8]	X	HIGH/LOW/NC
A16	RCLK[10]	X	HIGH/LOW/NC
A15	RD[12]	TA[2]	LOW
A14	RD[14]	TA[4]	LOW
A13	VSS	VSS	
A12	RD[17]	TA[7]	LOW
A11	RD[19]	TA[9]	LOW
A10	VSS	VSS	
A9	VSS	VSS	
A8	RCLK[21]	X	HIGH/LOW/NC
A7	RCLK[23]	X	HIGH/LOW/NC
A6	RCLK[25]	X	HIGH/LOW/NC
A5	RD[27]	X	HIGH/LOW/NC
A4	RD[29]	X	HIGH/LOW/NC
A3	VSS	VSS	
A2	VSS	VSS	
A1	VSS	VSS	
B20	VSS	VSS	
B19	VDD	VDD	
B18	VDD	VDD	
B17	RD[8]	X	HIGH/LOW/NC
B16	RD[10]	TA[0]	LOW
B15	RCLK[11]	X	HIGH/LOW/NC
B14	RCLK[13]	X	HIGH/LOW/NC
B13	RCLK[15]	X	HIGH/LOW/NC
B12	RCLK[16]	X	HIGH/LOW/NC
B11	RCLK[18]	X	HIGH/LOW/NC

PIN REF.	FREEDM-32 PINS	FREEDM-8 PINS	FREEDM-8 PIN TERMINATION
B10	RD[20]	TA[10]	LOW
B9	RCLK[20]	X	HIGH/LOW/NC
B8	RCLK[22]	X	HIGH/LOW/NC
B7	RD[24]	X	HIGH/LOW/NC
B6	RD[26]	X	HIGH/LOW/NC
B5	RCLK[27]	X	HIGH/LOW/NC
B4	RCLK[29]	X	HIGH/LOW/NC
B3	VDD	VDD	
B2	VDD	VDD	
B1	VSS	VSS	
C20	VSS	VSS	
C19	VDD	VDD	
C18	VDD	VDD	
C17	RD[7]	RD[7]	
C16	RD[9]	X	HIGH/LOW/NC
C15	RD[11]	TA[1]	LOW
C14	RCLK[12]	X	HIGH/LOW/NC
C13	RCLK[14]	X	HIGH/LOW/NC
C12	RD[16]	TA[6]	LOW
C11	RD[18]	TA[8]	LOW
C10	RCLK[19]	X	HIGH/LOW/NC
C9	RD[21]	TA[11]	LOW
C8	RD[23]	TWRB	HIGH
C7	RD[25]	X	HIGH/LOW/NC
C6	RCLK[26]	X	HIGH/LOW/NC
C5	RCLK[28]	X	HIGH/LOW/NC
C4	PCICLK	PCICLK	
C3	VDD	VDD	
C2	VDD	VDD	
C1	VSS	VSS	
D20	RD[5]	RD[5]	
D19	RCLK[5]	RCLK[5]	
D18	RCLK[6]	RCLK[6]	
D17	NC	NC	N/C
D16	RCLK[7]	RCLK[7]	
D15	RCLK[9]	X	HIGH/LOW/NC
D14	VDD	VDD	
D13	RD[13]	TA[3]	LOW
D12	RD[15]	TA[5]	LOW
D11	RCLK[17]	X	HIGH/LOW/NC

PIN REF.	FREEDM-32 PINS	FREEDM-8 PINS	FREEDM-8 PIN TERMINATION
D10	VDD	VDD	
D9	RD[22]	TRDB	HIGH
D8	RCLK[24]	X	HIGH/LOW/NC
D7	VDD	VDD	
D6	RD[28]	X	HIGH/LOW/NC
D5	PCICLKO	PCICLKO	
D4	VBIAS	VBIAS	
D3	GNTB	GNTB	
D2	AD[31]	AD[31]	
D1	AD[30]	AD[30]	
E20	RD[3]	RD[3]	
E19	RCLK[3]	RCLK[3]	
E18	RCLK[4]	RCLK[4]	
E17	RD[6]	RD[6]	
E4	REQB	REQB	
E3	AD[29]	AD[29]	
E2	AD[27]	AD[27]	
E1	AD[26]	AD[26]	
F20	RCLK[1]	RCLK[1]	
F19	RD[2]	RD[2]	
F18	RCLK[2]	RCLK[2]	
F17	RD[4]	RD[4]	
F4	AD[28]	AD[28]	
F3	AD[25]	AD[25]	
F2	AD[24]	AD[24]	
F1	CBEB[3]	CBEB[3]	
G20	RBLK	RBLK	
G19	RD[0]	RD[0]	
G18	RD[1]	RD[1]	
G17	VDD	VDD	
G4	VDD	VDD	
G3	IDSEL	IDSEL	
G2	AD[22]	AD[22]	
G1	AD[21]	AD[21]	
H20	VBIAS	VBIAS	
H19	SYSCLK	SYSCLK	
H18	RBD	RBD	
H17	RCLK[0]	RCLK[0]	
H4	AD[23]	AD[23]	
H3	AD[20]	AD[20]	

PIN REF.	FREEDM-32 PINS	FREEDM-8 PINS	FREEDM-8 PIN TERMINATION
H2	AD[18]	AD[18]	
H1	VSS	VSS	
J20	VSS	VSS	
J19	TCK	TCK	
J18	TMS	TMS	
J17	TRSTB	TRSTB	
J4	AD[19]	AD[19]	
J3	AD[17]	AD[17]	
J2	AD[16]	AD[16]	
J1	CBEB[2]	CBEB[2]	
K20	VSS	VSS	
K19	TDI	TDI	
K18	TDO	TDO	
K17	VDD	VDD	
K4	FRAMEB	FRAMEB	
K3	IRDYB	IRDYB	
K2	TRDYB	TRDYB	
K1	DEVSELB	DEVSELB	
L20	TD[0]	TD[0]	
L19	TCLK[0]	TCLK[0]	
L18	TD[1]	TD[1]	
L17	TCLK[1]	TCLK[1]	
L4	VDD	VDD	
L3	STOPB	STOPB	
L2	LOCKB	LOCKB	
L1	VSS	VSS	
M20	TD[2]	TD[2]	
M19	TCLK[2]	TCLK[2]	
M18	TD[3]	TD[3]	
M17	TD[4]	TD[4]	
M4	CBEB[1]	CBEB[1]	
M3	SERRB	SERRB	
M2	PERRB	PERRB	
M1	VSS	VSS	
N20	VSS	VSS	
N19	TCLK[3]	TCLK[3]	
N18	TCLK[4]	TCLK[4]	
N17	TD[6]	TD[6]	
N4	AD[11]	AD[11]	
N3	AD[14]	AD[14]	

PIN REF.	FREEDM-32 PINS	FREEDM-8 PINS	FREEDM-8 PIN TERMINATION
N2	AD[15]	AD[15]	
N1	PAR	PAR	
P20	TD[5]	TD[5]	
P19	TCLK[5]	TCLK[5]	
P18	TCLK[6]	TCLK[6]	
P17	VDD	VDD	
P4	VDD	VDD	
P3	AD[10]	AD[10]	
P2	AD[12]	AD[12]	
P1	AD[13]	AD[13]	
R20	TD[7]	TD[7]	
R19	TCLK[7]	TCLK[7]	
R18	TD[8]	NC	N/C
R17	TCLK[9]	X	HIGH/LOW/NC
R4	AD[5]	AD[5]	
R3	CBEB[0]	CBEB[0]	
R2	AD[8]	AD[8]	
R1	AD[9]	AD[9]	
T20	TCLK[8]	X	HIGH/LOW/NC
T19	TD[9]	NC	N/C
T18	TD[10]	NC	N/C
T17	TCLK[11]	X	HIGH/LOW/NC
T4	AD[1]	AD[1]	
T3	AD[4]	AD[4]	
T2	AD[6]	AD[6]	
T1	AD[7]	AD[7]	
U20	TCLK[10]	X	HIGH/LOW/NC
U19	TD[11]	NC	N/C
U18	TD[12]	NC	N/C
U17	NC	NC	N/C
U16	TD[13]	NC	N/C
U15	TD[15]	NC	N/C
U14	VDD	VDD	
U13	TCLK[18]	X	HIGH/LOW/NC
U12	TD[21]	TDAT[5]	N/C
U11	VDD	VDD	
U10	TCLK[25]	X	HIGH/LOW/NC
U9	TD[28]	TDAT[12]	N/C
U8	TD[30]	TDAT[14]	N/C
U7	VDD	VDD	

PIN REF.	FREEDM-32 PINS	FREEDM-8 PINS	FREEDM-8 PIN TERMINATION
U6	PMCTEST	PMCTEST	
U5	RCLK[30]	X	HIGH/LOW/NC
U4	VBIAS	VBIAS	
U3	AD[0]	AD[0]	
U2	AD[2]	AD[2]	
U1	AD[3]	AD[3]	
V20	VSS	VSS	
V19	VDD	VDD	
V18	VDD	VDD	
V17	TCLK[12]	X	HIGH/LOW/NC
V16	TCLK[14]	X	HIGH/LOW/NC
V15	TCLK[16]	X	HIGH/LOW/NC
V14	TD[18]	TDAT[2]	N/C
V13	TD[20]	TDAT[4]	N/C
V12	TD[22]	TDAT[6]	N/C
V11	TCLK[23]	X	HIGH/LOW/NC
V10	TD[25]	TDAT[9]	N/C
V9	TD[27]	TDAT[11]	N/C
V8	TCLK[28]	X	HIGH/LOW/NC
V7	TCLK[30]	X	HIGH/LOW/NC
V6	TBD	TBD	
V5	PCIINTB	PCIINTB	
V4	RD[30]	X	HIGH/LOW/NC
V3	VDD	VDD	
V2	VDD	VDD	
V1	VSS	VSS	
W20	VSS	VSS	
W19	VDD	VDD	
W18	VDD	VDD	
W17	TCLK[13]	X	HIGH/LOW/NC
W16	TCLK[15]	X	HIGH/LOW/NC
W15	TD[17]	TDAT[1]	N/C
W14	TD[19]	TDAT[3]	N/C
W13	TCLK[20]	X	HIGH/LOW/NC
W12	TCLK[22]	X	HIGH/LOW/NC
W11	TD[23]	TDAT[7]	N/C
W10	TCLK[24]	X	HIGH/LOW/NC
W9	TCLK[26]	X	HIGH/LOW/NC
W8	TCLK[27]	X	HIGH/LOW/NC
W7	TCLK[29]	X	HIGH/LOW/NC

PIN REF.	FREEDM-32 PINS	FREEDM-8 PINS	FREEDM-8 PIN TERMINATION
W6	TCLK[31]	X	HIGH/LOW/NC
W5	RSTB	RSTB	
W4	RD[31]	X	HIGH/LOW/NC
W3	VDD	VDD	
W2	VDD	VDD	
W1	VSS	VSS	
Y20	VSS	VSS	
Y19	VSS	VSS	
Y18	VSS	VSS	
Y17	TD[14]	NC	N/C
Y16	TD[16]	TDAT[0]	N/C
Y15	TCLK[17]	X	HIGH/LOW/NC
Y14	TCLK[19]	X	HIGH/LOW/NC
Y13	TCLK[21]	X	HIGH/LOW/NC
Y12	VSS	VSS	
Y11	VSS	VSS	
Y10	TD[24]	TDAT[8]	N/C
Y9	TD[26]	TDAT[10]	N/C
Y8	VSS	VSS	
Y7	TD[29]	TDAT[13]	N/C
Y6	TD[31]	TDAT[15]	N/C
Y5	TBCLK	TBCLK	
Y4	RCLK[31]	X	HIGH/LOW/NC
Y3	VSS	VSS	
Y2	VSS	VSS	
Y1	VSS	VSS	

4 FREEDM-8 PIN DESCRIPTION

4.1 Line Side Interface Signals (36)

Pin Name	Type	Pin No.	Function
RCLK[0] RCLK[1] RCLK[2] RCLK[3] RCLK[4] RCLK[5] RCLK[6] RCLK[7]	Input	H17 F20 F18 E19 E18 D19 D18 D16	The receive line clock signals (RCLK[7:0]) contain the recovered line clock for the 8 independently timed links. Processing of the receive links are on a priority basis, in descending order from RCLK[0] to RCLK[7]. Therefore, the highest rate link should be connected to RCLK[0] and the lowest to RCLK[7]. RD[7:0] is sampled on the rising edge of the corresponding RCLK[7:0] clock. For channelised T1 or E1 links, RCLK[n] must be gapped during the framing bit (for T1 interfaces) or during time-slot 0 (for E1 interfaces) of the RD[n] stream. The FREEDM-8 uses the gapping information to determine the time-slot alignment in the receive stream. RCLK[7:0] is nominally a 50% duty cycle clock of 1.544 MHz for T1 links and 2.048 MHz for E1 links. For unchannelised links, RCLK[n] must be externally gapped during the bits or time-slots that are not part of the transmission format payload (i.e. not part of the HDLC packet). RCLK[2:0] is nominally a 50% duty cycle clock between 0 and 52 MHz. RCLK[7:3] is nominally a 50% duty cycle clock between 0 and 10 MHz.

RD[0] RD[1] RD[2] RD[3] RD[4] RD[5] RD[6] RD[7]	Input	G19 G18 F19 E20 F17 D20 E17 C17	The receive data signals (RD[7:0]) contain the recovered line data for the 8 independently timed links. Processing of the receive links are on a priority basis, in descending order form RD[0] to RD[7]. Therefore, the highest rate link should be connected to RD[0] and the lowest to RD[7]. For channelised links, RD[n] contains the 24 (T1) or 31 (E1) time-slots that comprise the channelised link. RCLK[n] must be gapped during the T1 framing bit position or the E1 frame alignment signal (time-slot 0). The FREEDM-8 uses the location of the gap to determine the channel alignment on RD[n]. For unchannelised links, RD[n] contains the HDLC packet data. For certain transmission formats, RD[n] may contain place holder bits or time-slots. RCLK[n] must be externally gapped during the place holder positions in the RD[n] stream. The FREEDM-8 supports a maximum data rate of 10 Mbit/s on an individual RD[7:3] link and a maximum data rate of 52 Mbit/s on RD[2:0]. RD[7:0] is sampled on the rising edge of the corresponding RCLK[7:0] clock.
RBD	Tri-state Output	H18	The receive BERT data signal (RBD) contains the receive bit error rate test data. RBD reports the data on the selected one of the receive data signals (RD[7:0]) and is updated on the falling edge of RBCLK. RBD may be tri-stated by setting the RBEN bit in the FREEDM-8 Master BERT Control register low.
RBCLK	Tri-state Output	G20	The receive BERT clock signal (RBCLK) contains the receive bit error rate test clock. RBCLK is a buffered version of the selected one of the receive clock signals (RCLK[7:0]). RBCLK may be tri-stated by setting the RBEN bit in the FREEDM-8 Master BERT Control register low.

TCLK[0] TCLK[1] TCLK[2] TCLK[3] TCLK[4] TCLK[5] TCLK[6] TCLK[7]	Input	L19 L17 M19 N19 N18 P19 P18 R19	The transmit line clock signals (TCLK[7:0]) contain the transmit clocks for the 8 independently timed links. Processing of the transmit links is on a priority basis, in descending order from TCLK[0] to TCLK[7]. Therefore, the highest rate link should be connected to TCLK[0] and the lowest to TCLK[7]. TD[7:0] is updated on the falling edge of the corresponding TCLK[7:0] clock. For channelised T1 or E1 links, TCLK[n] must be gapped during the framing bit (for T1 interfaces) or during time-slot 0 (for E1 interfaces) of the TD[n] stream. The FREEDM-8 uses the gapping information to determine the time-slot alignment in the transmit stream. For unchannelised links, TCLK[n] must be externally gapped during the bits or time-slots that are not part of the transmission format payload (i.e. not part of the HDLC packet). TCLK[7:3] is nominally a 50% duty cycle clock between 0 and 10 MHz. TCLK[2:0] is nominally a 50% duty cycle clock between 0 and 52 MHz. Typical values for TCLK[7:0] include 1.544 MHz (for T1 links) and 2.048 MHz (for E1 links).

TD[0] TD[1] TD[2] TD[3] TD[4] TD[5] TD[6] TD[7]	Output	L20 L18 M20 M18 M17 P20 N17 R20	The transmit data signals (TD[7:0]) contains the transmit data for the 8 independently timed links in normal mode (PMCTEST set low). Processing of the transmit links are on a priority basis, in descending order from TD[0] to TD[7]. Therefore, the highest rate link should be connected to TD[0] and the lowest to TD[7]. For channelised links, TD[n] contains the 24 (T1) or 31 (E1) time-slots that comprise the channelised link. TCLK[n] must be gapped during the T1 framing bit position or the E1 frame alignment signal (time-slot 0). The FREEDM-8 uses the location of the gap to determine the channel alignment on TD[n]. For unchannelised links, TD[n] contains the HDLC packet data. For certain transmission formats, TD[n] may contain place holder bits or time-slots. TCLK[n] must be externally gapped during the place holder positions in the TD[n] stream. The FREEDM-8 supports a maximum data rate of 10 Mbit/s on an individual TD[7:3] link and a maximum data rate of 52 Mbit/s on TD[2:0]. TD[7:0] is updated on the falling edge of the corresponding TCLK[7:0] clock.
TBD	Input	V6	The transmit BERT data signal (TBD) contains the transmit bit error rate test data. When the TBEN bit in the FREEDM-8 Master BERT Control register is set high, the data on TDB is transmitted on the selected one of the transmit data signals (TD[7:0]). TBD is sampled on the rising edge of TBCLK.
TBCLK	Tri-state Output	Y5	The transmit BERT clock signal (TBCLK) contains the transmit bit error rate test clock. TBCLK is a buffered version of the selected one of the transmit clock signals (TCLK[7:0]). TBCLK may be tri-stated by setting the TBEN bit in the FREEDM-8 Master BERT Control register low.

4.2 PCI Host Interface Signals (51)

Pin Name	Type	Pin No.	Feature
PCICLK	Input	C4	The PCI clock signal (PCICLK) provides timing for PCI bus accesses. PCICLK is a nominally 50% duty cycle, 0 to 33 MHz clock.
PCICLKO	Output	D5	The PCI clock output signal (PCICLKO) is a buffered version of the PCICLK. PCICLKO may be used to drive the SYSCLK input.

AD[0] AD[1] AD[2] AD[3] AD[4] AD[5] AD[6] AD[7] AD[8] AD[9] AD[10] AD[11] AD[12] AD[13] AD[14] AD[15] AD[16] AD[17] AD[18] AD[19] AD[20] AD[21] AD[22] AD[23] AD[24] AD[25] AD[26] AD[27] AD[28] AD[29] AD[30] AD[31]	I/O	U3 T4 U2 U1 T3 R4 T2 T1 R2 R1 P3 N4 P2 P1 N3 N2 J2 J3 H2 J4 H3 G1 G2 H4 F2 F3 E1 E2 F4 E3 D1 D2	The PCI address and data bus (AD[31:0]) carries the PCI bus multiplexed address and data. During the first clock cycle of a transaction, AD[31:0] contains a physical byte address. During subsequent clock cycles of a transaction, AD[31:0] contains data. A transaction is defined as an address phase followed by one or more data phases. When Little-Endian byte formatting is selected, AD[31:24] contain the most significant byte of a DWORD while AD[7:0] contain the least significant byte. When Big-Endian byte formatting is selected. AD[7:0] contain the most significant byte of a DWORD while AD[31:24] contain the least significant byte. When the FREEDM-8 is the initiator, AD[31:0] is an output bus during the first (address) phase of a transaction. For write transactions, AD[31:0] remains an output bus for the data phases of the transaction. For read transactions, AD[31:0] is an input bus during the data phases. When the FREEDM-8 is the target, AD[31:0] is an input bus during the first (address) phase of a transaction. For write transactions, AD[31:0] remains an input bus during the data phases of the transaction. For read transactions, AD[31:0] is an output bus during the data phases. When the FREEDM-8 is not involved in the current transaction, AD[31:0] is tri-stated. As an output bus, AD[31:0] is updated on the rising edge of PCICLK. As an input bus, AD[31:0] is sampled on the rising edge of PCICLK.

C/BEB[0] C/BEB[1] C/BEB[2] C/BEB[3]	I/O	R3 M4 J1 F1	The PCI bus command and byte enable bus (C/BEB[3:0]) contains the bus command or the byte valid indications. During the first clock cycle of a transaction, C/BEB[3:0] contains the bus command code. For subsequent clock cycles, C/BEB[3:0] identifies which bytes on the AD[31:0] bus carry valid data. C/BEB[3] is associated with byte 3 (AD[31:24]) while C/BEB[0] is associated with byte 0 (AD[7:0]). When C/BEB[n] is set high, the associated byte is invalid. When C/BEB[n] is set low, the associated byte is valid. When the FREEDM-8 is the initiator, C/BEB[3:0] is an output bus. When the FREEDM-8 is the target, C/BEB[3:0] is an input bus. When the FREEDM-8 is not involved in the current transaction, C/BEB[3:0] is tri-stated. As an output bus, C/BEB[3:0] is updated on the rising edge of PCICLK. As an input bus, C/BEB[3:0] is sampled on the rising edge of PCICLK.
PAR	I/O	N1	The parity signal (PAR) indicates the parity of the AD[31:0] and C/BEB[3:0] buses. Even parity is calculated over all 36 signals in the buses regardless of whether any or all the bytes on the AD[31:0] are valid. PAR always reports the parity of the previous PCICLK cycle. Parity errors detected by the FREEDM-8 are indicated on output PERRB and in the FREEDM-8 Master Interrupt Status register. When the FREEDM-8 is the initiator, PAR is an output for writes and an input for reads. When the FREEDM-8 is the target, PAR is an input for writes and an output for reads. When the FREEDM-8 is not involved in the current transaction, PAR is tri-stated. As an output signal, PAR is updated on the rising edge of PCICLK. As an input signal, PAR is sampled on the rising edge of PCICLK.

FRAMEB	I/O	K4	The active low cycle frame signal (FRAMEB) identifies a transaction cycle. When FRAMEB transitions low, the start of a bus transaction is indicated. FRAMEB remains low to define the duration of the cycle. When FRAMEB transitions high, the last data phase of the current transaction is indicated. When the FREEDM-8 is the initiator, FRAMEB is an output. When the FREEDM-8 is the target, FRAMEB is an input. When the FREEDM-8 is not involved in the current transaction, FRAMEB is tri-stated. As an output signal, FRAMEB is updated on the rising edge of PCICLK. As an input signal, FRAMEB is sampled on the rising edge of PCICLK.
TRDYB	I/O	K2	The active low target ready signal (TRDYB) indicates when the target is ready to start or continue with a transaction. TRDYB works in conjunction with IRDYB to complete transaction data phases. During a transaction in progress, TRDYB is set high to indicate that the target cannot complete the current data phase and to force a wait state. TRDYB is set low to indicate that the target can complete the current data phase. The data phase is completed when TRDYB is set low and the initiator ready signal (IRDYB) is also set low. When the FREEDM-8 is the initiator, TRDYB is an input. When the FREEDM-8 is the target, TRDYB is an output. During accesses to FREEDM-8 registers, TRDYB is set high to extend data phases over multiple PCICLK cycles. When the FREEDM-8 is not involved in the current transaction, TRDYB is tri-stated. As an output signal, TRDYB is updated on the rising edge of PCICLK. As an input signal, TRDYB is sampled on the rising edge of PCICLK.

IRDYB	I/O	K3	The active low initiator ready (IRDYB) signal is used to indicate whether the initiator is ready to start or continue with a transaction. IRDYB works in conjunction with TRDYB to complete transaction data phases. When IRDYB is set high and a transaction is in progress, the initiator is indicating it cannot complete the current data phase and is forcing a wait state. When IRDYB is set low and a transaction is in progress, the initiator is indicating it has completed the current data phase. The data phase is completed when IRDYB is set low and the target ready signal (IRDYB) is also set low. When the FREEDM-8 is the initiator, IRDYB is an output. When the FREEDM-8 is the target, IRDYB is an input. When the FREEDM-8 is not involved in the current transaction, IRDYB is tri-stated. IRDYB is updated on the rising edge of PCICLK or sampled on the rising edge of PCICLK depending on whether it is an output or an input.
STOPB	I/O	L3	The active low stop signal (STOPB) requests the initiator to stop the current bus transaction. When STOPB is set high by a target, the initiator continues with the transaction. When STOPB is set low, the initiator will stop the current transaction. When the FREEDM-8 is the initiator, STOPB is an input. When STOPB is sampled low, the FREEDM-8 will terminate the current transaction in the next PCICLK cycle. When the FREEDM-8 is the target, STOPB is an output. The FREEDM-8 only issues transaction stop requests when its internal bus latency buffers are in a near overflow state. When the FREEDM-8 is not involved in the current transaction, STOPB is tri-stated. STOPB is updated on the rising edge of PCICLK or sampled on the rising edge of PCICLK depending on whether it is an output or an input.

IDSEL	Input	G3	The initialization device select signal (IDSEL) enables read and write access to the PCI configuration registers. When IDSEL is set high during the address phase of a transaction and the C/BEB[3:0] code indicates a register read or write, the FREEDM-8 performs a PCI configuration register transaction and asserts the DEVSELB signal in the next PCICLK period. IDSEL is sampled on the rising edge of PCICLK.
DEVSELB	I/O	K1	The active low device select signal (DEVSELB) indicates that a target claims the current bus transaction. During the address phase of a transaction, all targets decode the address on the AD[31:0] bus. When a target, recognizes the address as its own, it sets DEVSELB low to indicate to the initiator that the address is valid. If no target claims the address in six bus clock cycles, the initiator assumes that the target does not exist or cannot respond and aborts the transaction. When the FREEDM-8 is the initiator, DEVSELB is an input. If no target responds to an address in six PCICLK cycles, the FREEDM-8 will abort the current transaction and alerts the PCI Host via an interrupt. When the FREEDM-8 is the target, DEVSELB is an output. DELSELB is set low when the address on AD[31:0] is recognised. When the FREEDM-8 is not involved in the current transaction, DEVSELB is tri-stated. FREEDM-8 is updated on the rising edge of PCICLK or sampled on the rising edge of PCICLK depending on whether it is an output or an input.

LOCKB	Input	L2	The active low bus lock signal (LOCKB) locks a target device. When LOCKB and FRAME are set low, and the FREEDM-8 is the target, an initiator is locking the FREEDM-8 as an "owned" target. Under these circumstances, the FREEDM-8 will reject all transaction with other initiators. The FREEDM-8 will continue to reject other initiators until its owner releases the lock by forcing both FRAMEB and LOCKB high. As a initiator, the FREEDM-8 will never lock a target. LOCKB is sampled using the rising edge of PCICLK.
REQB	Output	E4	The active low PCI bus request signal (REQB) requests an external arbiter for control of the PCI bus. REQB is set low when the FREEDM-8 desires access to the host memory. REQB is set high when access is not desired. REQB is updated on the rising edge of PCICLK.
GNTB	Input	D3	The active low PCI bus grant signal (GNTB) indicates the granting of control over the PCI in response to a bus request via the REQB output. When GNTB is set high, the FREEDM-8 does not have control over the PCI bus. When GNTB is set low, the external arbiter has granted the FREEDM-8 control over the PCI bus. However, the FREEDM-8 will not proceed until the FRAMEB signal is sampled high, indicating no current transactions are in progress. GNTB is sampled on the rising edge of PCICLK.
PCIINTB	OD Output	V5	The active low PCI interrupt signal (PCIINTB) is set low when a FREEDM-8 interrupt source is active, and that source is unmasked. The FREEDM-8 may be enabled to report many alarms or events via interrupts. PCIINTB returns high when the interrupt is acknowledged via an appropriate register access. PCIINTB is an open drain output and is updated on the rising edge of PCICLK.

PERRB	I/O	M2	The active low parity error signal (PERRB) indicates a parity error over the AD[31:0] and C/BEB[3:0] buses. Parity error is detect when even parity calculations do not match the PAR signal. PERRB is set low at the cycle immediately following an offending PAR cycle. PERRB is set high when no parity error is detected. PERRB is enabled by setting the PERREN bit in the Control/Status register in the PCI Configuration registers space. Regardless of the setting of PERREN, parity errors are always reported by the PERR bit in the Control/Status register in the PCI Configuration registers space. PERRB is updated on the rising edge of PCICLK.
SERRB	OD Output	M3	The active low system error signal (SERRB) indicates an address parity error. Address parity errors are detected when the even parity calculations during the address phase do not match the PAR signal. When the FREEDM-8 detects a system error, SERRB is set low for one PCICLK period. SERRB is enabled by setting the SERREN bit in the Control/Status register in the PCI Configuration registers space. Regardless of the setting of SERREN, parity errors are always reported by the SERR bit in the Control/Status register in the PCI Configuration registers space. SERRB is an open drain output and is updated on the rising edge of PCICLK.

4.3 Miscellaneous Interface Signals (11)

Pin Name	Type	Pin No.	Feature
SYSCLK	Input	H19	The system clock (SYSCLK) provides timing for the core logic. SYSCLK is nominally a 50% duty cycle 25 MHz to 33 MHz clock.
RSTB	Input	W5	The active low reset signal (RSTB) signal provides an asynchronous FREEDM-8 reset. RSTB is an asynchronous input. When RSTB is set low, all FREEDM-8 registers are forced to their default states. In addition, TD[7:0] are forced high and all PCI output pins are forced tri-state and will remain high or tri-stated, respectively, until RSTB is set high.
PMCTEST	Input	U6	The PMC production test enable signal (PMCTEST) places the FREEDM-8 is test mode. When PMCTEST is set high, production test vectors can be executed to verify manufacturing via the test mode interface signals TA[10:0], TA[11]/TRS, TRDB, TWRB and TDAT[15:0]. PMCTEST is set low in normal operation. PMCTEST is an asynchronous input and has an integral pull-down resistor.
TCK	Input	J19	The test clock signal (TCK) provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. TMS and TDI are sampled on the rising edge of TCK. TDO is updated on the falling edge of TCK.
TMS	Input	J18	The test mode select signal (TMS) controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	K19	The test data input signal (TDI) carries test data into the FREEDM-8 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.

TDO	Tri-state	K18	The test data output signal (TDO) carries test data out of the FREEDM-8 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	J17	The active low test reset signal (TRSTB) provides an asynchronous FREEDM-8 test access port reset via the IEEE P1149.1 test access port. TRSTB is an asynchronous input with an integral pull up resistor. Note that when TRSTB is not being used, it must be connected to the RSTB input.
VBIAS[3:1]	Input	U4 D4 H20	The bias signals (VBIAS[3:1]) provide 5 Volt bias to input and I/O pads to allow the FREEDM-8 to tolerate connections to 5 Volt devices.

4.4 Production Test Interface Signals (30)

Pin Name	Type	Pin No.	Feature
TA[0] TA[1] TA[2] TA[3] TA[4] TA[5] TA[6] TA[7] TA[8] TA[9] TA[10]	Input	B16 C15 A15 D13 A14 D12 C12 A12 C11 A11 B10	The test mode address bus (TA[10:0]) selects specific registers during production test (PMCTEST set high) read and write accesses.
TA[11]/TRS		C9	The test register select signal (TA[11]/TRS) selects between normal and test mode register accesses during production test (PMCTEST set high). TRS is set high to select test registers and is set low to select normal registers. In normal operation (PMCTEST set low), TA[11:0] should be tied low.
TRDB	Input	D9	The test mode read enable signal (TRDB) is set low during FREEDM-8 register read accesses during production test (PMCTEST set high). The FREEDM-8 drives the test data bus (TDAT[15:0]) with the contents of the addressed register while TRDB is low. In normal operation (PMCTEST set low), TRDB should be tied high.
TWRB	Input	C8	The test mode write enable signal (TWRB) is set low during FREEDM-8 register write accesses during production test (PMCTEST set high). The contents of the test data bus (TDAT[15:0]) are clocked into the addressed register on the rising edge of TWRB. In normal operation (PMCTEST set low), TWRB should be tied high.

TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	I/O	Y16 W15 V14 W14 V13 U12 V12 W11 Y10 V10 Y9 V9 U9 Y7 U8 Y6	The bi-directional test mode data bus (TDAT[15:0]) carries data read from or written to FREEDM-8 registers during production test. In normal operation (PMCTEST set low), TDAT[15:0] should be left unconnected.

4.5 Don’t Care Signals (58)

Pin Name	Type	Pin No.	Feature
X	Input	B17 C16 B7 C7 B6 A5 D6 A4 V4 W4 T20 R17 U20 T17 V17 W17 V16 W16 V15 Y15 U13 Y14 W13 Y13 W12 V11 W10 U10 W9 W8 V8 W7 V7 W6 A17 D15	The Don't Care pins X may be connected to logic high or logic low arbitrarily. Optionally, they may be left floating.

X	Input	A16 B15 C14 B14 C13 B13 B12 D11 B11 C10 B9 A8 B8 A7 D8 A6 C6 B5 C5 B4 U5 Y4	The Don't Care pins X may be connected to logic high or logic low arbitrarily. Optionally, they may be left floating.

4.6 No Connect Signals (10)

Pin Name	Type	Pin No.	Feature
NC[9:0]	Open	D17 U17 R18 T19 T18 U19 U18 U16 Y17 U15	The No-Connect pins NC[9:0] must be left unconnected.

4.7 Power and Ground Signals (60)

Pin Name	Type	Pin No.	Feature
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18 VDD19 VDD20 VDD21 VDD22 VDD23 VDD24 VDD25 VDD26 VDD27 VDD28	Power	B2 B3 B18 B19 C2 C3 C18 C19 D7 D10 D14 G4 G17 K17 L4 P4 P17 U7 U11 U14 V2 V3 V18 V19 W2 W3 W18 W19	The DC power pins should be connected to a well decoupled +3.3 V DC supply.

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32	Ground	A1 A2 A3 A9 A10 A13 A18 A19 A20 B1 B20 C1 C20 H1 J20 K20 L1 M1 N20 V1 V20 W1 W20 Y1 Y2 Y3 Y8 Y11 Y12 Y18 Y19 Y20	The DC ground pins should be connected to ground.

Notes on Pin Description:

1. All FREEDM-8 inputs and bi-directionals present minimum capacitive loading and operate at TTL compatible logic levels. PCI signals conform to the 5 Volt signaling environment.

2. Most FREEDM-8 digital outputs and bi-directionals have 4 mA drive capability, except the PCICLKO, TD[0], TD[1], TD[2] and REQB outputs which have 6 mA drive capability.

3. Inputs TMS, TDI and TRSTB are Schmitt triggered and have internal pull-up resistors.

4. Inputs RD[7:0], RCLK[7:0], TCLK[7:0], SYSCLK, PCICLK, TBD, RSTB, GNTB, IDSEL, LOCKB, PMCTEST, TA[11:0], TRDB, TWRB, and TDAT[15:0] are Schmitt triggered.

5. To avoid damage to the device, the VBIAS[3:1] signals must be connected together externally and must be kept at a voltage that is equal to or higher than the VDD[28:1] power supplies.

5 FREEDM 32 FOOTPRINT

The FREEDM-32 is in a 256 pin ball grid array package.

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	VSS	RCLK[8]	RCLK[10]	RD[12]	RD[14]	VSS	RD[17]	RD[19]	VSS	VSS	RCLK[21]	RCLK[23]	RCLK[25]	RD[27]	RD[29]	VSS	VSS	VSS	A
B	VSS	VDD	VDD	RD[8]	RD[10]	RCLK[11]	RCLK[13]	RCLK[15]	RCLK[16]	RCLK[18]	RD[20]	RCLK[20]	RCLK[22]	RD[24]	RD[26]	RCLK[27]	RCLK[29]	VDD	VDD	VSS	B
C	VSS	VDD	VDD	RD[7]	RD[9]	RD[11]	RCLK[12]	RCLK[14]	RD[16]	RD[18]	RCLK[19]	RD[21]	RD[23]	RD[25]	RCLK[26]	RCLK[28]	PCICLK	VDD	VDD	VSS	C
D	RD[5]	RCLK[5]	RCLK[6]	NC	RCLK[7]	RCLK[9]	VDD	RD[13]	RD[15]	RCLK[17]	VDD	RD[22]	RCLK[24]	VDD	RD[28]	PCICLKO	VBIAS[2]	GNTB	AD[31]	AD[30]	D
E	RD[3]	RCLK[3]	RCLK[4]	RD[6]													REQB	AD[29]	AD[27]	AD[26]	E
F	RCLK[1]	RD[2]	RCLK[2]	RD[4]													AD[28]	AD[25]	AD[24]	CBEB[3]	F
G	RBCLK	RD[0]	RD[1]	VDD													VDD	IDSEL	AD[22]	AD[21]	G
H	VBIAS[1]	SYSCLK	RBD	RCLK[0]													AD[23]	AD[20]	AD[18]	VSS	H
J	VSS	TCK	TMS	TRSTB													AD[19]	AD[17]	AD[16]	CBEB[2]	J
K	VSS	TDI	TDO	VDD					BOTTOM VIEW								FRAMEB	IRDYB	TRDYB	DEVSELB	K
L	TD[0]	TCLK[0]	TD[1]	TCLK[1]													VDD	STOPB	LOCKB	VSS	L
M	TD[2]	TCLK[2]	TD[3]	TD[4]													CBEB[1]	SERRB	PERRB	VSS	M
N	VSS	TCLK[3]	TCLK[4]	TD[6]													AD[11]	AD[14]	AD[15]	PAR	N
P	TD[5]	TCLK[5]	TCLK[6]	VDD													VDD	AD[10]	AD[12]	AD[13]	P
R	TD[7]	TCLK[7]	TD[8]	TCLK[9]													AD[5]	CBEB[0]	AD[8]	AD[9]	R
T	TCLK[8]	TD[9]	TD[10]	TCLK[11]													AD[1]	AD[4]	AD[6]	AD[7]	T
U	TCLK[10]	TD[11]	TD[12]	NC	TD[13]	TD[15]	VDD	TCLK[18]	TD[21]	VDD	TCLK[25]	TD[28]	TD[30]	VDD	PMCTEST	RCLK[30]	VBIAS[3]	AD[0]	AD[2]	AD[3]	U
V	VSS	VDD	VDD	TCLK[12]	TCLK[14]	TCLK[16]	TD[18]	TD[20]	TD[22]	TCLK[23]	TD[25]	TD[27]	TCLK[28]	TCLK[30]	TBD	PCIINTB	RD[30]	VDD	VDD	VSS	V
W	VSS	VDD	VDD	TCLK[13]	TCLK[15]	TD[17]	TD[19]	TCLK[20]	TCLK[22]	TD[23]	TCLK[24]	TCLK[26]	TCLK[27]	TCLK[29]	TCLK[31]	RSTB	RD[31]	VDD	VDD	VSS	W
Y	VSS	VSS	VSS	TD[14]	TD[16]	TCLK[17]	TCLK[19]	TCLK[21]	VSS	VSS	TD[24]	TD[26]	VSS	TD[29]	TD[31]	TBCLK	RCLK[31]	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

6 FREEDM-32 PIN DESCRIPTION

6.1 Line Side Interface Signals (132)

Pin Name	Type	Pin No.	Function
RCLK[0] RCLK[1] RCLK[2] RCLK[3] RCLK[4] RCLK[5] RCLK[6] RCLK[7] RCLK[8] RCLK[9] RCLK[10] RCLK[11] RCLK[12] RCLK[13] RCLK[14] RCLK[15] RCLK[16] RCLK[17] RCLK[18] RCLK[19] RCLK[20] RCLK[21] RCLK[22] RCLK[23] RCLK[24] RCLK[25] RCLK[26] RCLK[27] RCLK[28] RCLK[29] RCLK[30] RCLK[31]	Input	H17 F20 F18 E19 E18 D19 D18 D16 A17 D15 A16 B15 C14 B14 C13 B13 B12 D11 B11 C10 B9 A8 B8 A7 D8 A6 C6 B5 C5 B4 U5 Y4	The receive line clock signals (RCLK[31:0]) contain the recovered line clock for the 32 independently timed links. Processing of the receive links are on a priority basis, in descending order from RCLK[0] to RCLK[31]. Therefore, the highest rate link should be connected to RCLK[0] and the lowest to RCLK[31]. RD[31:0] is sampled on the rising edge of the corresponding RCLK[31:0] clock. For channelised T1 or E1 links, RCLK[n] must be gapped during the framing bit (for T1 interfaces) or during time-slot 0 (for E1 interfaces) of the RD[n] stream. The FREEDM-32 uses the gapping information to determine the time-slot alignment in the receive stream. RCLK[31:0] is nominally a 50% duty cycle clock of 1.544 MHz for T1 links and 2.048 MHz for E1 links. For unchannelised links, RCLK[n] must be externally gapped during the bits or time-slots that are not part of the transmission format payload (i.e. not part of the HDLC packet). RCLK[2:0] is nominally a 50% duty cycle clock between 0 and 52 MHz. RCLK[31:3] is nominally a 50% duty cycle clock between 0 and 10 MHz.

RD[0] RD[1] RD[2] RD[3] RD[4] RD[5] RD[6] RD[7] RD[8] RD[9] RD[10] RD[11] RD[12] RD[13] RD[14] RD[15] RD[16] RD[17] RD[18] RD[19] RD[20] RD[21] RD[22] RD[23] RD[24] RD[25] RD[26] RD[27] RD[28] RD[29] RD[30] RD[31]	Input	G19 G18 F19 E20 F17 D20 E17 C17 B17 C16 B16 C15 A15 D13 A14 D12 C12 A12 C11 A11 B10 C9 D9 C8 B7 C7 B6 A5 D6 A4 V4 W4	The receive data signals (RD[31:0]) contain the recovered line data for the 32 independently timed links in normal mode (PMCTEST set low). Processing of the receive links are on a priority basis, in descending order form RD[0] to RD[31]. Therefore, the highest rate link should be connected to RD[0] and the lowest to RD[31]. For channelised links, RD[n] contains the 24 (T1) or 31 (E1) time-slots that comprise the channelised link. RCLK[n] must be gapped during the T1 framing bit position or the E1 frame alignment signal (time-slot 0). The FREEDM-32 uses the location of the gap to determine the channel alignment on RD[n]. For unchannelised links, RD[n] contains the HDLC packet data. For certain transmission formats, RD[n] may contain place holder bits or time-slots. RCLK[n] must be externally gapped during the place holder positions in the RD[n] stream. The FREEDM-32 supports a maximum data rate of 10 Mbit/s on an individual RD[31:3] link and a maximum data rate of 52 Mbit/s on RD[2:0]. RD[31:0] is sampled on the rising edge of the corresponding RCLK[31:0] clock.
RBD	Tri-state Output	H18	The receive BERT data signal (RBD) contains the receive bit error rate test data. RBD reports the data on the selected one of the receive data signals (RD[31:0]) and is updated on the falling edge of RBCLK. RBD may be tri-stated by setting the RBEN bit in the FREEDM-32 Master BERT Control register low.

RBCLK	Tri-state Output	G20	The receive BERT clock signal (RBCLK) contains the receive bit error rate test clock. RBCLK is a buffered version of the selected one of the receive clock signals (RCLK[31:0]). RBCLK may be tri-stated by setting the RBEN bit in the FREEDM-32 Master BERT Control register low.
TCLK[0] TCLK[1] TCLK[2] TCLK[3] TCLK[4] TCLK[5] TCLK[6] TCLK[7] TCLK[8] TCLK[9] TCLK[10] TCLK[11] TCLK[12] TCLK[13] TCLK[14] TCLK[15] TCLK[16] TCLK[17] TCLK[18] TCLK[19] TCLK[20] TCLK[21] TCLK[22] TCLK[23] TCLK[24] TCLK[25] TCLK[26] TCLK[27] TCLK[28] TCLK[29] TCLK[30] TCLK[31]	Input	L19 L17 M19 N19 N18 P19 P18 R19 T20 R17 U20 T17 V17 W17 V16 W16 V15 Y15 U13 Y14 W13 Y13 W12 V11 W10 U10 W9 W8 V8 W7 V7 W6	The transmit line clock signals (TCLK[31:0]) contain the transmit clocks for the 32 independently timed links. Processing of the transmit links is on a priority basis, in descending order from TCLK[0] to TCLK[31]. Therefore, the highest rate link should be connected to TCLK[0] and the lowest to TCLK[31]. TD[31:0] is updated on the falling edge of the corresponding TCLK[31:0] clock. For channelised T1 or E1 links, TCLK[n] must be gapped during the framing bit (for T1 interfaces) or during time-slot 0 (for E1 interfaces) of the TD[n] stream. The FREEDM-32 uses the gapping information to determine the time-slot alignment in the transmit stream. For unchannelised links, TCLK[n] must be externally gapped during the bits or time-slots that are not part of the transmission format payload (i.e. not part of the HDLC packet). TCLK[31:3] is nominally a 50% duty cycle clock between 0 and 10 MHz. TCLK[2:0] is nominally a 50% duty cycle clock between 0 and 52 MHz. Typical values for TCLK[31:0] include 1.544 MHz (for T1 links) and 2.048 MHz (for E1 links).

TD[0] TD[1] TD[2] TD[3] TD[4] TD[5] TD[6] TD[7] TD[8] TD[9] TD[10] TD[11] TD[12] TD[13] TD[14] TD[15] TD[16] TD[17] TD[18] TD[19] TD[20] TD[21] TD[22] TD[23] TD[24] TD[25] TD[26] TD[27] TD[28] TD[29] TD[30] TD[31]	Output	L20 L18 M20 M18 M17 P20 N17 R20 R18 T19 T18 U19 U18 U16 Y17 U15 Y16 W15 V14 W14 V13 U12 V12 W11 Y10 V10 Y9 V9 U9 Y7 U8 Y6	The transmit data signals (TD[31:0]) contains the transmit data for the 32 independently timed links in normal mode (PMCTEST set low). Processing of the transmit links are on a priority basis, in descending order from TD[0] to TD[31]. Therefore, the highest rate link should be connected to TD[0] and the lowest to TD[31]. For channelised links, TD[n] contains the 24 (T1) or 31 (E1) time-slots that comprise the channelised link. TCLK[n] must be gapped during the T1 framing bit position or the E1 frame alignment signal (time-slot 0). The FREEDM-32 uses the location of the gap to determine the channel alignment on TD[n]. For unchannelised links, TD[n] contains the HDLC packet data. For certain transmission formats, TD[n] may contain place holder bits or time-slots. TCLK[n] must be externally gapped during the place holder positions in the TD[n] stream. The FREEDM-32 supports a maximum data rate of 10 Mbit/s on an individual TD[31:3] link and a maximum data rate of 52 Mbit/s on TD[2:0]. TD[31:0] is updated on the falling edge of the corresponding TCLK[31:0] clock.
TBD	Input	V6	The transmit BERT data signal (TBD) contains the transmit bit error rate test data. When the TBERTEN bit in the BERT Control register is set high, the data on TDB is transmitted on the selected one of the transmit data signals (TD[31:0]). TBD is sampled on the rising edge of TBCLK.

TBCLK	Tri-state Output	Y5	The transmit BERT clock signal (TBCLK) contains the transmit bit error rate test clock. TBCLK is a buffered version of the selected one of the transmit clock signals (TCLK[31:0]). TBCLK may be tri-stated by setting the TBEN bit in the FREEDM-32 Master BERT Control register low.

6.2 PCI Host Interface Signals (51)

Pin Name	Type	Pin No.	Feature
PCICLK	Input	C4	The PCI clock signal (PCICLK) provides timing for PCI bus accesses. PCICLK is a nominally 50% duty cycle, 0 to 33 MHz clock.
PCICLKO	Output	D5	The PCI clock output signal (PCICLKO) is a buffered version of the PCICLK. PCICLKO may be used to drive the SYSCLK input.

AD[0] AD[1] AD[2] AD[3] AD[4] AD[5] AD[6] AD[7] AD[8] AD[9] AD[10] AD[11] AD[12] AD[13] AD[14] AD[15] AD[16] AD[17] AD[18] AD[19] AD[20] AD[21] AD[22] AD[23] AD[24] AD[25] AD[26] AD[27] AD[28] AD[29] AD[30] AD[31]	I/O	U3 T4 U2 U1 T3 R4 T2 T1 R2 R1 P3 N4 P2 P1 N3 N2 J2 J3 H2 J4 H3 G1 G2 H4 F2 F3 E1 E2 F4 E3 D1 D2	The PCI address and data bus (AD[31:0]) carries the PCI bus multiplexed address and data. During the first clock cycle of a transaction, AD[31:0] contains a physical byte address. During subsequent clock cycles of a transaction, AD[31:0] contains data. A transaction is defined as an address phase followed by one or more data phases. When Little-Endian byte formatting is selected, AD[31:24] contain the most significant byte of a DWORD while AD[7:0] contain the least significant byte. When Big-Endian byte formatting is selected. AD[7:0] contain the most significant byte of a DWORD while AD[31:24] contain the least significant byte. When the FREEDM-32 is the initiator, AD[31:0] is an output bus during the first (address) phase of a transaction. For write transactions, AD[31:0] remains an output bus for the data phases of the transaction. For read transactions, AD[31:0] is an input bus during the data phases. When the FREEDM-32 is the target, AD[31:0] is an input bus during the first (address) phase of a transaction. For write transactions, AD[31:0] remains an input bus during the data phases of the transaction. For read transactions, AD[31:0] is an output bus during the data phases. When the FREEDM-32 is not involved in the current transaction, AD[31:0] is tri-stated. As an output bus, AD[31:0] is updated on the rising edge of PCICLK. As an input bus, AD[31:0] is sampled on the rising edge of PCICLK.

C/BEB[0] C/BEB[1] C/BEB[2] C/BEB[3]	I/O	R3 M4 J1 F1	The PCI bus command and byte enable bus (C/BEB[3:0]) contains the bus command or the byte valid indications. During the first clock cycle of a transaction, C/BEB[3:0] contains the bus command code. For subsequent clock cycles, C/BEB[3:0] identifies which bytes on the AD[31:0] bus carry valid data. C/BEB[3] is associated with byte 3 (AD[31:24]) while C/BEB[0] is associated with byte 0 (AD[7:0]). When C/BEB[n] is set high, the associated byte is invalid. When C/BEB[n] is set low, the associated byte is valid. When the FREEDM-32 is the initiator, C/BEB[3:0] is an output bus. When the FREEDM-32 is the target, C/BEB[3:0] is an input bus. When the FREEDM-32 is not involved in the current transaction, C/BEB[3:0] is tri-stated. As an output bus, C/BEB[3:0] is updated on the rising edge of PCICLK. As an input bus, C/BEB[3:0] is sampled on the rising edge of PCICLK.
PAR	I/O	N1	The parity signal (PAR) indicates the parity of the AD[31:0] and C/BEB[3:0] buses. Even parity is calculated over all 36 signals in the buses regardless of whether any or all the bytes on the AD[31:0] are valid. PAR always reports the parity of the previous PCICLK cycle. Parity errors detected by the FREEDM-32 are indicated on output PERRB and in the FREEDM-32 Interrupt Status register. When the FREEDM-32 is the initiator, PAR is an output for writes and an input for reads. When the FREEDM-32 is the target, PAR is an input for writes and an output for reads. When the FREEDM-32 is not involved in the current transaction, PAR is tri-stated. As an output signal, PAR is updated on the rising edge of PCICLK. As an input signal, PAR is sampled on the rising edge of PCICLK.

FRAMEB	I/O	K4	The active low cycle frame signal (FRAMEB) identifies a transaction cycle. When FRAMEB transitions low, the start of a bus transaction is indicated. FRAMEB remains low to define the duration of the cycle. When FRAMEB transitions high, the last data phase of the current transaction is indicated. When the FREEDM-32 is the initiator, FRAMEB is an output. When the FREEDM-32 is the target, FRAMEB is an input. When the FREEDM-32 is not involved in the current transaction, FRAMEB is tri-stated. As an output signal, FRAMEB is updated on the rising edge of PCICLK. As an input signal, FRAMEB is sampled on the rising edge of PCICLK.
TRDYB	I/O	K2	The active low target ready signal (TRDYB) indicates when the target is ready to start or continue with a transaction. TRDYB works in conjunction with IRDYB to complete transaction data phases. During a transaction in progress, TRDYB is set high to indicate that the target cannot complete the current data phase and to force a wait state. TRDYB is set low to indicate that the target can complete the current data phase. The data phase is completed when TRDYB is set low and the initiator ready signal (IRDYB) is also set low. When the FREEDM-32 is the initiator, TRDYB is an input. When the FREEDM-32 is the target, TRDYB is an output. During accesses to FREEDM-32 registers, TRDYB is set high to extend data phases over multiple PCICLK cycles. When the FREEDM-32 is not involved in the current transaction, TRDYB is tri-stated. As an output signal, TRDYB is updated on the rising edge of PCICLK. As an input signal, TRDYB is sampled on the rising edge of PCICLK.

IRDYB	I/O	K3	The active low initiator ready (IRDYB) signal is used to indicate whether the initiator is ready to start or continue with a transaction. IRDYB works in conjunction with TRDYB to complete transaction data phases. When IRDYB is set high and a transaction is in progress, the initiator is indicating it cannot complete the current data phase and is forcing a wait state. When IRDYB is set low and a transaction is in progress, the initiator is indicating it has completed the current data phase. The data phase is completed when IRDYB is set low and the target ready signal (IRDYB) is also set low. When the FREEDM-32 is the initiator, IRDYB is an output. When the FREEDM-32 is the target, IRDYB is an input. When the FREEDM-32 is not involved in the current transaction, IRDYB is tri-stated. IRDYB is updated on the rising edge of PCICLK or sampled on the rising edge of PCICLK depending on whether it is an output or an input.
STOPB	I/O	L3	The active low stop signal (STOPB) requests the initiator to stop the current bus transaction. When STOPB is set high by a target, the initiator continues with the transaction. When STOPB is set low, the initiator will stop the current transaction. When the FREEDM-32 is the initiator, STOPB is an input. When STOPB is sampled low, the FREEDM-32 will terminate the current transaction in the next PCICLK cycle. When the FREEDM-32 is the target, STOPB is an output. The FREEDM-32 only issues transaction stop requests when its internal bus latency buffers are in a near overflow state. When the FREEDM-32 is not involved in the current transaction, STOPB is tri-stated. STOPB is updated on the rising edge of PCICLK or sampled on the rising edge of PCICLK depending on whether it is an output or an input.

IDSEL	Input	G3	The initialization device select signal (IDSEL) enables read and write access to the PCI configuration registers. When IDSEL is set high during the address phase of a transaction and the C/BEB[3:0] code indicates a register read or write, the FREEDM-32 performs a PCI configuration register transaction and asserts the DEVSELB signal in the next PCICLK period. IDSEL is sampled on the rising edge of PCICLK.
DEVSELB	I/O	K1	The active low device select signal (DEVSELB) indicates that a target claims the current bus transaction. During the address phase of a transaction, all targets decode the address on the AD[31:0] bus. When a target, recognizes the address as its own, it sets DEVSELB low to indicate to the initiator that the address is valid. If no target claims the address in six bus clock cycles, the initiator assumes that the target does not exist or cannot respond and aborts the transaction. When the FREEDM-32 is the initiator, DEVSELB is an input. If no target responds to an address in six PCICLK cycles, the FREEDM-32 will abort the current transaction and alerts the PCI Host via an interrupt. When the FREEDM-32 is the target, DEVSELB is an output. DELSELB is set low when the address on AD[31:0] is recognised. When the FREEDM-32 is not involved in the current transaction, DEVSELB is tri-stated. FREEDM-32 is updated on the rising edge of PCICLK or sampled on the rising edge of PCICLK depending on whether it is an output or an input.

LOCKB	Input	L2	The active low bus lock signal (LOCKB) locks a target device. When LOCKB and FRAME are set low, and the FREEDM-32 is the target, an initiator is locking the FREEDM-32 as an "owned" target. Under these circumstances, the FREEDM-32 will reject all transaction with other initiators. The FREEDM-32 will continue to reject other initiators until its owner releases the lock by forcing both FRAMEB and LOCKB high. As a initiator, the FREEDM-32 will never lock a target. LOCKB is sampled using the rising edge of PCICLK.
REQB	Output	E4	The active low PCI bus request signal (REQB) requests an external arbiter for control of the PCI bus. REQB is set low when the FREEDM-32 desires access to the host memory. REQB is set high when access is not desired. REQB is updated on the rising edge of PCICLK.
GNTB	Input	D3	The active low PCI bus grant signal (GNTB) indicates the granting of control over the PCI in response to a bus request via the REQB output. When GNTB is set high, the FREEDM-32 does not have control over the PCI bus. When GNTB is set low, the external arbiter has granted the FREEDM-32 control over the PCI bus. However, the FREEDM-32 will not proceed until the FRAMEB signal is sampled high, indicating no current transactions are in progress. GNTB is sampled on the rising edge of PCICLK.
PCIINTB	OD Output	V5	The active low PCI interrupt signal (PCIINTB) is set low when a FREEDM-32 interrupt source is active, and that source is unmasked. The FREEDM-32 may be enabled to report many alarms or events via interrupts. PCIINTB returns high when the interrupt is acknowledged via an appropriate register access. PCIINTB is an open drain output and is updated on the rising edge of PCICLK.

PERRB	I/O	M2	The active low parity error signal (PERRB) indicates a parity error over the AD[31:0] and C/BEB[3:0] buses. Parity error is detect when even parity calculations do not match the PAR signal. PERRB is set low at the cycle immediately following an offending PAR cycle. PERRB is set high when no parity error is detected. PERRB is enabled by setting the PERREN bit in the Control/Status register in the PCI Configuration registers space. Regardless of the setting of PERREN, parity errors are always reported by the PERR bit in the Control/Status register in the PCI Configuration registers space. PERRB is updated on the rising edge of PCICLK.
SERRB	OD Output	M3	The active low system error signal (SERRB) indicates an address parity error. Address parity errors are detected when the even parity calculations during the address phase do not match the PAR signal. When the FREEDM-32 detects a system error, SERRB is set low for one PCICLK period. SERRB is enabled by setting the SERREN bit in the Control/Status register in the PCI Configuration registers space. Regardless of the setting of SERREN, parity errors are always reported by the SERR bit in the Control/Status register in the PCI Configuration registers space. SERRB is an open drain output and is updated on the rising edge of PCICLK.

6.3 Miscellaneous Interface Signals (13)

Pin Name	Type	Pin No.	Feature
SYSCLK	Input	H19	The system clock (SYSCLK) provides timing for the core logic. SYSCLK is nominally a 50% duty cycle 25 MHz to 33 MHz clock.
RSTB	Input	W5	The active low reset signal (RSTB) signal provides an asynchronous FREEDM-32 reset, RSTB is an asynchronous input. When RSTB is set low, all FREEDM-32 registers are forced to their default states. In addition, TD[31:0] are forced high and all PCI ouput pins are forced tri-state and will remain high or tri-stated, respectively, until RSTB is set high.
PMCTEST	Input	U6	The PMC production test enable signal (PMCTEST) places the FREEDM-32 is test mode. When PMCTEST is set high, production test vectors can be executed to verify manufacturing via the test mode interface signals TA[10:0], TA[11]/TRS, TRDB, TWRB and TDAT[15:0]. PMCTEST is set low in normal operation. PMCTEST is an asynchronous input and has an integral pull-down resistor.
TCK	Input	J19	The test clock signal (TCK) provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. TMS and TDI are sampled on the rising edge of TCK. TDO is updated on the falling edge of TCK.
TMS	Input	J18	The test mode select signal (TMS) controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	K19	The test data input signal (TDI) carries test data into the FREEDM-32 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.

TDO	Tri-state	K18	The test data output signal (TDO) carries test data out of the FREEDM-32 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	J17	The active low test reset signal (TRSTB) provides an asynchronous FREEDM-32 test access port reset via the IEEE P1149.1 test access port. TRSTB is an asynchronous input with an integral pull up resistor. Note that when TRSTB is not being used, it must be connected to the RSTB input.
VBIAS[3:1]	Input	U4 D4 H20	The bias signals (VBIAS[3:1]) provide 5 Volt bias to input and I/O pads to allow the FREEDM-32 to tolerate connections to 5 Volt devices.
NC1	Open	D17	This pin must be left unconnected.
NC2	Open	U17	This pin must be left unconnected.

6.4 Production Test Interface Signals (0 - Multiplexed)

Pin Name	Type	Pin No.	Feature
TA[0] TA[1] TA[2] TA[3] TA[4] TA[5] TA[6] TA[7] TA[8] TA[9] TA[10] TA[11]/TRS	Input		The test mode address bus (TA[10:0]) selects specific registers during production test (PMCTEST set high) read and write accesses. TA[10:0] replace RD[20:10] when PMCTEST is set high. The test register select signal (TA[11]/TRS) selects between normal and test mode register accesses during production test (PMCTEST set high). TRS is set high to select test registers and is set low to select normal registers. TA[11]/TRS replaces RD[21] when PMCTEST is set high.
TRDB	Input		The test mode read enable signal (TRDB) is set low during FREEDM-32 register read accesses during production test (PMCTEST set high). The FREEDM-32 drives the test data bus (TDAT[15:0]) with the contents of the addressed register while TRDB is low. TRDB replaces RD[22] when PMCTEST is set high.
TWRB	Input		The test mode write enable signal (TWRB) is set low during FREEDM-32 register write accesses during production test (PMCTEST set high). The contents of the test data bus (TDAT[15:0]) are clocked into the addressed register on the rising edge of TWRB. TWRB replaces RD[23] when PMCTEST is set high.

TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	I/O		The bi-directional test mode data bus (TDAT[15:0]) carries data read from or written to FREEDM-32 registers during production test. TDAT[15:0] replace TD[31:16] when PMCTEST is set high.

6.5 Power and Ground Signals (60)

Pin Name	Type	Pin No.	Feature
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18 VDD19 VDD20 VDD21 VDD22 VDD23 VDD24 VDD25 VDD26 VDD27 VDD28	Power	B2 B3 B18 B19 C2 C3 C18 C19 D7 D10 D14 G4 G17 K17 L4 P4 P17 U7 U11 U14 V2 V3 V18 V19 W2 W3 W18 W19	The DC power pins should be connected to a well decoupled +3.3 V DC supply.

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32	Ground	A1 A2 A3 A9 A10 A13 A18 A19 A20 B1 B20 C1 C20 H1 J20 K20 L1 M1 N20 V1 V20 W1 W20 Y1 Y2 Y3 Y8 Y11 Y12 Y18 Y19 Y20	The DC ground pins should be connected to ground.

Notes on Pin Description:

1. All FREEDM-32 inputs and bi-directionals present minimum capacitive loading and operate at TTL compatible logic levels. PCI signals conform to the 5 Volt signaling environment.

2. Most FREEDM-32 digital outputs and bi-directionals have 4 mA drive capability, except the PCICLKO, TD[0], TD[1], TD[2] and REQB outputs which have 6 mA drive capability.

3. Inputs TMS, TDI and TRSTB are Schmitt triggered and have internal pull-up resistors.

4. Inputs RD[31:0], RCLK[31:0], TCLK[31:0], SYSCLK, PCICLK, TBD, RSTB, GNTB, IDSEL, LOCKB, PMCTEST are Schmitt triggered.

5. To avoid damage to the device, the VBIAS[3:1] signals must be connected together externally and must be kept at a voltage that is equal to or higher than the VDD[28:1] power supplies.

NOTES

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