PM7323

ASYNCHRONOUS SRAM FOR RCMP-200

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REFERENCE

[1] PMC-940904, "PM7322 RCMP Datasheet", Issue 4, PMC-Sierra Inc., March 1996.

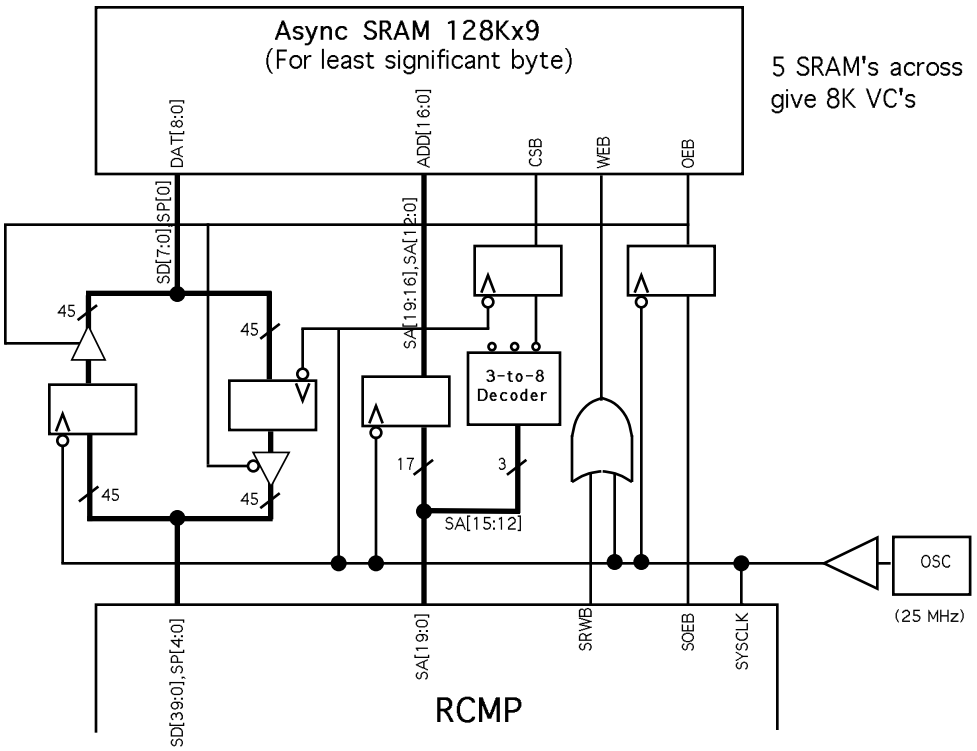
INTRODUCTION

The RCMP-200 is targeted at lowering the cost of switch port cards, where the aggregate data rate is less than 200 Mbps. The number of SRAM's required by the RCMP-200 to process the potentially large number of virtual connections (VC's) is still substantial. To further lower the cost per port card, asynchronous SRAM's, as opposed to expensive synchronous SRAM's, can be used with the RCMP-200 with the help of some glue logic. This application note describes the necessary glue logic and the timing considerations.

CIRCUIT DESCRIPTION

Fig. 1 shows the glue logic between the synchronous SRAM interface of the RCMP-200 and the asynchronous SRAM. The size of the SRAM is chosen to be 128Kx9, with 12ns access time[1]. Five of these SRAM's across make up the 45-bit word required, which includes 40 bits of data and 5 bits of parity. These constitute a bank of memory that corresponds to 8K VC's. Only one of the SRAM's is shown in the figure to illustrate the glue logic. It is quite straight-forward to apply this to larger configurations.

Fig. 1 Asynchronous SRAM Glue Logic



There are two main factors in designing this glue logic:

1. In a Read cycle, to align the read data out of the SRAM with the clock cycle expected by the synchronous RCMP-200 interface.

2. In a Write cycle, to align the timing of the address and data with the deassertion of the write-enable signal, which samples the data and writes it into memory.

[1]An example for this SRAM is the Cypress CY7C1088, which will be available by the end of 1996. Other SRAM sizes are available at the time of writing, such as 32k x 9 which will limit the number of VC's supported due to loading on the address/data buses. In any case, however, the same glue logic can be applied (with the exception that the address decoding will have to change).

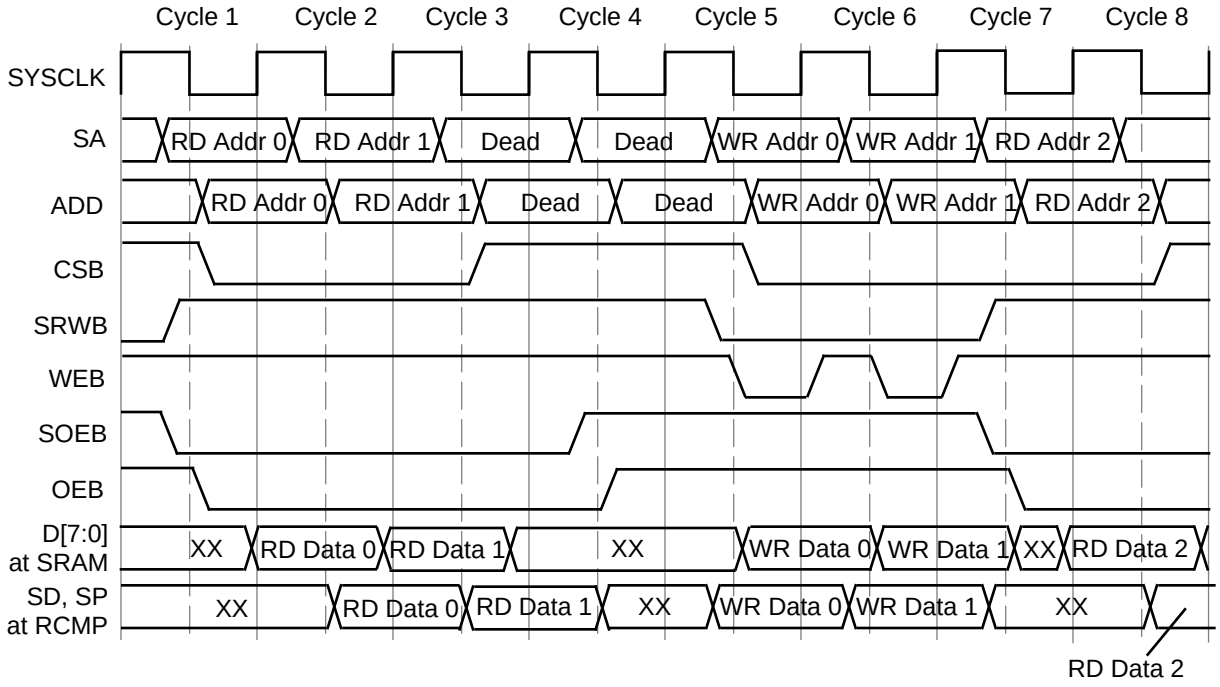
The first factor has to do with the Read operation of the RCMP-200[2], where the RCMP-200 outputs the SRAM address in one cycle and expects the Read data to be valid in the next clock cycle. As such, the Read data from the Asynchronous SRAM has to be retimed by a flip-flop, so that it can be held long enough for the RCMP-200 to sample. Hence the flip-flop in the returning data path. The reason for using a negative edge flip-flop will become clear in the next section.

The second factor deals with the problem of ensuring enough setup and hold times for the address/data with respect to the write enable (derived from SRWB of the RCMP-200) signal deassertion in a Write operation. The RCMP-200 toggles all its outputs after the positive edge of SYSCLK, and therefore, there is no guarantee of setup and hold between the address/data and SRWB. Two things are done by the glue logic to address this problem: 1) The write-enable (WEB) signal is generated by the OR of SRWB and SYSCLK, which effectively aligns the deassertion of WEB with the positive edge of SYSCLK. 2) The address and data are retimed by negative-edge flip-flop, so that they are centered with respect to WEB deassertion. The chip-select (CSB) and output-enable (OEB) signals are also retimed to align with the address/data.

[2]Please refer to Fig. 20 in [1], the Synchronous SRAM Interface Timing diagram.

TIMING CONSIDERATIONS

Fig. 2 Timing Diagram for Read and Write Operations



Two consecutive Read cycles are shown, followed by two consecutive Write cycles and finally another Read cycle. In the transition from a Read cycle to a Write cycle, two dead cycles are inserted to avoid conflict on the data bus. The first dead cycle (in Cycle 3) exists because Read data is expected back from the SRAM in that cycle. The RCMP-200 cannot start the Write cycle in Cycle 4 either, because SOEB is deasserted in Cycle 4 causing the SRAM to release the data bus. However, the RCMP-200 would drive the Write data in the same cycle, and there is no guarantee that the SRAM will release the bus early enough. There are no dead cycles in the transition from a Write cycle to a Read cycle, since only the RCMP-200 is driving the data bus before the transition and the bus will be tristated after.

In a Read cycle, say in Cycle 1, the RCMP-200 expects the Read data to be sampled at the beginning (positive edge of SYSCLK) of Cycle 3. To satisfy this, a flip-flop retimes the Read data out of the SRAM. The use of the negative edge of SYSCLK for retiming is because of the timing alignment required in a Write cycle.

In a Write cycle, say in Cycle 5, the OR of SRWB and SYSCLK effectively forces the deassertion of WEB to be on the positive edge of SYSCLK. The RCMP-200 outputs the address, data and SRWB on the positive edge, and they are retimed by negative-edge

flip-flops. This allows enough setup and hold times for the SRAM to sample the address and data on the deassertion of WEB.

The following timing constraints are important to be observed (note that RCMP-200 operates with a 25MHz SYSCLK, ie. a 40ns clock period):

1. The address decoder to generate the chip-selects must be fast, since the chip-selects have to retimed by the negative-edge flip-flop. With a half-period of 20ns and a RCMP-200 prop delay of 12ns at 20pF load (which applies here since the decoder is the only load on the address lines SA[15:12]), there is only 8ns left for the address decoder and the setup time of the flip-flop. It is recommended to use the fastest decoder or a PAL available today that has a prop delay of less than 5ns.

2. The SRAM uses the address and chip-select retimed by the flip-flops on the negative edge of SYSCLK, and outputs the Read data, which will be sampled by another flip-flop on the next negative edge of SYSCLK. Therefore, the SRAM access time must be less than 40ns minus the prop delay of the flip-flop that retimes the address, the prop delay of the tristate buffer, and the setup time of the flip-flop that retimes the Read data. Assuming 9ns prop delay and 2.5 ns setup time for the flip-flop, 5ns for the prop delay of the tristate buffer, the SRAM access time will have to be less than 21ns.

3. As a result of Constraint 1, assuming an address decoder prop delay of 5ns, the flip-flop should have a setup time of less than 3ns. Also, the flip-flop prop delay should be less than 11ns, because of the data bus path going from a flip-flop, through a tristate buffer (assuming a delay of 5ns) and into the RCMP-200 (with a setup time of 4ns). The use of tristatable flip-flop will improve the margins significantly.

4. The minimum width of WEB required by the SRAM should be greater than that provided by the OR of SRWB and SYSCLK, which is: the SYSCLK low pulse width. The maximum SYSCLK duty cycle allowed by the RCMP-200 is 60%, resulting in a low pulse width of 16ns. Therefore, the minimum width of WEB is 16ns.

SUMMARY

This application note describes the glue logic for the use of asynchronous SRAM's with the RCMP-200. Negative-edge retiming is used to align the synchronous signals of the RCMP-200 with the asynchronous requirements of the SRAM. Since the cost of the asynchronous SRAM's are at least half that of the synchronous counterparts, the cost savings (especially with large SRAM configurations) will more than make up for the overhead incurred by the glue logic.

NOTES

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