Ordering number : EN ———

Monolithic linear IC

LA9606W

RF/Matrix Signal Processing IC for MD Player

Preliminaly

Overview

The LA9606W is an IC for servo error signal generation, RF signal processing, and binarized output of wobble signals for mini disc playback. Combined with the LC89641, it can be used to configure an MD player.

Features

- Ultra-low current drain
- Servo error signal level freely settable by VCA
- Few peripheral components
- Ultra-miniature package

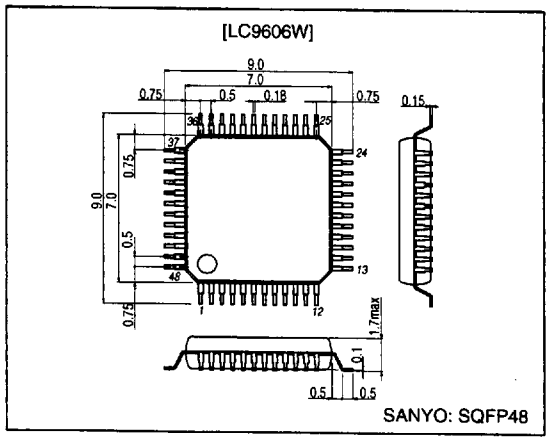
Functions

- I-V conversion amplifier for servo signal
- Pit/groove switching RF amplifier
- RF equalizer amplifier
- Servo signal VCA
- APC circuit
- Focus error amplifier
- Tracking error amplifier
- HFL circuit
- PEAK and BOTTOM output
- ADIP amplifier
- Prepit circuit (pit/groove discrimination circuit)
- ADIPCR

Package Dimensions

unit: mm

3163A-SQFP48



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
Allowable power dissipation	Pd max	Ta ≤ 75°C	100	mW
Operating temperature	Topr		−25 to +75	°C
Storage temperature	Tstg		−40 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		2.4	V
Operating supply voltage range	V_{CCop}		2.2 to 5.5	V

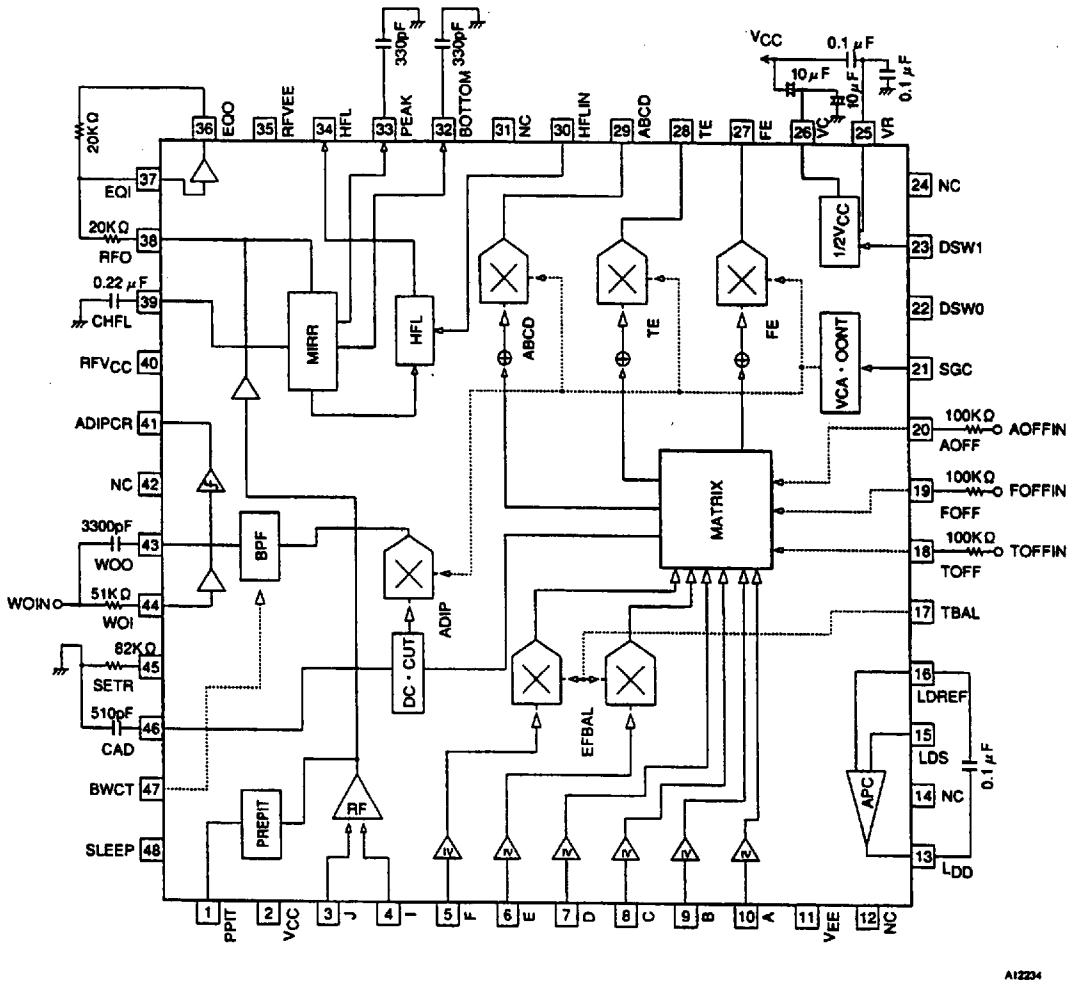
Electrical Characteristics at Ta = 25°C, V_{CC} = 2.4 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	DSW0 = DSW1 = 0 V	4.8	6.8	9.3	mA
Reference voltage	V_C	V_C	1.1	1.2	1.35	V
[RF AMP AL]						
Offset	RFALost	RFO: I = J = V_C, difference with V_C	−480	−340	−200	mV
Gain	RFALg	RFO/I : I = J	9.9	12.9	15.9	dB
[RF AMP GROVE]						
Offset	RFMGost	RFO: I = J = V_C, difference with V_C	−450	−320	−200	mV
Gain	RFMGg	RFO/I : J = V_C	29.5	32.5	35.5	dB
[RF AMP MO.PIT]						
Offset	RFMPost	RFO: I = J = V_C, difference with V_C	−480	−340	−200	mV
Gain	RFMPg	RFO/I : I = J	21.3	24.3	27.3	dB
[ABCD PIT]						
Offset	ABCDPost	ABCD: A = B = C = D = V_C, difference with V_C, SGC = 0.5 V	−830	−480	−250	mV
Gain	ABCDPg	ABCD/A (5 kHz) : A = B = C = D, SGC = 0.5 V	9.5	12	15.5	dB
−3dB	ABCDPfc	SGC = 0.5 V		18		kHz
[ABCD GROVE]						
Offset	ABCDMGost	ABCD: A = B = C = D = V_C, difference with V_C, SGC = 0.5 V	−830	−480	−250	mV
Gain	ABCDMGg	ABCD/A (5 kHz) : A = B = C = D, SGC = 0.5 V	6	9	12.5	dB
−3dB	ABCDMGfc	SGC = 0.5 V		60		kHz
[FE]						
Offset	FEost	FE: A = B = C = D = V_C, difference with V_C, SGC = 0.5 V	−120	0	+120	mV
Gain	FEg	FE/A (5 kHz) : A = −B = C = −D, SGC = 0.5 V	7.3	9.8	12.8	dB
−3dB	FEfc	SGC = 0.5 V		25		kHz
High-level output voltage	FEH	FE : A = C = V_C − 200 mV, B = D = V_C, SGC = 1.2 V	2.0	2.3	2.4	V
Low-level output voltage	FEL	FE : A = C = V_C, B = D = V_C − 200 mV, SGC = 1.2 V	0	0.1	0.4	V
[TE]						
Offset	TEost	TE: E = F = V_C, difference with V_C, SGC = 0.5 V	−400	0	+400	mV
Gain	TEg	TE/E (5 kHz) : E = −F, SGC = 0.5 V	22.9	25.9	28.9	dB
−3dB	TEfc	SGC = 0.5 V		30		kHz
High-level output voltage	TEH	TE : E = V_C − 100 mV, F = V_C, SGC = 0.7 V	2.0	2.3	2.4	V
Low-level output voltage	TEL	TE : F = V_C − 100 mV, E = V_C, SGC = 0.7 V	0	0.1	0.4	V
High-level balance range	BALH	TE : Δ Gain E /Fin, TBAL = 1.8 V, SGC = 0.5 V	3.3	5.3	7.8	dB
Low-level balance range	BALL	TE : Δ Gain E /Fin, TBAL = 0.8 V, SGC = 0.5 V	−7.8	−5.3	−3.3	dB
[ADIP]						
High-level output voltage	ADIPH	ADIPCR: WOI 51 kΩ, input V_C + 20 mV	2.0	2.3	2.4	V
Low-level output voltage	ADIPL	ADIPCR: WOI 51 kΩ, input V_C − 20 mV	0	0.1	0.4	V
[WOO]						
Gain	WOOg	WOO/A (22.05 kHz) : A = −B = −C = D BWCT = 1.2 V, SGC = 1.2 V	26	30.5	35	dB
f = 10 kHz	WOOfcL	WOO/A (10 kHz) : A = −B = −C = D Difference with WOOg, BWCT = 1.2 V, SGC = 1.2V	−13.5	−9.5	−5.5	dB
f = 30 kHz	WOOfcH	WOO/A (30 kHz) : A = −B = −C = D Difference with WOOg, BWCT = 1.2 V, SGC = 1.2 V	−8.5	−6	−2.5	dB
[APC]						
Reference voltage	LDS	LDD: LSD voltage such that LDREF = 0.2 V, LDD = 1.5 V	185	215	245	mV
OFF voltage	LDDof	LDD: DSW0 = DSW1 = 0 V	2.1	2.4		V
High-level output voltage	LDDH	LDD: LDREF = 0 V, LDS = 0.5 V	1.8	2.1	2.3	V
Low-level output voltage	LDDL	LDD: LDREF = 0.2 V, LDS = 0.1 V	50	120	250	mV
[HFL]						
High-level output voltage	HFLH	HFL: HFLIN = V_C − 70mV, DSW0 = 2.4 V, DSW1 = 0 V	2.0	2.3	2.4	V
Low-level output voltage	HFLL	HFL: HFLIN = V_C − 20mV, DSW0 = 2.4 V, DSW1 = 0 V	0	0.1	0.4	V

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PHBH]						
Output range	PHBH	PEAK-BOTTOM: I=J (1 MHz), level difference with RF0, DSW0=0V,DSW=2.4V	−150	−50	0	mV
[PREPIT]						
High-level output voltage	PPITH	PPIT: I = J = 200 kHz (50 mVp-p + V_C + 0.125 V), DSW0 = 2.4 V	2	2.3	2.4	V
Low-level output voltage	PPITL	PPIT: I = J = 20 kHz (50 mVp-p + V_C + 0.125 V), DSW0 = 2.4 V	0	0.1	0.4	V
HL switching time	PPITHL	PPIT: I = J = 200 kHz to 20 kHz (50 mVp-p + V_C + 0.125 V)	120	180	250	µs

Test Circuit



Equivalent Circuit