Freescale Semiconductor
Technical Data

Document Number: MC1321x
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MC1321x

Package Information
Case 1664-01
71-pin LGA [9x9 mm]

Ordering Information

Device	Device Marking	Package
MC13211[1]	13211	LGA
MC13212[1]	13212	LGA
MC13213[1]	13213	LGA

[1] See Table 1 for more details.

MC13211/212/213

ZigBee™ - Compliant Platform - 2.4 GHz Low Power Transceiver for the IEEE® 802.15.4 Standard plus Microcontroller

1 Introduction

The MC1321x family is Freescale's second-generation ZigBee platform which incorporates a low power 2.4 GHz radio frequency transceiver and an 8-bit microcontroller into a single 9x9x1 mm 71-pin LGA package. The MC1321x solution can be used for wireless applications from simple proprietary point-to-point connectivity to a complete ZigBee mesh network. The combination of the radio and a microcontroller in a small footprint package allows for a cost-effective solution.

The MC1321x contains an RF transceiver which is an 802.15.4 Standard compliant radio that operates in the 2.4 GHz ISM frequency band. The transceiver includes a low noise amplifier, 1mW nominal output power, PA with internal voltage controlled oscillator (VCO), integrated transmit/receive switch, on-board power supply regulation, and full spread-spectrum encoding and decoding.

The MC1321x also contains a microcontroller based on the HCS08 Family of Microcontroller Units (MCU), specifically the HCS08 Version A, and can provide up to 60KB of flash memory and 4KB of RAM. The onboard

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MCU allows the communications stack and also the application to reside on the same system-in-package (SIP). The MC1321x family is organized as follows:

- The MC13211 has 16KB of flash and 1KB of RAM and is an ideal solution for low cost, proprietary applications that require wireless point-to-point or star network connectivity. The MC13211 combined with the Freescale Simple MAC (SMAC) provides the foundation for proprietary applications by supplying the necessary source code and application examples to get users started on implementing wireless connectivity.
- The MC13212 contains 32K of flash and 2KB of RAM and is intended for use with the Freescale fully compliant 802.15.4 MAC. Custom networks based on the 802.15.4 Standard MAC can be implemented to fit user needs. The 802.15.4 Standard supports star, mesh and cluster tree topologies as well as beaconed networks.
- The MC13213 contains 60K of flash and 4KB of RAM and is also intended for use with the Freescale fully compliant 802.15.4 MAC where larger memory is required. In addition, this device can support ZigBee 2006 applications that use Freescale's BeeStack.

Applications include, but are not limited to, the following:

- Residential and commercial automation
  - Lighting control
  - Security
  - Access control
  - Heating, ventilation, air-conditioning (HVAC)
  - Automated meter reading (AMR)
- Industrial Control
  - Asset tracking and monitoring
  - Homeland security
  - Process management
  - Environmental monitoring and control
  - HVAC
  - Automated meter reading
- Health Care
  - Patient monitoring
  - Fitness monitoring
- Consumer
  - Human interface devices (keyboard, mice, etc.)
  - Remote control
  - Wireless toys

1.1 Ordering Information

Table 1 provides additional details about the MC1321x family.

Table 1. Orderable Parts Details

Device	Operating Temp Range (TA.)	Package	Memory Options	Description
MC13211	-40° to 85° C	LGA	1KB RAM, 16KB Flash	Intended for proprietary applications and Freescale Simple MAC (SMAC)
MC13211R2	-40° to 85° C	LGA Tape and Reel	1KB RAM, 16KB Flash	Intended for proprietary applications and Freescale Simple MAC (SMAC)
MC13212	-40° to 85° C	LGA	2KB RAM, 32KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC
MC13212R2	-40° to 85° C	LGA Tape and Reel	2KB RAM, 32KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC
MC13213	-40° to 85° C	LGA	4KB RAM, 60KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC. In addition, this device can support ZigBee 2006 applications that use Freescale's BeeStack.
MC13213R2	-40° to 85° C	LGA Tape and Reel	4KB RAM, 60KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC. In addition, this device can support ZigBee 2006 applications that use Freescale's BeeStack.

1.2 General Platform Features

- 802.15.4 Standard compliant on-chip transceiver/modem
  - 2.4GHz
  - 16 selectable channels
  - Programmable output power
- Multiple power saving modes
- 2V to 3.4V operating voltage with on-chip voltage regulators
- -40°C to +85°C temperature range
- Low external component count
- Supports single 16 MHz crystal clock source operation or dual crystal operation
- Support for SMAC, 802.15.4 Standard, and ZigBee software
- 9mm x 9mm x 1mm 71-pin LGA

1.3 Microcontroller Features

- Low voltage MCU with 40 MHz low power HCS08 CPU core
- Up to 60K flash memory with block protection and security and 4K RAM
  - MC13211: 16KB Flash, 1KB RAM
  - MC13212: 32KB Flash, 2KB RAM
  - MC13213: 60KB Flash, 4KB RAM
- Low power modes (Wait plus Stop2 and Stop3 modes)
- Dedicated serial peripheral interface (SPI) connected internally to 802.15.4 modem
- One 4-channel and one 1-channel 16-bit timer/pulse width modulator (TPM) module with selectable input capture, output capture, and PWM capability.
- 8-bit port keyboard interrupt (KBI)
- 8-channel 8-10-bit ADC
- Two independent serial communication interfaces (SCI)
- Multiple clock source options
  - Internal clock generator (ICG) with 243 kHz oscillator that has +/-0.2% trimming resolution and +/-0.5% deviation across voltage.
  - Startup oscillator of approximately 8 MHz
  - External crystal or resonator
  - External source from modem clock for very high accuracy source or system low-cost option
- Inter-integrated circuit (IIC) interface.
- In-circuit debug and flash programming available via on-chip background debug module (BDM)
  - Two comparator and 9 trigger modes
  - Eight deep FIFO for storing change-of-flow addresses and event-only data
  - Tag and force breakpoints
  - In-circuit debugging with single breakpoint
- System protection features
  - Programmable low voltage interrupt (LVI)
  - Optional watchdog timer (COP)
  - Illegal opcode detection
- Up to 32 MCU GPIO with programmable pullups

1.4 RF Modem Features

- Fully compliant 802.15.4 Standard transceiver supports 250 kbps O-QPSK data in 5.0 MHz channels and full spread-spectrum encode and decode
- Operates on one of 16 selectable channels in the 2.4 GHz ISM band
- -1 dBm to 0 dBm nominal output power, programmable from -27 dBm to +3 dBm typical
- Receive sensitivity of <-92 dBm (typical) at 1% PER, 20-byte packet, much better than the 802.15.4 Standard of -85 dBm
- Integrated transmit/receive switch
- Dual PA ouput pairs which can be programmed for full differential single-port or dual-port operation that supports an external LNA and/or PA.
- Three low power modes for increased battery life
- Programmable frequency clock output for use by MCU
- Onboard trim capability for 16 MHz crystal reference oscillator eliminates need for external variable capacitors and allows for automated production frequency calibration
- Four internal timer comparators available to supplement MCU timer resources
- Supports both packet data mode and streaming data mode
- Seven GPIO to supplement MCU GPIO

1.5 Software Features

Freescale provides a wide range of software functionality to complement the MC1321x hardware. There are three levels of application solutions:

1. Simple proprietary wireless connectivity.
2. User networks built on the 802.15.4 MAC standard.
3. ZigBee 2006 compliant, Freescale BeeStack.

1.5.1 Simple MAC (SMAC)

- Small memory footprint (about 3 Kbytes typical)
- Supports point-to-point and star network configurations
- Proprietary networks
- Source code and application examples provided

1.5.2 802.15.4 Standard-Compliant MAC

- Supports star, mesh and cluster tree topologies
- Supports beaconed networks
- Supports GTS for low latency
- Multiple power saving modes (idle doze, hibernate)

1.5.3 ZigBee 2006-Compliant. Freescale BeeStack

- Supports ZigBee 2006 specification
- Supports star, mesh and tree networks
- Advanced Encryption Standard (AES) 128-bit security

1.6 System Block Diagram

Figure 1 shows a simplified block diagram of the MC1321x solution.

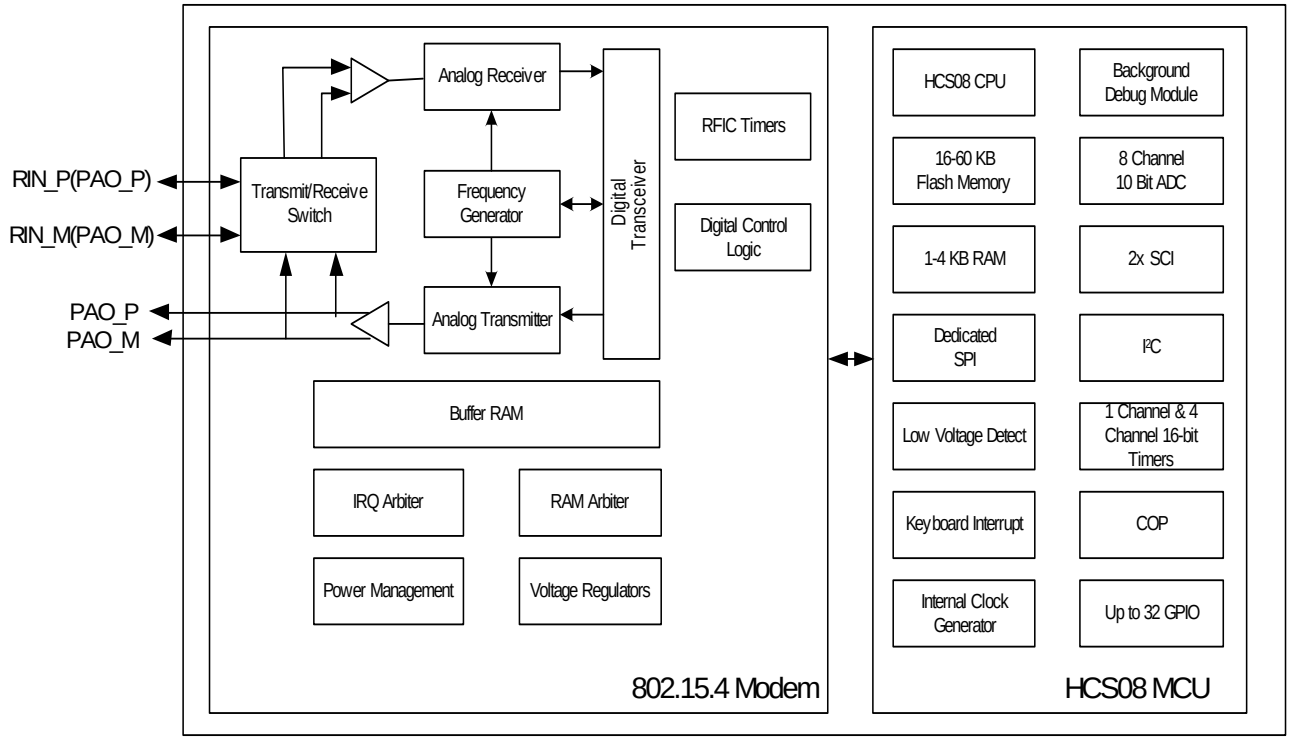


Figure 1. MC1321x System Level Block Diagram

1.7 System Clock Configuration

The MC321x device allows for a wide array of system clock configurations:

- Pins are provided for a separate external clock source for the CPU. The external clock source can by derived from a crystal oscillator or from an external clock source
- Pins are provided for a 16 MHz crystal for the modem clock source (required)
- The modem crystal oscillator frequency can be trimmed through programming to maintain the tight tolerances required by the 802.15.4 Standard
- The modem provides a CLKO programmable frequency clock output that can be used as an external source to the CPU. As a result, a single crystal system clock solution is possible
- Out of reset, the MCU uses an internally generated clock (approximately 8-MHz) for start-up. This allows recovery from stop or reset without a long crystal start-up delay
- The MCU contains an internal clock generator (which can be trimmed) that can be used to run the MCU for low power operation. This internal reference is approximately 243 kHz

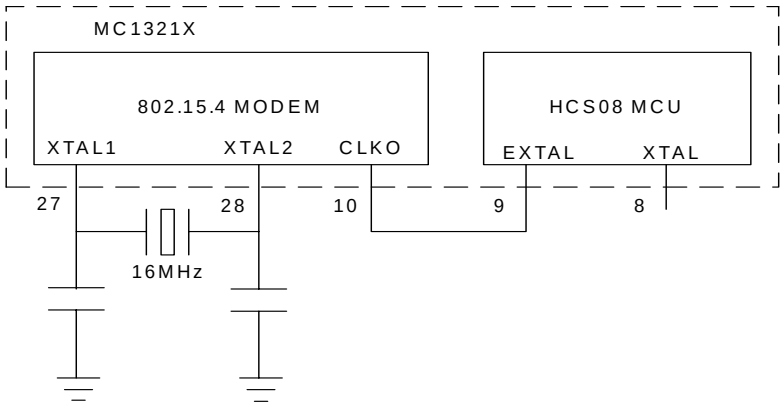


Figure 2. MC1321x Single Crystal System Clock Structure

2 MC1321x Pin Assignment and Connections

Figure 3 shows the MC1321x pinout.

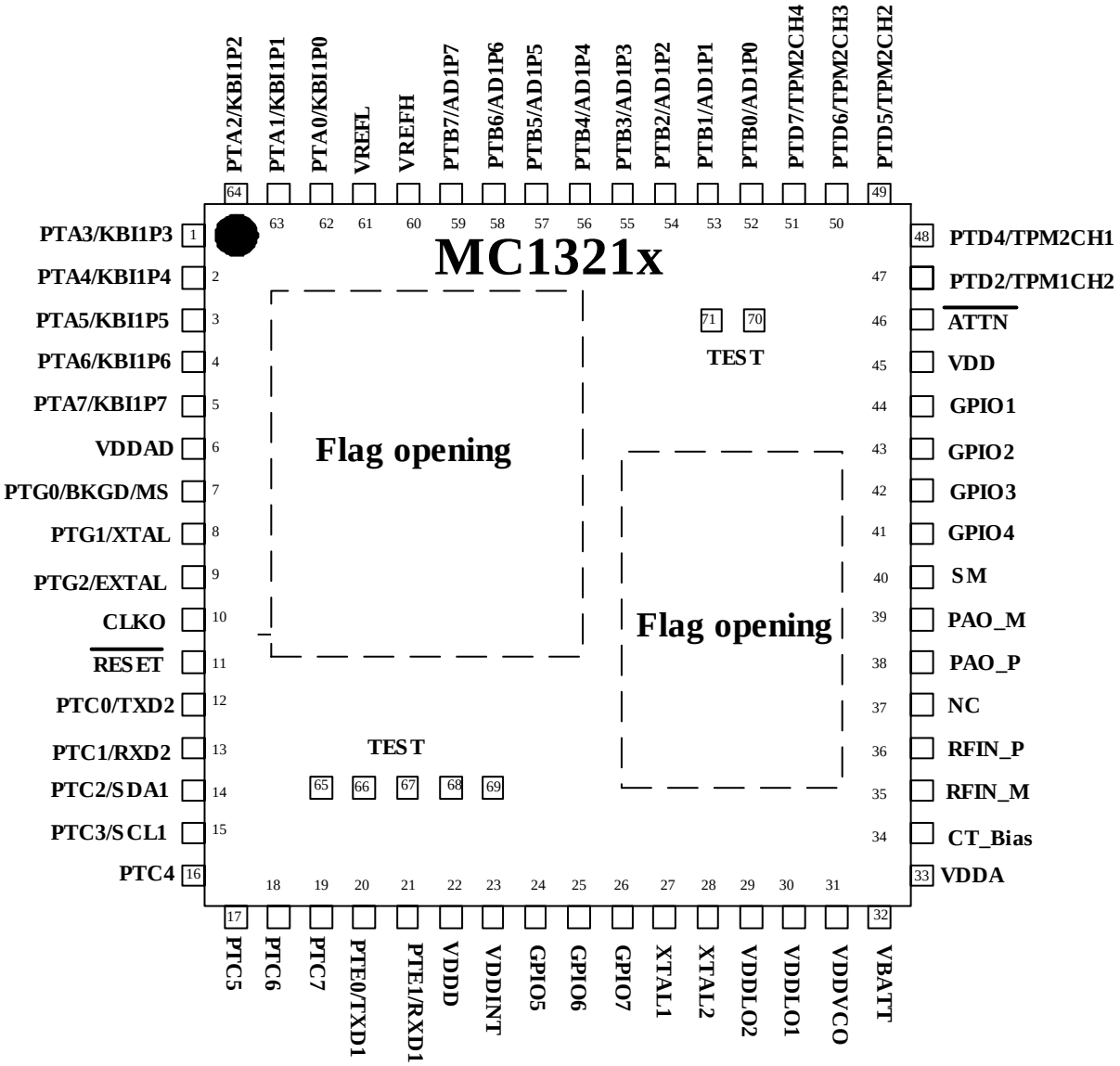


Figure 3. MC1321x Pinout (Top View)

2.1 Pin Definitions

Table 2 details the MC1321x pinout and functionality.

Table 2. Pin Function Description

Pin #	Pin Name	Type	Description	Functionality
1	PTA3/KBI1P3	Digital Input/Output	MCU Port A Bit 3 / Keyboard Input Bit 3	
2	PTA4/KBI1P4	Digital Input/Output	MCU Port A Bit 4 / Keyboard Input Bit 4	
3	PTA5/KBI1P5	Digital Input/Output	MCU Port A Bit 5 / Keyboard Input Bit 5	
4	PTA6/KBI1P6	Digital Input/Output	MCU Port A Bit 6 / Keyboard Input Bit 6	
5	PTA7/KBI1P7	Digital Input/Output	MCU Port A Bit 7 / Keyboard Input Bit 7	
6	VDDAD	Power Input	MCU power supply to ATD	Decouple to ground.
7	PTG0/BKGND/MS	Digital Input/Output	MCU Port G Bit 0 / Background / Mode Select	PTG0 is output only. Pin is I/O when used as BDM function.
8	PTG1/XTAL	Digital Input/Output/ Output	MCU Port G Bit 1 / Crystal oscillator output	Full I/O when not used as clock source.
9	PTG2/EXTAL	Digital Input/Output/ Input	MCU Port G Bit 2 / Crystal oscillator input	Full I/O when not used as clock source.
10	CLKO	Digital Output	Modem Clock Output	Programmable frequencies of: 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 62.5 kHz, 32.786+ kHz (default), and 16.393+ kHz.
11	$\overline{\text{RESET}}$	Digital Input/Output	MCU reset. Active low	
12	PTC0/TXD2	Digital Input/Output	MCU Port C Bit 0 / SCI2 TX data out	
13	PTC1/RXD2	Digital Input/Output	MCU Port C Bit 1/ SCI2 RX data in	
14	PTC2/SDA1	Digital Input/Output	MCU Port C Bit 1/ IIC bus data	
15	PTC3/SCL1	Digital Input/Output	MCU Port C Bit 1/ IIC bus clock	
16	PTC4	Digital Input/Output	MCU Port C Bit 4	
17	PTC5	Digital Input/Output	MCU Port C Bit 5	

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
18	PTC6	Digital Input/Output	MCU Port C Bit 6	
19	PTC7	Digital Input/Output	MCU Port C Bit 7	
20	PTE0/TXD1	Digital Input/Output	MCU Port E Bit 0 / SCI1 TX data out	
21	PTE1/RXD1	Digital Input/Output	MCU Port E Bit 1/ SCI1 RX data in	
22	VDDD	Power Output	Modem regulated output supply voltage	Decouple to ground.
23	VDDINT	Power Input	Modem digital interface supply	2.0 to 3.4 V. Decouple to ground. Connect to Battery.
24	GPIO5[1]	Digital Input/Output	General Purpose Input/Output 5.	See Footnote 1
25	GPIO6	Digital Input/Output	Modem General Purpose Input/Output 6	
26	GPIO7	Digital Input/Output	Modem General Purpose Input/Output 7	
27	XTAL1	Input	Modem crystal reference oscillator input	Connect to 16 MHz crystal and load capacitor.
28	XTAL2	Input/Output	Modem crystal reference oscillator output	Connect to 16 MHz crystal and load capacitor. Do not load this pin by using it as a 16 MHz source. Measure 16 MHz output at CLKO, programmed for 16 MHz.
29	VDDLO2	Power Input	Modem LO2 VDD supply	Connect to VDDA externally.
30	VDDLO1	Power Input	Modem LO1 VDD supply	Connect to VDDA externally.
31	VDDVCO	Power Output	Modem VCO regulated supply bypass	Decouple to ground.
32	VBATT	Power Input	Modem voltage regulators' input	Decouple to ground. Connect to Battery.
33	VDDA	Power Output	Modem analog regulated supply output	Decouple to ground. Connect to directly VDDLO1 and VDDLO2 externally and to PAO_P and PAO_M through a bias network.
34	CT_Bias	RF Control Output	Modem bias voltage/control signal for RF external components	When used with internal T/R switch, provides ground reference for RX and VDDA reference for TX. Can also be used as a control signal with external LNA, antenna switch, and/or PA.
35	RFIN_M	RF Input (Output)	Modem RF input/output negative	When used with internal T/R switch, this is a bi-directional RF port for the internal LNA and PA
36	RFIN_P	RF Input (Output)	Modem RF input/output positive	When used with internal T/R switch, this is a bi-directional RF port for the internal LNA and PA

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
37	NC		Not used	May be grounded or left open
38	PAO_P	RF Output	Modem power amplifier RF output positive	Open drain. Connect to VDDA through a bias network when used with external balun. Not used when internal T/R switch is used.
39	PAO_M	RF Output	Modem power amplifier RF output negative	Open drain. Connect to VDDA through a bias network when used with external balun. Not used when internal T/R switch is used.
40	SM	Input	Test Mode pin	Must be grounded for normal operation
41	GPIO4[1]	Digital Input/ Output	General Purpose Input/Output 4.	See Footnote 1
42	GPIO3	Digital Input/Output	Modem General Purpose Input/Output 3	
43	GPIO2	Test Point	MCU Port E Bit 6 / Modem General Purpose Input/Output 2	Internally connected pins. When gpio_alt_en, Register 9, Bit 7 = 1, GPIO2 functions as a “CRC Valid” indicator.
44	GPIO1	Test Point	MCU Port E Bit 7 / Modem General Purpose Input/Output 1	Internally connected pins. When gpio_alt_en, Register 9, Bit 7 = 1, GPIO1 functions as an “Out of Idle” indicator.
45	VDD	Power Input	MCU main power supply	Decouple to ground.
46	$\overline{\text{ATTN}}$[2]	Digital Input	Active Low Attention. Transitions IC from either Hibernate or Doze Modes to Idle.	See Footnote 2
47	PTD2/TPM1CH2	Digital Input/Output	MCU Port D Bit 2 / TPM1 Channel 2	
48	PTD4/TPM2CH1	Digital Input/Output	MCU Port D Bit 4 / TPM2 Channel 1	
49	PTD5/TPM2CH2	Digital Input/Output	MCU Port D Bit 5 / TPM2 Channel 2	
50	PTD6/TPM2CH3	Digital Input/Output	MCU Port D Bit 6 / TPM2 Channel 3	
51	PTD7/TPM2CH4	Digital Input/Output	MCU Port D Bit 7 / TPM2 Channel 4	
52	PTB0/AD1P0	Input/Output	MCU Port B Bit 0 / ATD analogChannel 0	
53	PTB1/AD1P1	Input/Output	MCU Port B Bit 1 / ATD analog Channel 1	
54	PTB2/AD1P2	Input/Output	MCU Port B Bit 2 / ATD analog Channel 2	
55	PTB3/AD1P3	Input/Output	MCU Port B Bit 3 / ATD analog Channel 3	

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
56	PTB4/AD1P4	Input/Output	MCU Port B Bit 4 / ATD analog Channel 4	
57	PTB5/AD1P5	Input/Output	MCU Port B Bit 5 / ATD analog Channel 5	
58	PTB6/AD1P6	Input/Output	MCU Port B Bit 6 / ATD analog Channel 6	
59	PTB7/AD1P7	Input/Output	MCU Port B Bit 7 / ATD analog Channel 7	
60	VREFH	Input	MCU high reference voltage for ATD	
61	VREFL	Input	MCU low reference voltage for ATD	
62	PTA0/KBI1P0	Digital Input/Output	MCU Port A Bit 0 / Keyboard Input Bit 0	
63	PTA1/KBI1P1	Digital Input/Output	MCU Port A Bit 1 / Keyboard Input Bit 1	
64	PTA2/KBI1P2	Digital Input/Output	MCU Port A Bit 2 / Keyboard Input Bit 2	
65	TEST	Test Point	For factory test	Do not connect
66	TEST	Test Point	For factory test	Do not connect
67	TEST	Test Point	For factory test	Do not connect
68	TEST	Test Point	For factory test	Do not connect
69	TEST	Test Point	For factory test	Do not connect
70	TEST	Test Point	For factory test	Do not connect
71	TEST	Test Point	For factory test	Do not connect
FLAG	VSS	Power input	External package flag. Common VSS	Connect to ground.

[1] The transceiver GPIO pins default to inputs at reset. There are no programmable pullups on these pins. Unused GPIO pins should be tied to ground if left as inputs, or if left unconnected, they should be programmed as outputs set to the low state.

[2] During low power modes, input must remain driven by MCU.

2.2 Internal Functional Interconnects

The MCU provides control for the 802.15.4 modem. The required interconnects between the devices are routed onboard the SiP. In addition, the signals are brought out to external pads primarily for use as test points. These signals can be useful when writing and debugging software.

Table 3. Internal Functional Interconnects

Pin #	MCU Signal	Modem Signal	Description
43	PTE6	GPIO2	Modem GPIO2 output acts as “CRC Valid” status indicator for Stream Data Mode to MCU.
44	PTE7	GPIO1	Modem GPIO1 output acts as “Out of Idle” status indicator for Stream Data Mode to MCU.
46	PTD0	$\overline{\text{ATTN}}$	MCU Port D Bit 0 drives the attention ($\overline{\text{ATTN}}$) input of the modem to wake modem from Hibernate or Doze Mode.
	PTE5/SPSCK1	SPICLK[1]	MCU SPI master SPI clock output drives modem SPICLK slave clock input.
	PTE4/MOSI1	MOSI[1]	MCU SPI master MOSI output drives modem slave MOSI input
	PTE3/MISO1	MISO[2]	Modem SPI slave MISO output drives MCU master MISO input
	PTE2/$\overline{\text{SS1}}$	$\overline{\text{CE}}$[1]	MCU SPI master SS output drives modem slave $\overline{\text{CE}}$ input
	IRQ	$\overline{\text{M\_IRQ}}$	Modem interrupt request $\overline{\text{M\_IRQ}}$ output drives MCU IRQ input
	PTD1	RXTXEN[1]	MCU Port D Bit 1 drives the RXTXEN input to the modem to enable TX or RX or CCA operations.
	PTD3	$\overline{\text{M\_RST}}$	MCU Port D Bit 3 drives the reset $\overline{\text{M\_RST}}$ input to the modem.

1 During low power modes, input must remain driven by MCU.

2 By default MISO is tri-stated when $\overline{\text{CE}}$ is negated. For low power operation, miso_hiz_en (Bit 11, Register 07) should be set to zero so that MISO is driven low when $\overline{\text{CE}}$ is negated.

NOTE

To use the MCU and modem signals as described in Table 3, the MCU needs to be programmed appropriately for the stated function.

3 MC1321x Serial Peripheral Interface (SPI)

The MC1321x modem and CPU communicate primarily through the onboard SPI command channel. Figure 4 shows the SiP internal interconnects with the SPI bus highlighted. The MCU has a single SPI module that is dedicated to the modem SPI interface. The modem is a slave only and the MCU SPI must be programmed and used as a master only. Further, the SPI performance is limited by the modem constraints of 8 MHz SPI clock frequency, and use of the SPI must be programmed to meet the modem SPI protocol.

3.1 SiP Level SPI Pin Connections

The SiP level SPI pin connections are all internal to the device. Figure 4 shows the SiP interconnections with the SPI bus highlighted.

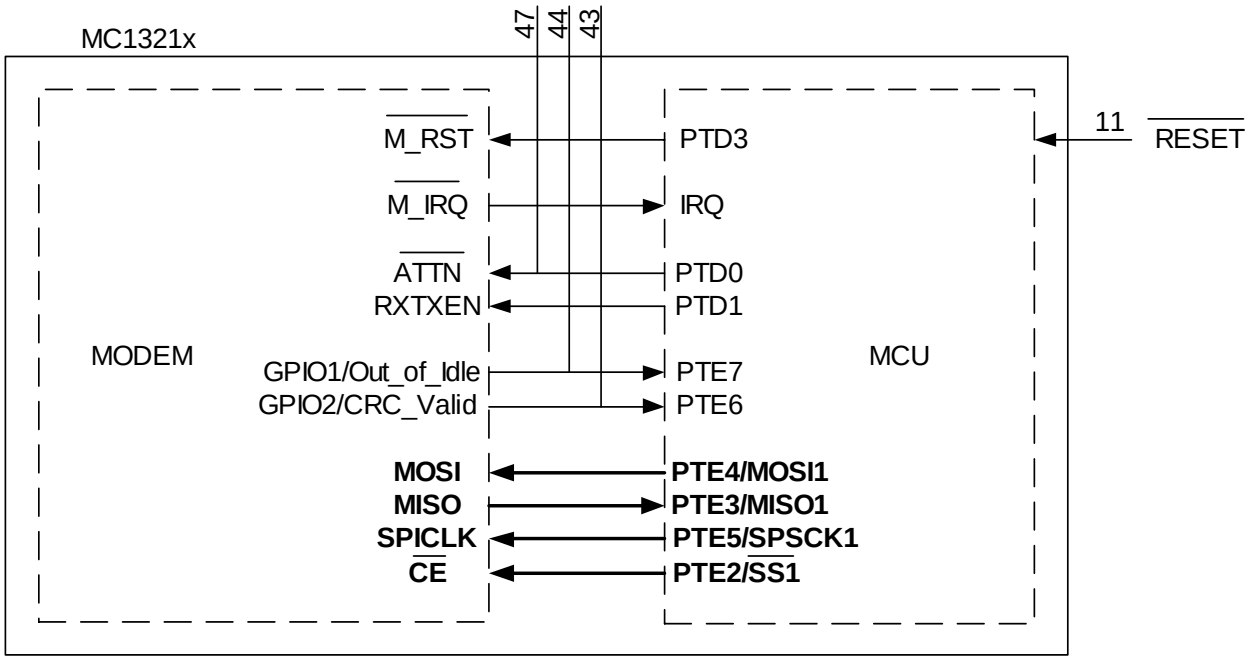


Figure 4. MC1321x Internal Interconnects Highlighting SPI Bus

Table 4. MC1321x Internal SPI Connections

MCU Signal	Modem Signal	Description
PTE5/SPSCK1	SPICLK	MCU SPI master SPI clock output drives modem SPICLK slave clock input.
PTE4/MOSI1	MOSI	MCU SPI master MOSI output drives modem slave MOSI input
PTE3/MISO1	MISO	Modem SPI slave MISO output drives MCU master MISO input
PTE2/$\overline{SS1}$	$\overline{CE}$	MCU SPI master SS output drives modem slave $\overline{CE}$ input

3.2 SPI Features

- MCU bus master
- Modem bus slave
- Programmable SPI clock rate; maximum rate is 8 MHz
- Double-buffered transmit and receive at MCU
- Serial clock phase and polarity must meet modem requirements (MCU control bits
- Slave select programmed to meet modem protocol

3.3 SPI System Block Diagram

Figure 5 shows the SPI system level diagram.

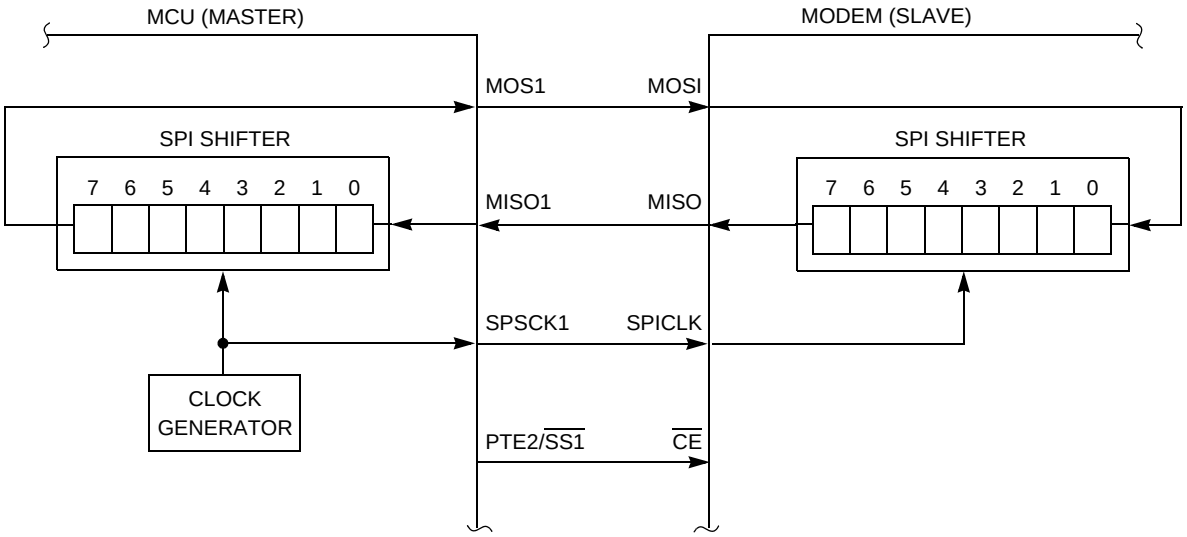


Figure 5. SPI System Block Diagram

Figure 5 shows the SPI modules of the MCU and modem in the master-slave arrangement. The MCU (master) initiates all SPI transfers. During a transfer, the master shifts data out (on the MOSI pin) to the slave while simultaneously shifting data in (on the MISO pin) from the slave. Although the SPI interface supports simultaneous data exchange between master and slave, the modem SPI protocol only uses data exchange in one direction at a time. The SPSCK signal is a clock output from the master and an input to the slave. The slave device must be selected by a low level on the slave select input ($\overline{SS1}$ pin).

4 802.15.4 Standard Modem

4.1 Block Diagram

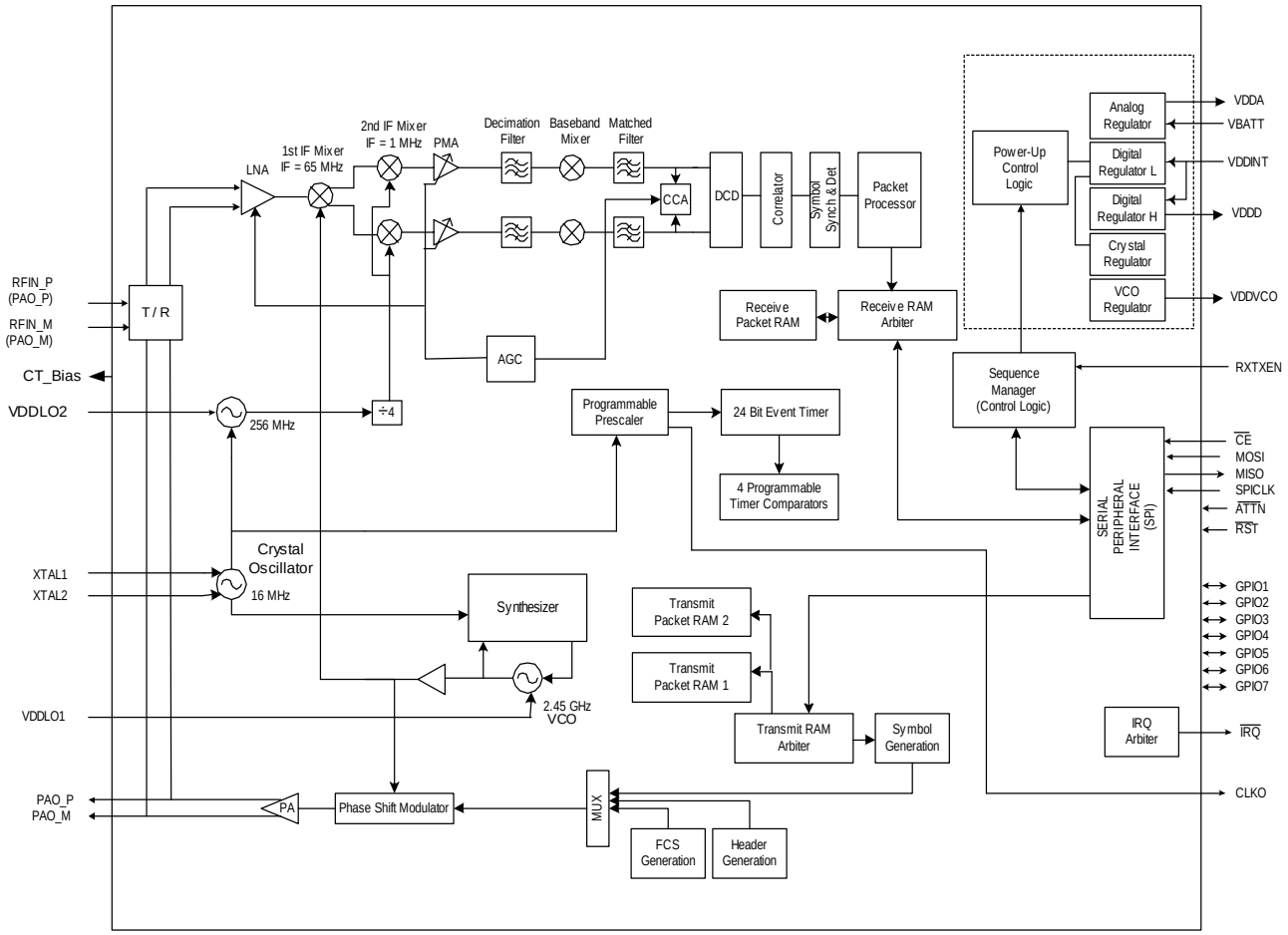


Figure 6. 802.15.4 Standard Modem Block Diagram

4.2 Data Transfer Modes

The 802.15.4 modem has two data transfer modes:

1. Packet Mode — Data is buffered in on-chip RAM
2. Streaming Mode — Data is processed word-by-word

The Freescale 802.15.4 MAC software only supports the streaming mode of data transfer. For proprietary applications, packet mode can be used to conserve MCU resources.

4.3 Packet Structure

Figure 7 shows the packet structure of the 802.15.4 modem. Payloads of up to 125 bytes are supported. The 802.15.4 modem adds a four-byte preamble, a one-byte Start of Frame Delimiter (SFD), and a one-byte Frame Length Indicator (FLI) before the data. A Frame Check Sequence (FCS) is calculated and appended to the end of the data.

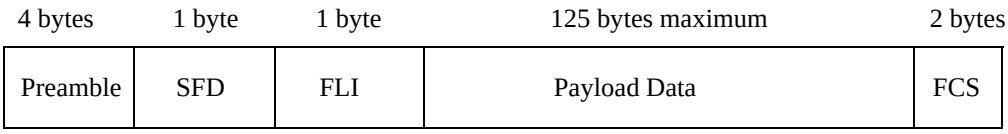


Figure 7. 802.15.4 modem Packet Structure

4.4 Receive Path Description

In the receive signal path, the RF input is converted to low IF In-phase and Quadrature (I & Q) signals through two down-conversion stages. A Clear Channel Assessment (CCA) can be performed based upon the baseband energy integrated over a specific time interval. The digital back end performs Differential Chip Detection (DCD), the correlator “de-spreads” the Direct Sequence Spread Spectrum (DSSS) Offset QPSK (O-QPSK) signal, determines the symbols and packets, and detects the data.

The preamble, SFD, and FLI are parsed and used to detect the payload data and FCS (which are stored in RAM in Packet Mode). A two-byte FCS is calculated on the received data and compared to the FCS value appended to the transmitted data, which generates a Cyclical Redundancy Check (CRC) result. A parameter of received energy during the reception called the Link Quality Indicator is measured over a 64 µs period after the packet preamble and stored in an SPI register.

If the 802.15.4 modem is in Packet Mode, the data is stored in RAM and processed as an entire packet. The MCU is notified that an entire packet has been received via an interrupt.

If the 802.15.4 modem is in streaming mode, the MCU is notified by a recurring interrupt on a word-by-word basis.

Figure 8 shows CCA reported power level versus input power. Note that CCA reported power saturates at about -57 dBm input power which is well above 802.15.4 Standard requirements. Figure 9 shows energy detection/LQI reported level versus input power.

NOTE

For both graphs, the required 802.15.4 Standard accuracy and range limits are shown. A 3.5 dBm offset has been programmed into the CCA reporting level to center the level over temperature in the graphs.

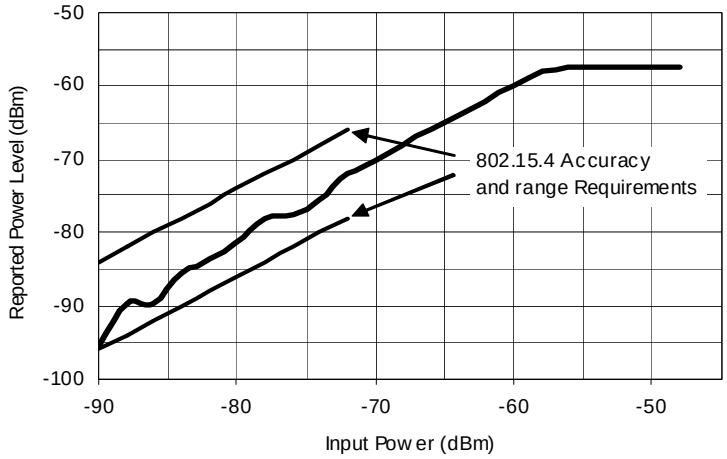


Figure 8. Reported Power Level versus Input Power in Clear Channel Assessment Mode

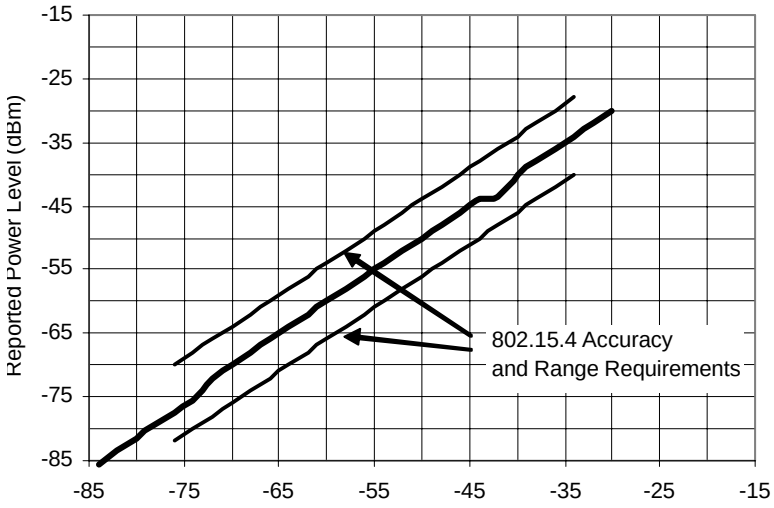


Figure 9. Reported Power Level Versus Input Power for Energy Detect or Link Quality Indicator

4.5 Transmit Path Description

For the transmit path, the TX data that was previously written to the internal RAM is retrieved (packet mode) or the TX data is clocked in via the SPI (stream mode), formed into packets per the 802.15.4 PHY, spread, and then up-converted to the transmit frequency.

If the 802.15.4 modem is in packet mode, data is processed as an entire packet. The data is first loaded into the TX buffer. The MCU then requests that the modem transmit the data. The MCU is notified via an interrupt when the whole packet has successfully been transmitted.

In streaming mode, the data is fed to the 802.15.4 modem on a word-by-word basis with an interrupt serving as a notification that the 802.15.4 modem is ready for more data. This continues until the whole packet is transmitted.

In both modes, a two-byte FCS is calculated in hardware from the payload data and appended to the packet. This done without intervention from the user.

4.6 Functional Description

The following sections provide a detailed description of the MC1321x functionality including the operating modes and the Serial Peripheral Interface (SPI).

4.6.1 802.15.4 Modem Operational Modes

The 802.15.4 modem has a number of operational modes that allow for low-current operation. Transition from the Off to Idle mode occurs when $\overline{\text{M\_RST}}$ is negated. Once in Idle, the SPI is active and is used to control the IC. Transition to Hibernate and Doze modes is enabled via the SPI. These modes are summarized, along with the transition times, in Table 5. Current drain in the various modes is listed in Table 8, DC Electrical Characteristics.

Table 5. 802.15.4 Modem Mode Definitions and Transition Times

Mode	Definition	Transition Time To or From Idle
Off	All IC functions Off, Leakage only. $\overline{\text{M\_RST}}$ asserted. Digital outputs are tri-stated including $\overline{\text{IRQ}}$	10 - 25 ms to Idle
Hibernate	Crystal Reference Oscillator Off. (SPI not functional.) IC Responds to $\overline{\text{ATTN}}$. Data is retained.	7 - 20 ms to Idle
Doze	Crystal Reference Oscillator On but CLKO output available only if Register 7, Bit 9 = 1 for frequencies of 1 MHz or less. (SPI not functional.) Responds to $\overline{\text{ATTN}}$ and can be programmed to enter Idle Mode through an internal timer comparator.	(300 + 1/CLKO) µs to Idle
Idle	Crystal Reference Oscillator On with CLKO output available. SPI active.	
Receive	Crystal Reference Oscillator On. Receiver On.	144 µs from Idle
Transmit	Crystal Reference Oscillator On. Transmitter On.	144 µs from Idle

4.6.2 Serial Peripheral Interface (SPI)

The MCU directs the 802.15.4 modem, checks its status, and reads/writes data to the device through the 4-wire SPI port. The transceiver operates as a SPI slave device only. A transaction between the host and the 802.15.4 modem occurs as multiple 8-bit bursts on the SPI. The modem SPI signals are:

1. Chip Enable ($\overline{CE}$) - A transaction on the SPI port is framed by the active low $\overline{CE}$ input signal. A transaction is a minimum of 3 SPI bursts and can extend to a greater number of bursts.
2. SPI Clock (SPICLK) - The host drives the SPICLK input to the 802.15.4 modem. Data is clocked into the master or slave on the leading (rising) edge of the return-to-zero SPICLK and data out changes state on the trailing (falling) edge of SPICLK.

NOTE

For the MCU, the SPI clock format is the clock phase control bit CPHA = 0 and the clock polarity control bit CPOL = 0.

3. Master Out/Slave In (MOSI) - Incoming data from the host is presented on the MOSI input.
4. Master In/Slave Out (MISO) - The 802.15.4 modem presents data to the master on the MISO output.

Although the SPI port is fully static, internal memory, timer and interrupt arbiters require an internal clock (CLK_{core}), derived from the crystal reference oscillator, to communicate from the SPI registers to internal registers and memory.

4.6.2.1 SPI Burst Operation

The SPI port of the MCU transfers data in bursts of 8 bits with most significant bit (MSB) first. The master (MCU) can send a byte to the slave (transceiver) on the MOSI line and the slave can send a byte to the master on the MISO line. Although an 802.15.4 modem transaction is three or more SPI bursts long, the timing of a single SPI burst is shown in Figure 10. The maximum SPI clock rate is 8 Mhz from the MCU because the modem is limited by this number.

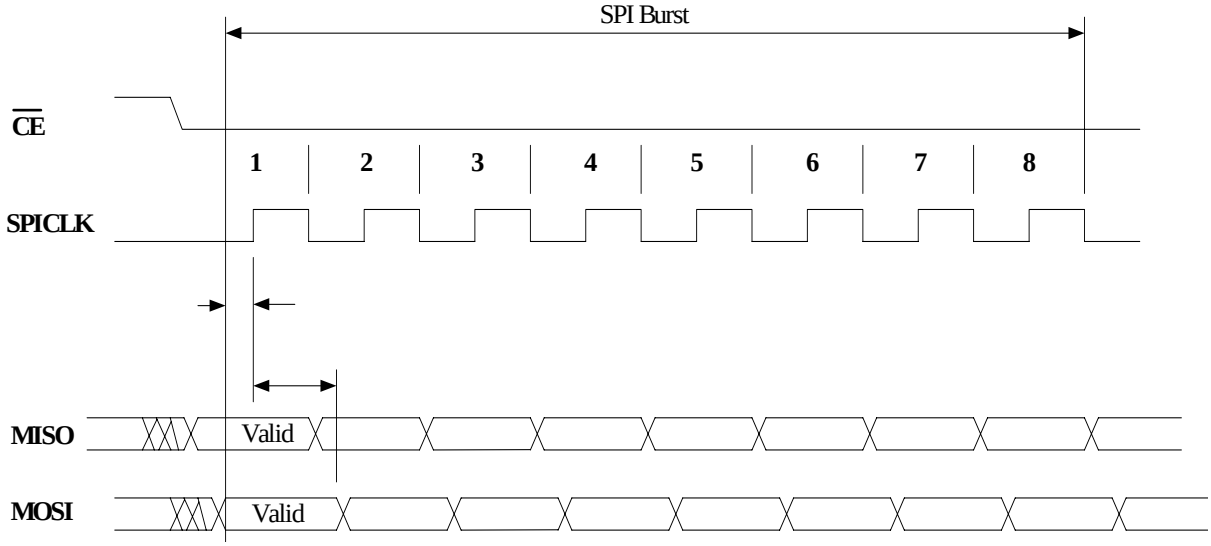


Figure 10. SPI Single Burst Timing Diagram

4.6.2.2 SPI Transaction Operation

Although the SPI port of the MCU transfers data in bursts of 8 bits, the 802.15.4 modem requires that a complete SPI transaction be framed by $\overline{CE}$, and there will be three (3) or more bursts per transaction. The assertion of $\overline{CE}$ to low signals the start of a transaction. The first SPI burst is a write of an 8-bit header to the transceiver (MOSI is valid) that defines a 6-bit address of the internal resource being accessed and identifies the access as being a read or write operation. In this context, a write is data written to the 802.15.4 modem and a read is data written to the SPI master. The following SPI bursts will be either the write data (MOSI is valid) to the transceiver or read data from the transceiver (MISO is valid).

Although the SPI bus is capable of sending data simultaneously between master and slave, the 802.15.4 modem never uses this mode. The number of data bytes (payload) will be a minimum of 2 bytes and can extend to a larger number depending on the type of access. After the final SPI burst, $\overline{CE}$ is negated to high to signal the end of the transaction.

An example SPI read transaction with a 2-byte payload is shown in Figure 11.

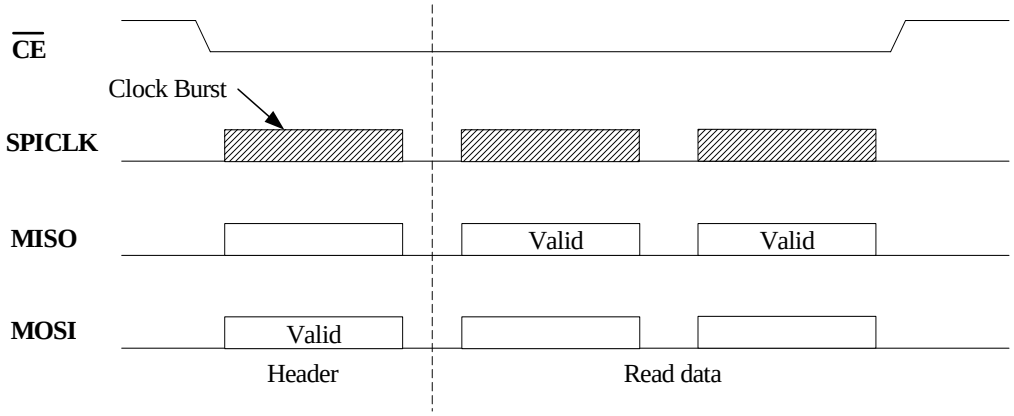


Figure 11. SPI Read Transaction Diagram

4.7 Modem Crystal Oscillator

The modem crystal oscillator uses the following external pins as shown in Figure 12.

1. XTAL1 - reference oscillator input.
2. XTAL2 - reference oscillator output. Note that this pin should not be loaded as a reference source or to measure frequency; instead use CLKO to measure or supply 16 MHz.

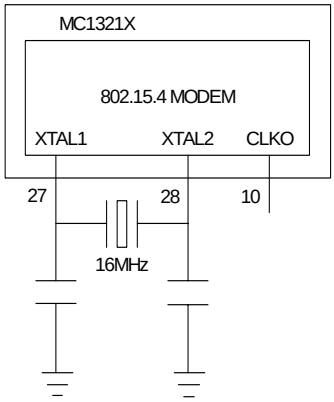


Figure 12. Modem Crystal Oscillator

The 802.15.4 Standard requires that several frequency tolerances be kept within ± 40 ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will still result in acceptable performance. The primary determining factor in meeting the 802.15.4 Standard is the tolerance of the crystal oscillator reference frequency. A number of factors can contribute to this tolerance and a crystal specification will quantify each of them:

1. The initial (or make) tolerance of the crystal resonant frequency itself.
2. The variation of the crystal resonant frequency with temperature.
3. The variation of the crystal resonant frequency with time, also commonly known as aging.
4. The variation of the crystal resonant frequency with load capacitance, also commonly known as pulling. This is affected by:
   a) The external load capacitor values - initial tolerance and variation with temperature
   b) The internal trim capacitor values - initial tolerance and variation with temperature
   c) Stray capacitance on the crystal pin nodes - including stray on-chip capacitance, stray package capacitance and stray board capacitance; and its initial tolerance and variation with temperature

Freescale has specified that a 16 MHz crystal with a <9 pF load capacitance is required. The 802.15.4 modem does not contain a reference divider, so 16 MHz is the only frequency that can be used. A crystal requiring higher load capacitance is prohibited because a higher load on the amplifier circuit may compromise its performance. The crystal manufacturer defines the load capacitance as that total external capacitance seen across the two terminals of the crystal. The oscillator amplifier configuration used in the 802.15.4 modem requires two balanced load capacitors from each terminal of the crystal to ground. As such, the capacitors are seen to be in series by the crystal, so each must be <18 pF for proper loading.

The modem uses the 16 MHz crystal oscillator as the reference oscillator for the system and a programmable warp capability is provided. It is controlled by programming CLKO_Ctl Register 0A, Bits

15-8 (xtal_trim[7:0]). The trimming procedure varies the frequency by a few hertz per step, depending on the type of crystal. The high end of the frequency spectrum is set when xtal_trim[7:0] is set to zero. As xtal_trim[7:0] is increased, the frequency is decreased. Accuracy of this feature can be observed by varying xtal_trim[7:0] and using a spectrum analyzer or frequency counter to track the change in frequency of the crystal signal. The reference oscillator frequency can be measured at the CLKO contact by programming CLKO_Ctl Register 0A, Bits 2-0, to value 000.

Figure 13 shows typical oscillator frequency decrease versus the value programmed in xtal_trim[7:0].

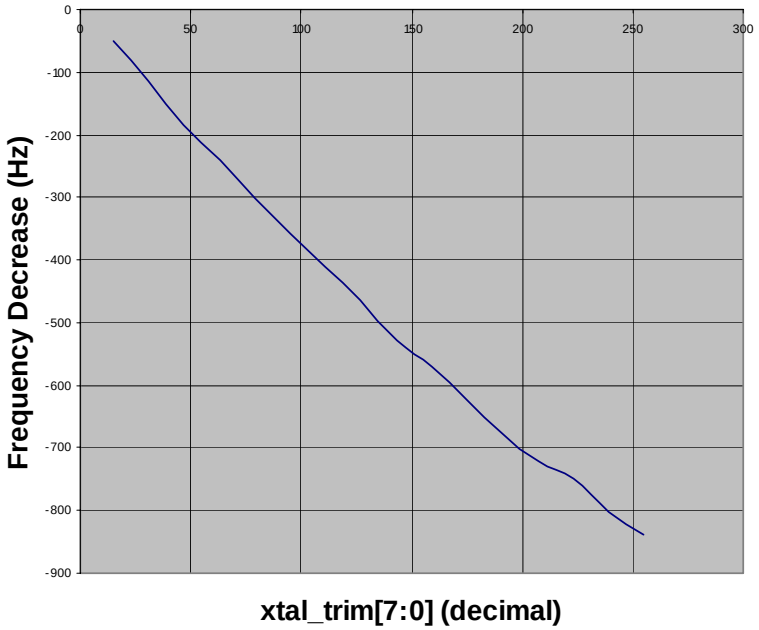


Figure 13. Crystal Frequency Variation vs. xtal_trim[7:0]

4.8 Radio Usage

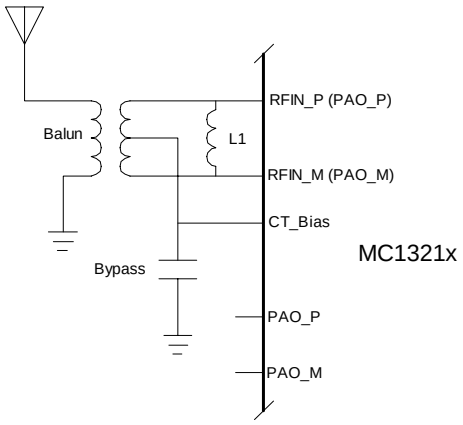
The MC1321x RF analog interface has been designed to provide maximum flexibility as well as low external part count and cost. An on-chip transmit/receive (T/R) switch with bias switch (CT_Bias) can be used for a simple single antenna interface with a balun. Alternately, separate full differential RFIN and PAO outputs can be utilized for separate RX and TX antennae or external LNA and PA designs.

Figure 14 shows three possible configurations for the transceiver radio RF usage.

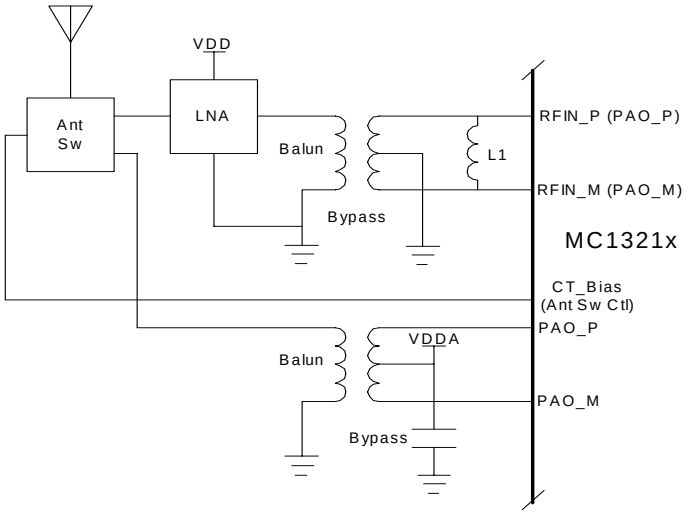
1. Figure 14A shows a single antenna configuration in which the MC1321x internal T/R switch is used. The balun converts the single-ended antenna to differential signals that interface to the RFIN_x (PAO_x) pins of the radio. The CT_Bias pin provides the proper bias point to the balun depending on operation, that is, CT_Bias is at VDDA voltage for transmit and is at ground for receive. The internal T/R switch enables the signal to an onboard LNA for receive and enables the onboard PAs for transmit.
2. Figure 14B shows a single antenna configuration with an external low noise amplifier (LNA) for greater range. An external antenna switch is used to multiplex the antenna between receive and transmit. An LNA is in the receive path to add gain for greater receive sensitivity. Two external baluns are required to convert the single-ended antenna switch signals to the differential signals

required by the radio. Separate RFIN and PAO signals are provided for connection with the baluns, and the CT_Bias signal is programmed to provide the external switch control. The polarity of the external switch control is selectable.

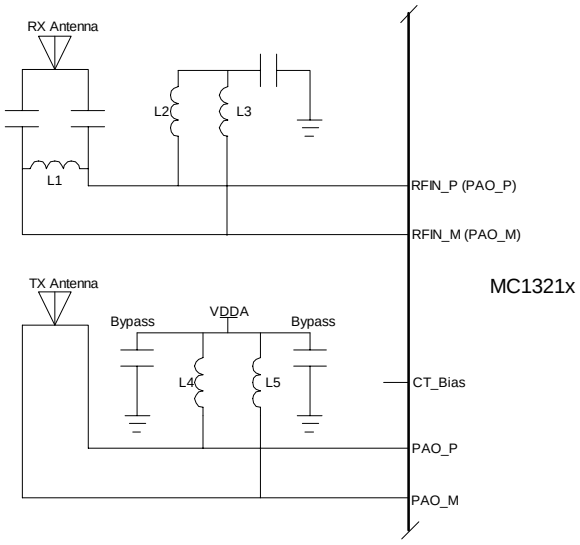
3. Figure 14C shows a dual antenna configuration where there is a RX antenna and a TX antenna. For the receive side, the RX antenna is ac-coupled to the differential RFIN inputs and these capacitors along with inductor L1 form a matching network. Inductors L2 and L3 are ac-coupled to ground to form a frequency trap. For the transmit side, the TX antenna is connected to the differential PAO outputs, and inductors L4 and L5 provide dc-biasing to VDDA but are ac isolated.



14A) Using Onboard T/R Switch



14B) Using External Antenna Switch With LNA

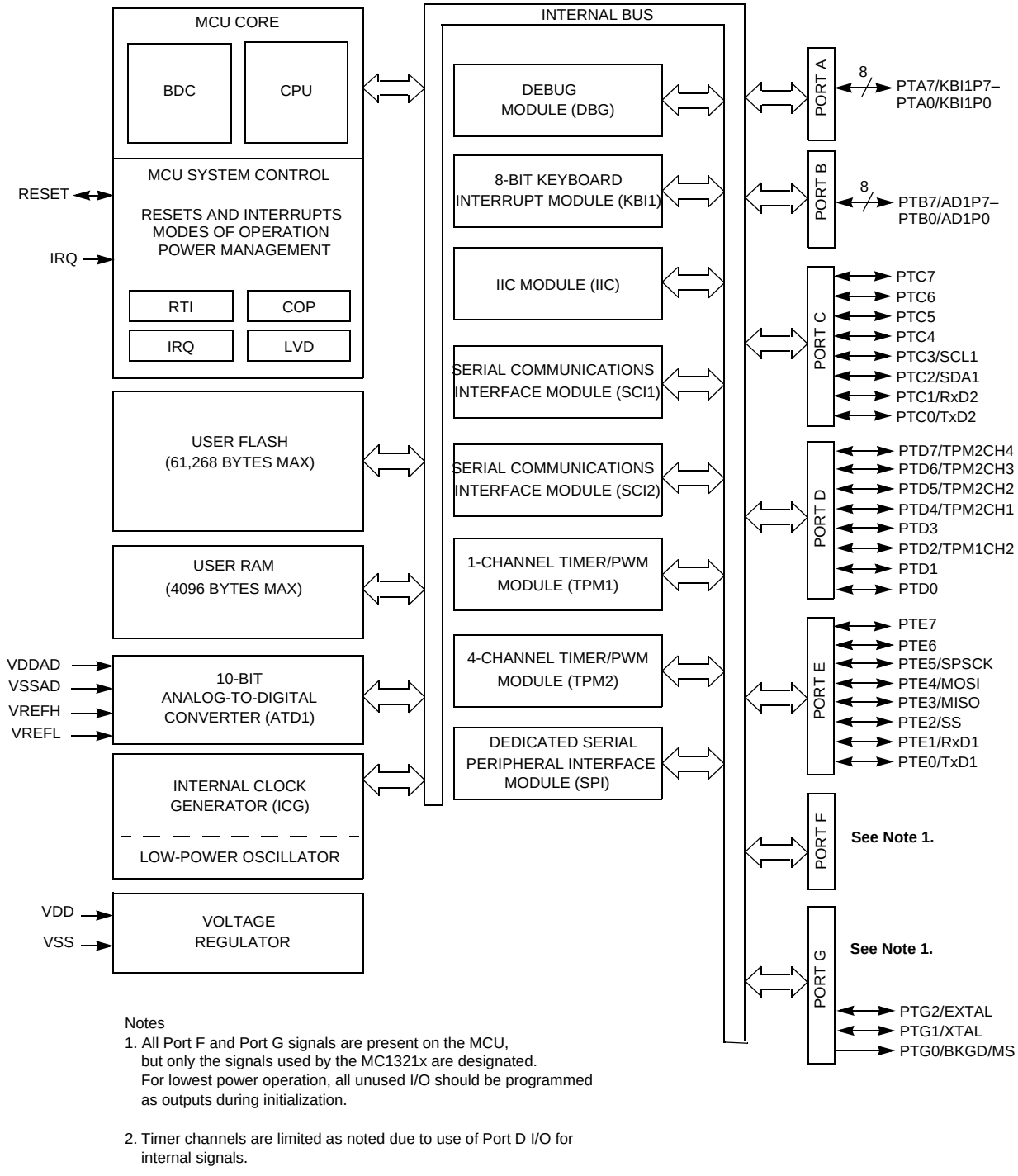


14C) Using Dual Antennae

Figure 14. Using the MC1321x with External RF Components

5 MCU

5.1 MCU Block Diagram



Notes
1. All Port F and Port G signals are present on the MCU, but only the signals used by the MC1321x are designated. For lowest power operation, all unused I/O should be programmed as outputs during initialization.

2. Timer channels are limited as noted due to use of Port D I/O for internal signals.

Figure 15. MCU Block Diagram (HCS08, Version A)

5.2 MCU Modes of Operation

The MCU has multiple operational modes to facilitate maximum system performance while also providing low-power modes. In the MC1321x, the MCU can use the following modes:

- Run
- Wait
- Stop2
- Stop3

NOTE

The MCU can also be programmed for Stop1 mode, but this mode IS NOT USABLE. The reset to the modem function is controlled by an MCU GPIO and the GPIO state must be maintained during the MCU “stop” condition. Stop1 mode does not control I/O states as required during modem power down condition.

5.2.1 Run Mode

This is the normal operating mode for the HCS08. This mode is selected when the BKGD/MS pin is high at the rising edge of reset. In this mode, the CPU executes code from internal memory with execution beginning at the address fetched from memory at $FFFE:$FFFF after reset.

5.2.2 Wait Mode

Wait Mode is entered by executing a WAIT instruction. Upon execution of the WAIT instruction, the CPU enters a low-power state in which it is not clocked. The I bit in CCR is cleared when the CPU enters the wait mode, enabling interrupts. When an interrupt request occurs, the CPU exits the wait mode and resumes processing, beginning with the stacking operations leading to the interrupt service routine.

While the MCU is in Wait Mode, there are some restrictions on which background debug commands can be used. Only the BACKGROUND command and memory-access-with-status commands are available when the MCU is in wait mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from Wait Mode and enter active background mode.

5.2.3 Stop 2

The Stop2 Mode provides very low standby power consumption and maintains the contents of RAM and the current state of all of the I/O pins. Stop2 can be entered only if the LVD circuit is not enabled in Stop Modes (either LVDE or LVDSE not set).

Before entering Stop2 Mode, the user must save the contents of the I/O port registers, as well as any other memory-mapped registers they want to restore after exit of Stop2, to locations in RAM. Upon exit of Stop2, these values can be restored by user software before pin latches are opened.

When the MCU is in Stop2 Mode, all internal circuits that are powered from the voltage regulator are turned off, except for the RAM. The voltage regulator is in a low-power standby state, as is the ATD. Upon entry into Stop2, the states of the I/O pins are latched. The states are held while in Stop2 Mode and after exiting Stop2 Mode until a 1 is written to PPDACK in SPMSC2.

Exit from Stop2 is performed by asserting either of the wake-up pins: $\overline{\text{RESET}}$ or IRQ, or by an RTI interrupt. IRQ is always an active low input when the MCU is in Stop2, regardless of how it was configured before entering Stop2.

Upon wake-up from Stop2 Mode, the MCU will start up as from a power-on reset (POR) except pin states remain latched. The CPU will take the reset vector. The system and all peripherals will be in their default reset states and must be initialized.

After waking up from Stop2, the PPDF bit in SPMSC2 is set. This flag may be used to direct user code to go to a Stop2 recovery routine. PPDF remains set and the I/O pin states remain latched until a 1 is written to PPDACK in SPMSC2.

To maintain I/O state for pins that were configured as general-purpose I/O, the user must restore the contents of the I/O port registers, which have been saved in RAM, to the port registers before writing to the PPDACK bit. If the port registers are not restored from RAM before writing to PPDACK, then the register bits will assume their reset states when the I/O pin latches are opened and the I/O pins will switch to their reset states.

For pins that were configured as peripheral I/O, the user must reconfigure the peripheral module that interfaces to the pin before writing to the PPDACK bit. If the peripheral module is not enabled before writing to PPDACK, the pins will be controlled by their associated port control registers when the I/O latches are opened.

A separate self-clocked source (approximately 1 kHz) for the real-time interrupt allows a walk-up from Stop2 or Stop3 Modes with no external components. When RTIS2:RTIS1:RTIS0 = 0:0:0, the real-time interrupt function and this 1-kHz source are disabled. Power consumption is lower when the 1-kHz source is disabled, but in that case the real-time interrupt cannot wake the MCU from stop.

5.2.4 Stop3

Upon entering the Stop3 Mode, all of the clocks in the MCU, including the oscillator itself, are halted. The ICG is turned off, the ATD is disabled, and the voltage regulator is put in standby. The states of all of the internal registers and logic, as well as the RAM content, are maintained. The I/O pin states are not latched at the pin as in Stop2. Instead they are maintained by virtue of the states of the internal logic driving the pins being maintained.

Exit from Stop3 is performed by asserting $\overline{\text{RESET}}$, an asynchronous interrupt pin, or through the real-time interrupt. The asynchronous interrupt pins are the IRQ or KBI pins.

If Stop3 is exited by means of the $\overline{\text{RESET}}$ pin, then the MCU will be reset and operation will resume after taking the reset vector. Exit by means of an asynchronous interrupt or the real-time interrupt will result in the MCU taking the appropriate interrupt vector.

A separate self-clocked source (approximately1 kHz) for the real-time interrupt allows a wake up from Stop2 or Stop3 Modes with no external components. When RTIS2:RTIS1:RTIS0 = 0:0:0, the real-time interrupt function and this 1-kHz source are disabled. Power consumption is lower when the 1-kHz source is disabled, but in that case the real-time interrupt cannot wake the MCU from stop.

5.3 MCU Memory

As shown in Figure 16, on-chip memory in the MC1321x series of MCUs consists of RAM, FLASH program memory for non-volatile data storage, plus I/O and control/status registers. The registers are divided into three groups:

- Direct-page registers ($0000 through $007F)
- High-page registers ($1800 through $182B)
- Nonvolatile registers ($FFB0 through $FFBF)

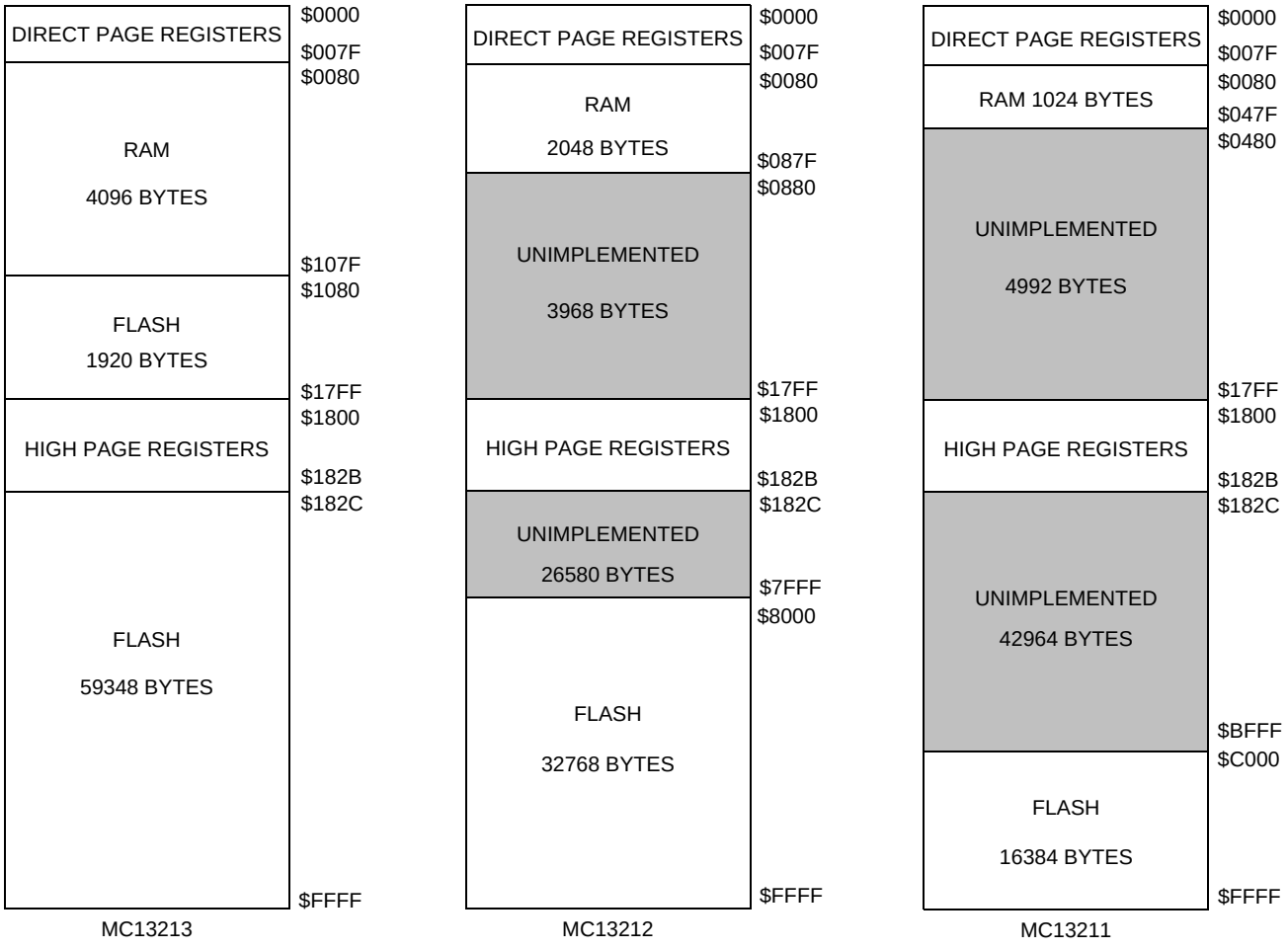


Figure 16. MC1321X Memory Maps

5.4 MCU Internal Clock Generator (ICG)

The ICG provides multiple options for MCU clock sources. This block along with the ability to provide the MCU clock form the modem offers a user great flexibility when making choices between cost, precision, current draw, and performance. As seen in Figure 17, the ICG consists of four functional blocks.

- **Oscillator Block** — The Oscillator Block provides means for connecting an external crystal or resonator. Two frequency ranges are software selectable to allow optimal start-up and stability. Alternatively, the oscillator block can be used to route an external square wave to the MCU system clock. External sources such as the modem CLKO output can provide a low cost source or a very precise clock source. The oscillator is capable of being configured for low power mode or high amplitude mode as selected by HGO.
- **Internal Reference Generator** — The Internal Reference Generator consists of two controlled clock sources. One is designed to be approximately 8 MHz and can be selected as a local clock for the background debug controller. The other internal reference clock source is typically 243 kHz and can be trimmed for finer accuracy via software when a precise timed event is input to the MCU. This provides a highly reliable, low-cost clock source.
- **Frequency-Locked Loop** — A Frequency-Locked Loop (FLL) stage takes either the internal or external clock source and multiplies it to a higher frequency. Status bits provide information when the circuit has achieved lock and when it falls out of lock. Additionally, this block can monitor the external reference clock and signals whether the clock is valid or not.
- **Clock Select Block** — The Clock Select Block provides several switch options for connecting different clock sources to the system clock tree. ICGDCLK is the multiplied clock frequency out of the FLL, ICGERCLK is the reference clock frequency from the crystal or external clock source, and FFE (fixed frequency enable) is a control signal used to control the system fixed frequency clock (XCLK). ICGLCLK is the clock source for the background debug controller (BDC).

The module is intended to be very user friendly with many of the features occurring automatically without user intervention.

5.4.1 Features

Features of the ICG and clock distribution system:

- Several options for the MCU primary clock source allow a wide range of cost, frequency, and precision choices:
  - 32 kHz–100 kHz crystal or resonator
  - 1 MHz–16 MHz crystal or resonator
  - External clock supplied by modem CLKO or other source
  - Internal reference generator
- Defaults to self-clocked mode to minimize startup delays
- Frequency-locked loop (FLL) generates 8 MHz to 40 MHz (for bus rates up to 20 MHz). When using modem CLKO as external source, maximum FLL frequency is 32 MHz (16 MHz bus rate) with CLKO = 16 MHz or maximum FLL frequency is 40 MHz (20 MHz bus rate) with CLKO = 4 MHz.

— Uses external or internal clock as reference frequency

- Automatic lockout of non-running clock sources
- Reset or interrupt on loss of clock or loss of FLL lock
- Digitally-controlled oscillator (DCO) preserves previous frequency settings, allowing fast frequency lock when recovering from stop3 mode
- DCO will maintain operating frequency during a loss or removal of reference clock. When FLL is engaged (FEE or FEI) loss of lock or loss of clock adds a divide-by-2 to ICG to prevent over-clocking of the system.
- Post-FLL divider selects 1 of 8 bus rate divisors (/1 through /128)
- Separate self-clocked source for real-time interrupt
- Trimmable internal clock source supports SCI communications without additional external components
- Automatic FLL engagement after lock is acquired
- Selectable low-power/high-gain oscillator modes

5.4.2 Modes of Operation

This section provides a high-level description only.

- Mode 1 — Off

  The output clock, ICGOUT, is static. This mode may be entered when the STOP instruction is executed.

- Mode 2 — Self-clocked (SCM)

  Default mode of operation that is entered out of reset. The ICG's FLL is open loop and the digitally controlled oscillator (DCO) is free running at a frequency set by the filter bits.

- Mode 3 — FLL engaged internal (FEI)

  In this mode, the ICG's FLL is used to create frequencies that are programmable multiples of the internal reference clock.

  — FLL engaged internal unlocked is a transition state which occurs while the FLL is attempting to lock. The FLL DCO frequency is off target and the FLL is adjusting the DCO to match the target frequency.

  — FLL engaged internal locked is a state which occurs when the FLL detects that the DCO is locked to a multiple of the internal reference.

- Mode 4 — FLL bypassed external (FBE)

  In this mode, the ICG is configured to bypass the FLL and use an external clock as the clock source.

- Mode 5 — FLL engaged external (FEE)

  The ICG's FLL is used to generate frequencies that are programmable multiples of the external clock reference.

  — FLL engaged external unlocked is a transition state which occurs while the FLL is attempting to lock. The FLL DCO frequency is off target and the FLL is adjusting the DCO to match the target frequency.

— FLL engaged external locked is a state which occurs when the FLL detects that the DCO is locked to a multiple of the internal reference.

Figure 17 is a top-level diagram that shows the functional organization of the internal clock generation (ICG) module.

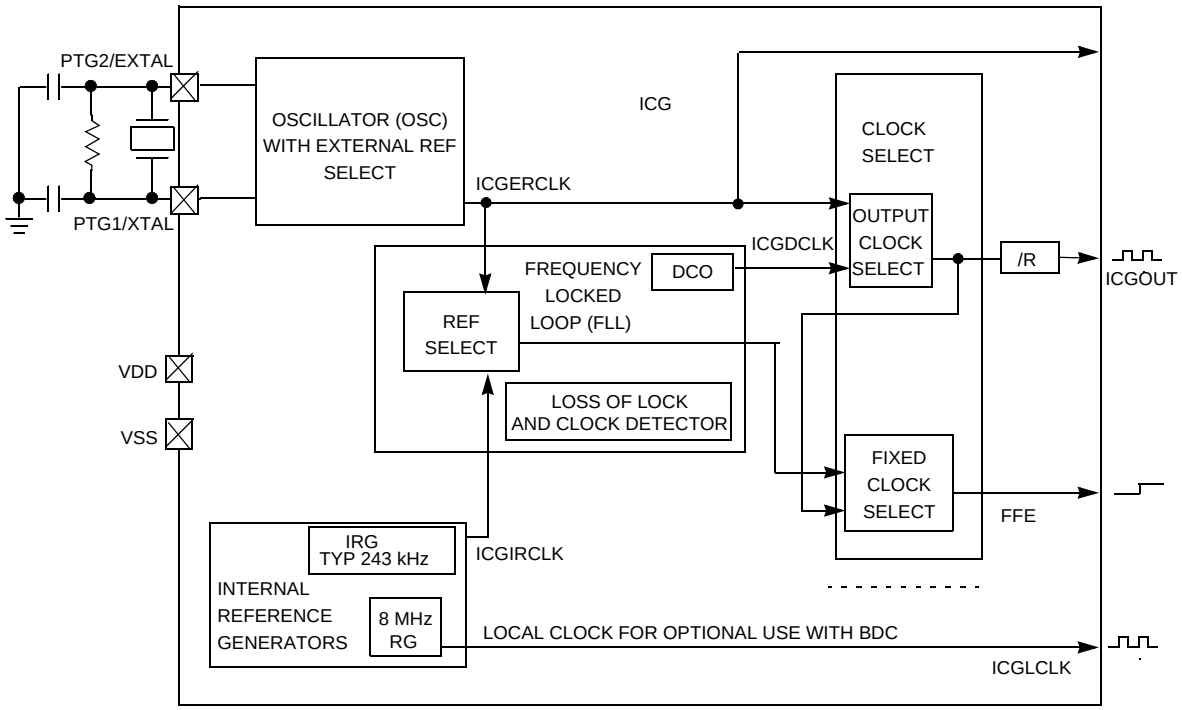


Figure 17. ICG Block Diagram

5.5 Central Processing Unit (CPU)

The HCS08 CPU is fully source- and object-code-compatible with the M68HC08 CPU. Several instructions and enhanced addressing modes were added to improve C compiler efficiency and to support a new background debug system which replaces the monitor mode of earlier M68HC08 microcontrollers (MCU).

5.5.1 CPU Features

Features of the CPU include:

- Object code fully upward-compatible with M68HC05 and M68HC08 Families
- All registers and memory are mapped to a single 64-Kbyte address space
- 16-bit stack pointer (any size stack anywhere in 64-Kbyte address space)
- 16-bit index register (H:X) with powerful indexed addressing modes
- 8-bit accumulator (A)
- Many instructions treat X as a second general-purpose 8-bit register
- Seven addressing modes:

- Inherent — Operands in internal registers
- Relative — 8-bit signed offset to branch destination
- Immediate — Operand in next object code byte(s)
- Direct — Operand in memory at 0x0000–0x00FF
- Extended — Operand anywhere in 64-Kbyte address space
- Indexed relative to H:X — Five submodes including auto increment
- Indexed relative to SP — Improves C efficiency dramatically

- Memory-to-memory data move instructions with four address mode combinations
- Overflow, half-carry, negative, zero, and carry condition codes support conditional branching on the results of signed, unsigned, and binary-coded decimal (BCD) operations
- Efficient bit manipulation instructions
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- STOP and WAIT instructions to invoke low-power operating modes

5.5.2 Programmer's Model and CPU Registers

Figure 18 shows the five CPU registers. CPU registers are not part of the memory map.

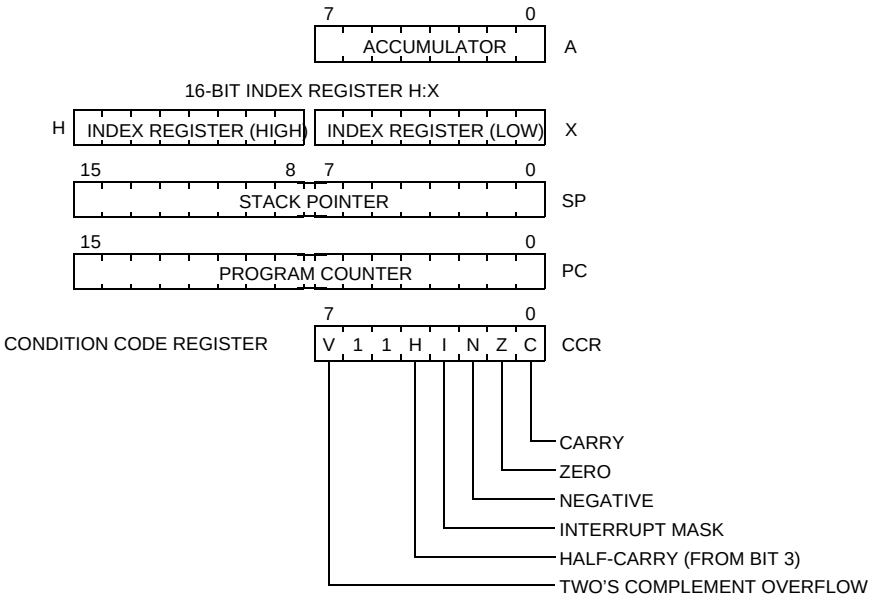


Figure 18. CPU Registers

5.6 Parallel Input/Output

The MC1321x HCS08 has seven I/O ports which include a total of 56 general-purpose I/O signals (one of these pins, PTG0, is output only). The MC1321x family does not use all the these signals as denoted in Figure 15. Port F and part of port G are not utilized. The MC1321x family makes use of the remaining I/O as pinned-out I/O or as internally dedicated signal for communication with the 802.15.4 modem.

As stated above port F and part of port G are not utilized. These signals and any unused IO should be programmed as outputs during initialization for lowest power operation. Many of these pins are shared with on-chip peripherals such as timer systems, various communication ports, or keyboard interrupts. When these other modules are not controlling the port pins, they revert to general-purpose I/O control. For each I/O pin, a port data bit provides access to input (read) and output (write) data, a data direction bit controls the direction of the pin, and a pullup enable bit enables an internal pullup device (provided the pin is configured as an input), and a slew rate control bit controls the rise and fall times of the pins.Parallel I/O features include:

- A total of 32 general-purpose I/O pins in seven ports (PTG0 is output only)
- High-current drivers on port C
- Hysteresis input buffers
- Software-controlled pullups on each input pin
- Software-controlled slew rate output buffers
- Eight port A pins shared with KBI1
- Eight port B pins shared with ATD1
- Eight high-current port C pins shared with SCI2 and IIC1
- Eight port D pins shared with TPM1 and TPM2
- Eight port E pins shared with SCI1 and SPI1
- Eight port G pins shared with EXTAL, XTAL, and BKGD/MS

NOTE

Not all port G signals and no port F signals are bonded out, but are present in the MCU hardware (see Figure 15). These port I/O signals should be programmed as outputs set to the low state.

5.7 MCU Peripherals

5.7.1 Modem Dedicated Serial Peripheral Interface (SPI) Module

The HCS08 provides one serial peripheral interface (SPI) module which is connected within the SiP to the modem SPI port. The four pins associated with SPI functionality are shared with port E pins 2–5. When the SPI is enabled, the direction of pins is controlled by module configuration.

The MCU SPI port is used only in master mode on the MC1321x family. The user must program the SPI module for the proper characteristics as listed in the features below and also program the $\overline{SS}$ signal to have the proper use to support the modem transaction protocol for the modem $\overline{CE}$ signal.

5.7.1.1 SPI Features

Features of the SPI module use include:

- Used in master mode only
- Programmable transmit bit rate (maximum usable rate is 8 MHz with modem)
- Double-buffered transmit and receive
- Serial clock phase and polarity option must be programmed to CPHA = 0 and CPOL = 0
- Programmable slave select output to support modem SPI protocol
- MSB-first data transfer

5.7.1.2 SPI Module Block Diagram

Figure 19 is a block diagram of the SPI module. The central element of the SPI is the SPI shift register. Data is written to the double-buffered transmitter (write to SPI1D) and gets transferred to the SPI shift register at the start of a data transfer. After shifting in a byte of data, the data is transferred into the double-buffered receiver where it can be read (read from SPI1D). Pin multiplexing logic controls connections between MCU pins and the SPI module.

When the SPI is configured as a master, the clock output is routed to the SPSCK pin, the shifter output is routed to MOSI, and the shifter input is routed from the MISO pin.

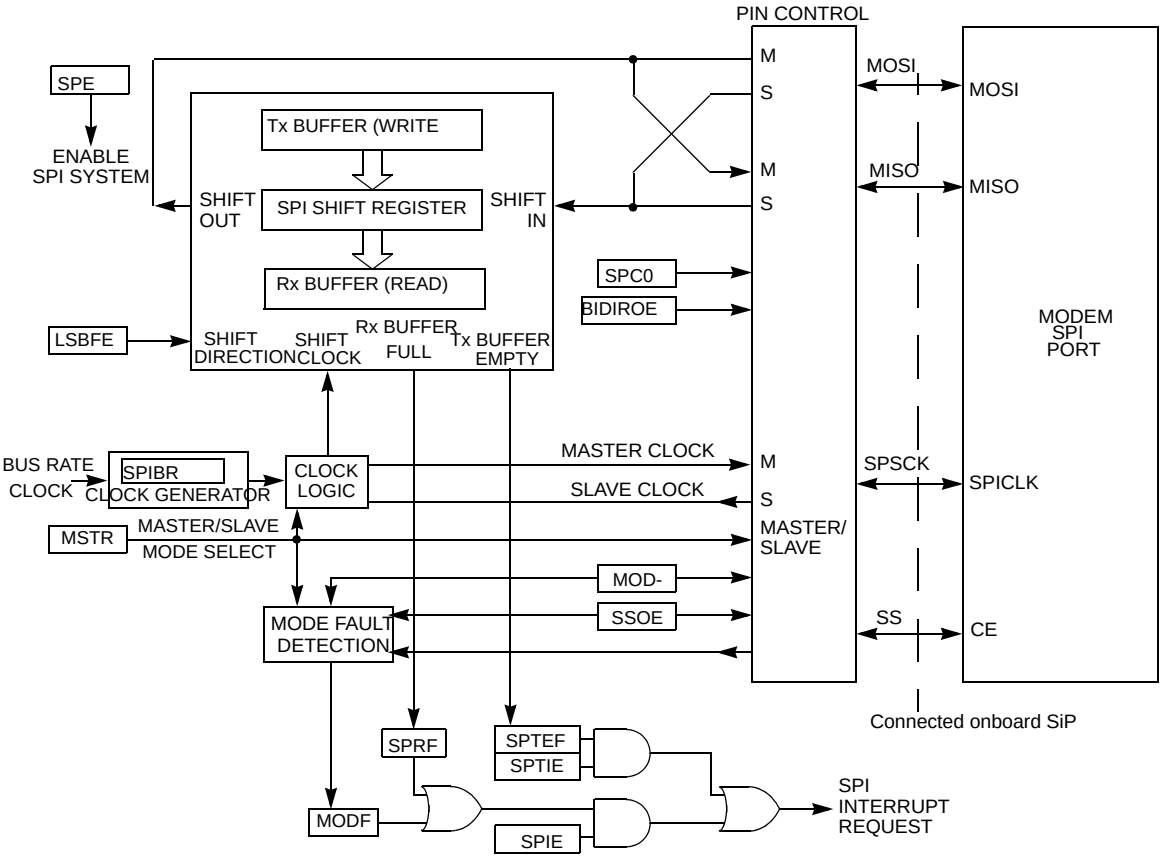


Figure 19. Modem Dedicated SPI Block Diagram

5.7.2 Keyboard Interrupt (KBI) Module

The HCS08 has one KBI module with eight keyboard interrupt inputs that share port A pins.

The KBI module allows up to eight pins to act as additional interrupt sources. Four of these pins allow falling-edge sensing while the other four can be configured for either rising-edge sensing or falling-edge sensing. The sensing mode for all eight pins can also be modified to detect edges and levels instead of only edges.

This on-chip peripheral module is called a keyboard interrupt (KBI) module because originally it was designed to simplify the connection and use of row-column matrices of keyboard switches. However, these inputs are also useful as extra external interrupt inputs and as an external means of waking up the MCU from stop or wait low-power modes.

5.7.3 KBI Features

The keyboard interrupt (KBI) module features include:

- Keyboard interrupts selectable on eight port pins:
  - — Four falling-edge/low-level sensitive
  - — Four falling-edge/low-level or rising-edge/high-level sensitive
  - — Choice of edge-only or edge-and-level sensitivity
  - — Common interrupt flag and interrupt enable control
  - — Capable of waking up the MCU from stop3 or wait mode

5.7.3.1 KBI Block Diagram

Figure 20 shows the block diagram for the KBI module.

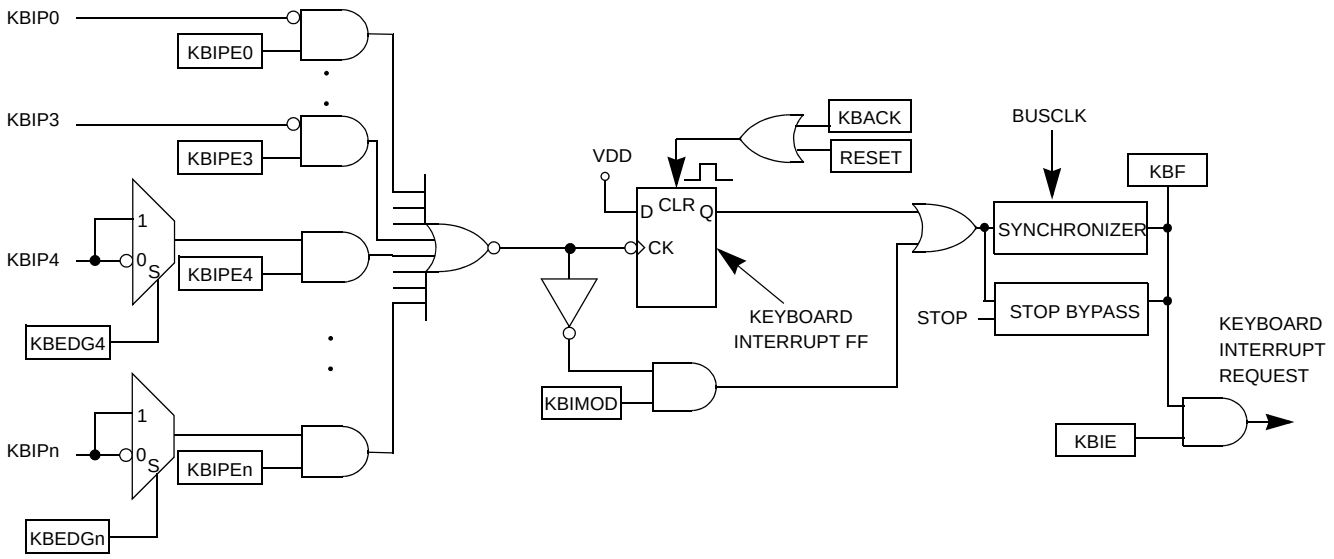


Figure 20. KBI Block Diagram

5.7.4 Timer/PWM (TPM) Module Introduction

The HCS08 includes two independent Timer/PWM (TPM) modules which support traditional input capture, output compare, or buffered edge-aligned pulse-width modulation (PWM) on each channel. A control bit in each TPM configures all channels in that timer to operate as center-aligned PWM functions. In each of these two TPMs, timing functions are based on a separate 16-bit counter with prescaler and modulo features to control frequency and range (period between overflows) of the time reference. This timing system is ideally suited for a wide range of control applications, and the center-aligned PWM capability on the 3-channel TPM extends the field of applications to motor control in small appliances.

The use of the fixed system clock, XCLK, as the clock source for either of the TPM modules allows the TPM prescaler to run using the oscillator rate divided by two (ICGERCLK/2). This clock source must be selected only if the ICG is configured in either FBE or FEE mode. In FBE mode, this selection is redundant because the BUSCLK frequency is the same as XCLK. In FEE mode, the proper conditions must be met for XCLK to equal ICGERCLK/2. Selecting XCLK as the clock source with the ICG in either FEI or SCM mode will result in the TPM being non-functional.

5.7.4.1 TPM Features

The timer system in the MC1321x family MCU includes a 1-channel TPM1 and a separate 4-channel TPM2. Timer system features include:

- A total of 5 channels:
  - Each channel may be input capture, output compare, or buffered edge-aligned PWM
  - Rising-edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
  - Selectable polarity on PWM outputs
- Each TPM may be configured for buffered, center-aligned pulse-width modulation (CPWM) on all channels
- Clock source to prescaler for each TPM is independently selectable as bus clock, fixed system clock, or an external pin
- Prescale taps for divide by 1, 2, 4, 8, 16, 32, 64, or 128
- 16-bit free-running or up/down (CPWM) count operation
- 16-bit modulus register to control counter range
- Timer system enable
- One interrupt per channel plus terminal count interrupt

5.7.4.2 TPM Block Diagram

The TPM uses one input/output (I/O) pin per channel, TPMxCHn where x is the TPM number (for example, 1 or 2) and n is the channel number (for example, 1–4). The TPM shares its I/O pins with general-purpose I/O port pins. Figure 21 shows the structure of a TPM. Some MCUs include more than one TPM, with various numbers of channels.

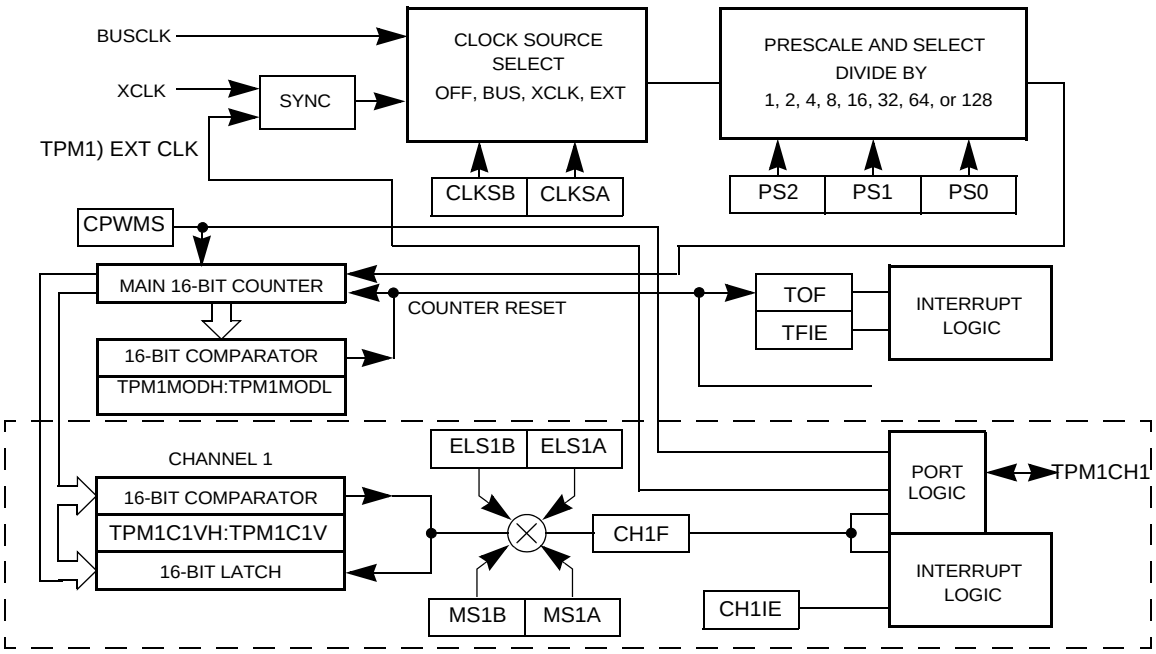


Figure 21. TPM Block Diagram

5.7.5 Serial Communications Interface (SCI) Module

The HCS08 includes two independent serial communications interface (SCI) modules — sometimes called universal asynchronous receiver/transmitters (UARTs). Typically, these systems are used to connect to the RS232 serial input/output (I/O) port of a personal computer or workstation, and they can also be used to communicate with other embedded controllers.

A flexible, 13-bit, modulo-based baud rate generator supports a broad range of standard baud rates beyond 115.2 kbaud. Transmit and receive within the same SCI use a common baud rate, and each SCI module has a separate baud rate generator.

This SCI system offers many advanced features not commonly found on other asynchronous serial I/O peripherals on other embedded controllers. The receiver employs an advanced data sampling technique that ensures reliable communication and noise detection. Hardware parity, receiver wakeup, and double buffering on transmit and receive are also included.

5.7.5.1 SCI Features

Features of SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - — Transmit data register empty and transmission complete
  - — Receive data register full

— Receive overrun, parity error, framing error, and noise error
— Idle receiver detect

- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Receiver walk-up by idle-line or address-mark

5.7.5.2 SCI Block Diagrams

The SCI allows full-duplex, asynchronous, NRZ serial communication among the MCU and remote devices, including other MCUs. The SCI comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator. During normal operation, the MCU monitors the status of the SCI, writes the data to be transmitted, and processes received data. Figure 22 and Figure 23 show the SCI transmitter and receiver block diagrams.

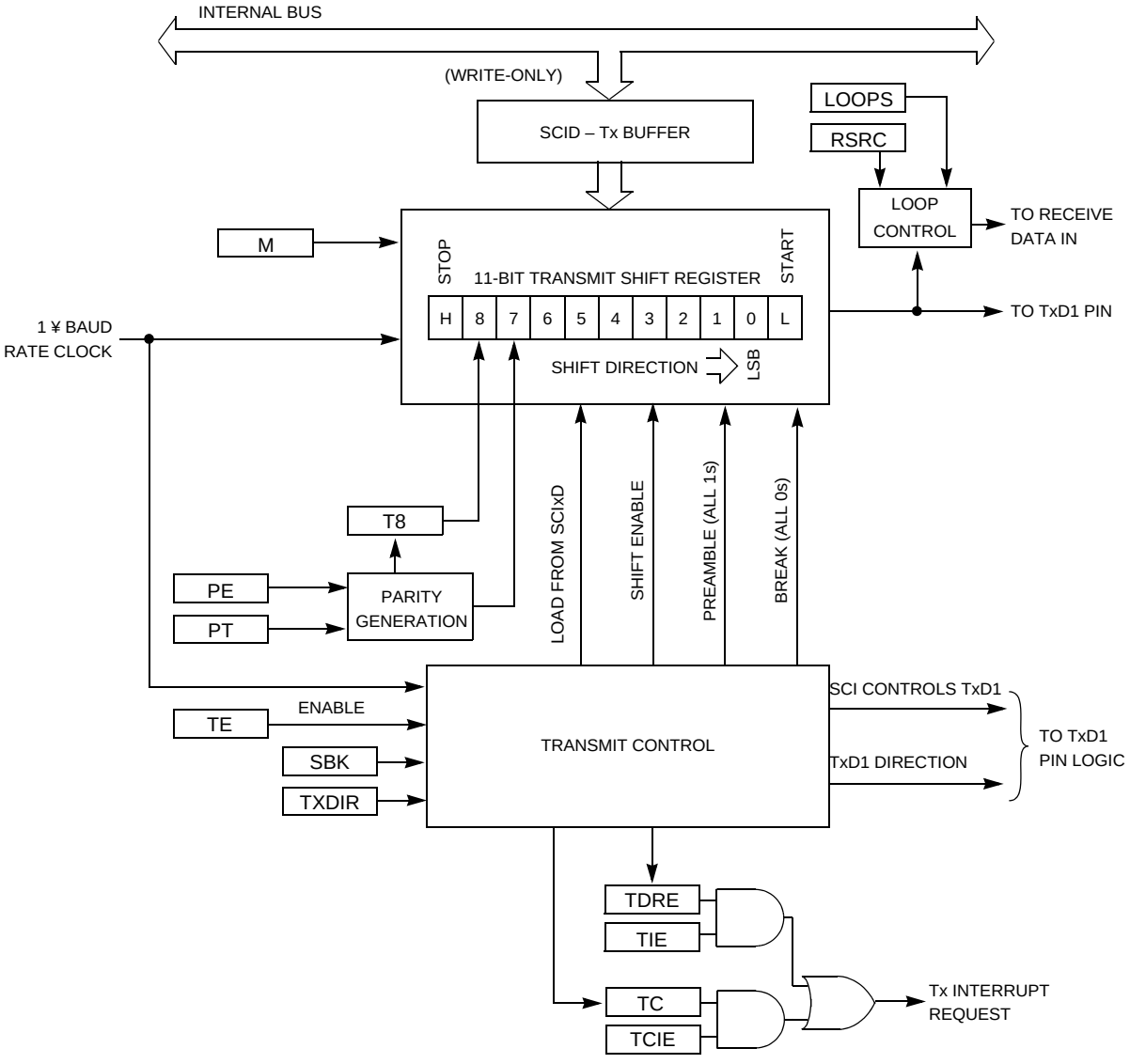


Figure 22. SCI Transmitter

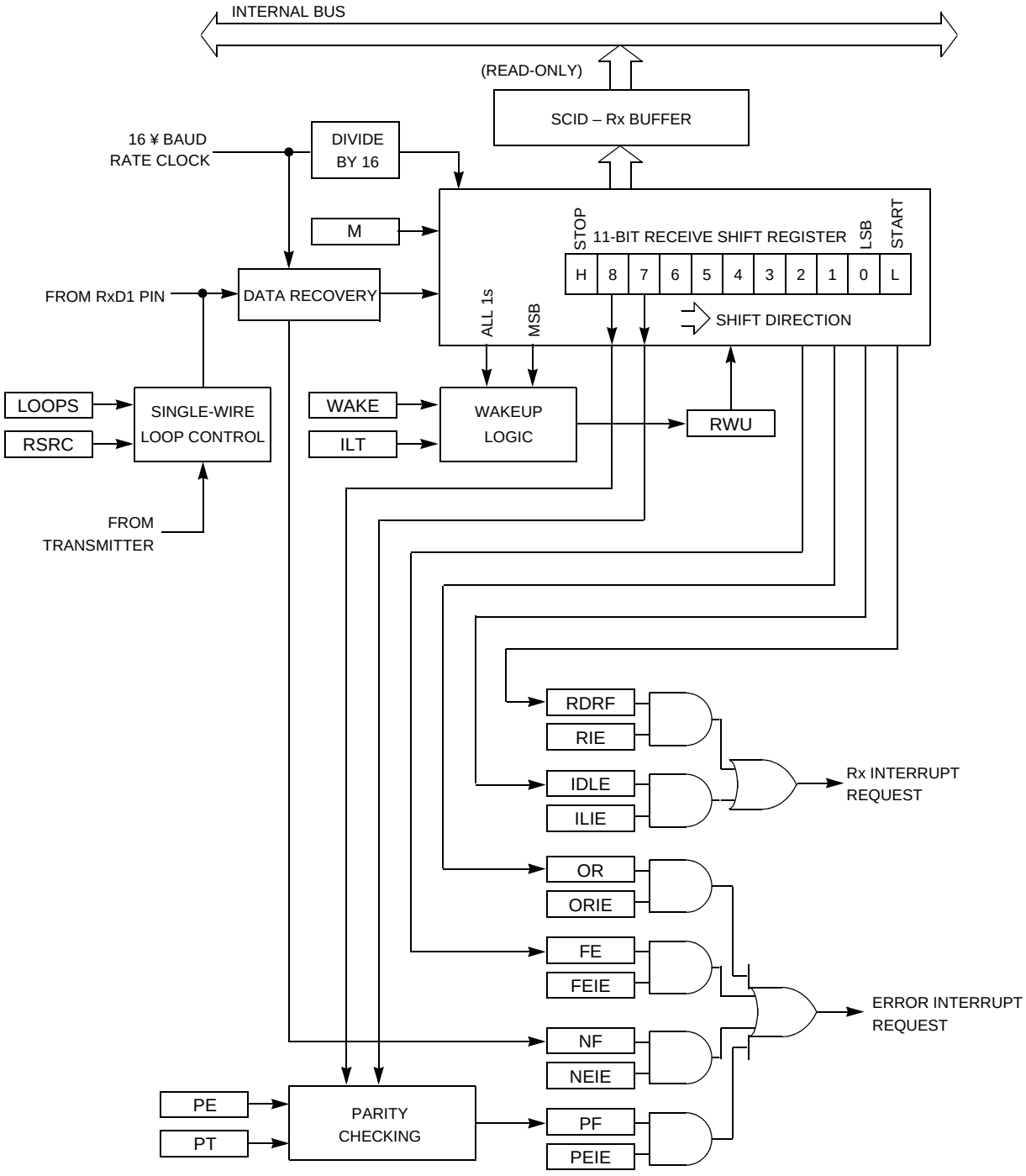


Figure 23. SCI Receiver

5.7.6 Inter-Integrated Circuit (IIC) Module

The HCS08 microcontroller provides one inter-integrated circuit (IIC) module for communication with other integrated circuits. The two pins associated with this module, SDA and SCL share port C pins 2 and 3, respectively. All functionality as described in this section is available on HCS08. When the IIC is enabled, the direction of pins is controlled by module configuration. If the IIC is disabled, both pins can be used as general-purpose I/O.

The inter-integrated circuit (IIC) provides a method of communication between a number of devices{statement}. The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

5.7.6.1 IIC Features

The IIC includes these features:

- IP bus V2.0 compliant Compatible with IIC bus standard
- Multi-master operation {statement}
- Software programmable for one of 64 different serial clock frequencies {iic_prescale.asm}
- Software selectable acknowledge bit {iic_ack.asm}
- Interrupt driven byte-by-byte data transfer {iic_int.asm}
- Arbitration lost interrupt with automatic mode switching from master to slave {iic_int.asm}
- Calling address identification interrupt {iic_int.asm}
- START and STOP signal generation/detection {iic_transmit.asm}{iic_receive.asm}{iic_receive_addon.asm}
- Repeated START signal generation {iic_transmit.asm}
- Acknowledge bit generation/detection {iic_ack.asm}
- Bus busy detection {iic_bus_busy.asm}

5.7.6.2 IIC Modes of Operation

The IIC functions the same in normal and monitor modes. A brief description of the IIC in the various MCU modes is given here.

Run mode	This is the basic mode of operation. To conserve power in this mode, disable the module.
Wait mode	The module will continue to operate while the MCU is in wait mode and can provide a wake-up interrupt.
Stop mode	The IIC is inactive in Stop3 Mode for reduced power consumption. The STOP instruction does not affect IIC register states. Stop1 and Stop2 will reset the register contents.

5.7.6.3 IIC Block Diagram

Figure 24 shows a block diagram of the IIC module.

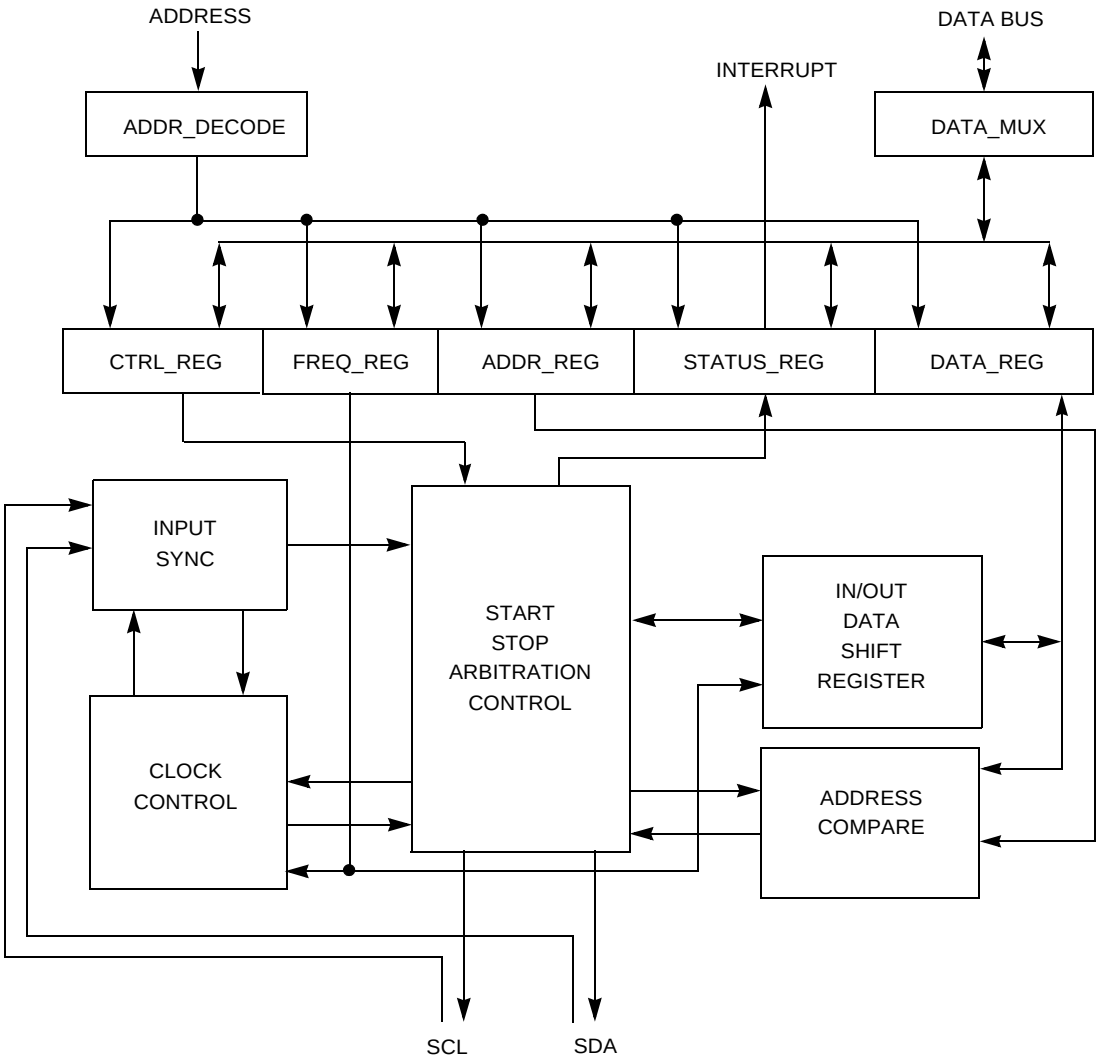


Figure 24. IIC Functional Block Diagram

5.7.7 Analog-to-Digital (ATD) Module

The HCS08 provides one 8-channel analog-to-digital (ATD) module. The eight ATD channels share Port B. Each channel individually can be configured for general-purpose I/O or for ATD functionality.

5.7.7.1 ATD Features

- 8-/10-bit resolution
- 14.0 μsec, 10-bit single conversion time at a conversion frequency of 2 MHz
- Left-/right-justified result data
- Left-justified signed data mode
- Conversion complete flag or conversion complete interrupt generation
- Analog input multiplexer for up to eight analog input channels
- Single or continuous conversion mode

5.7.7.2 ATD Modes of Operation

The ATD has two modes for low power

1. Stop mode
2. Power-down mode

5.7.7.2.1 ATD Stop Mode

When the MCU goes into Stop Mode, the MCU stops the clocks and the ATD analog circuitry is turned off, placing the module into a low-power state. Once in stop mode, the ATD module aborts any single or continuous conversion in progress. Upon exiting stop mode, no conversions occur and the registers have their previous values. As long as the ATDPU bit is set prior to entering stop mode, the module is reactivated coming out of stop.

5.7.7.2.2 ATD Power Down Mode

Clearing the ATDPU bit in register ATD1C also places the ATD module in a low-power state. The ATD conversion clock is disabled and the analog circuitry is turned off, placing the module in power-down mode. (This mode does not remove power to the ATD module.) Once in power-down mode, the ATD module aborts any conversion in progress. Upon setting the ATDPU bit, the module is reactivated. During power-down mode, the ATD registers are still accessible.

NOTE

The reset state of the ATDPU bit is zero. Therefore, the module is reset into the power-down state.

5.7.7.3 ATD Block Diagram

Figure 25 shows the functional structure of the ATD module.

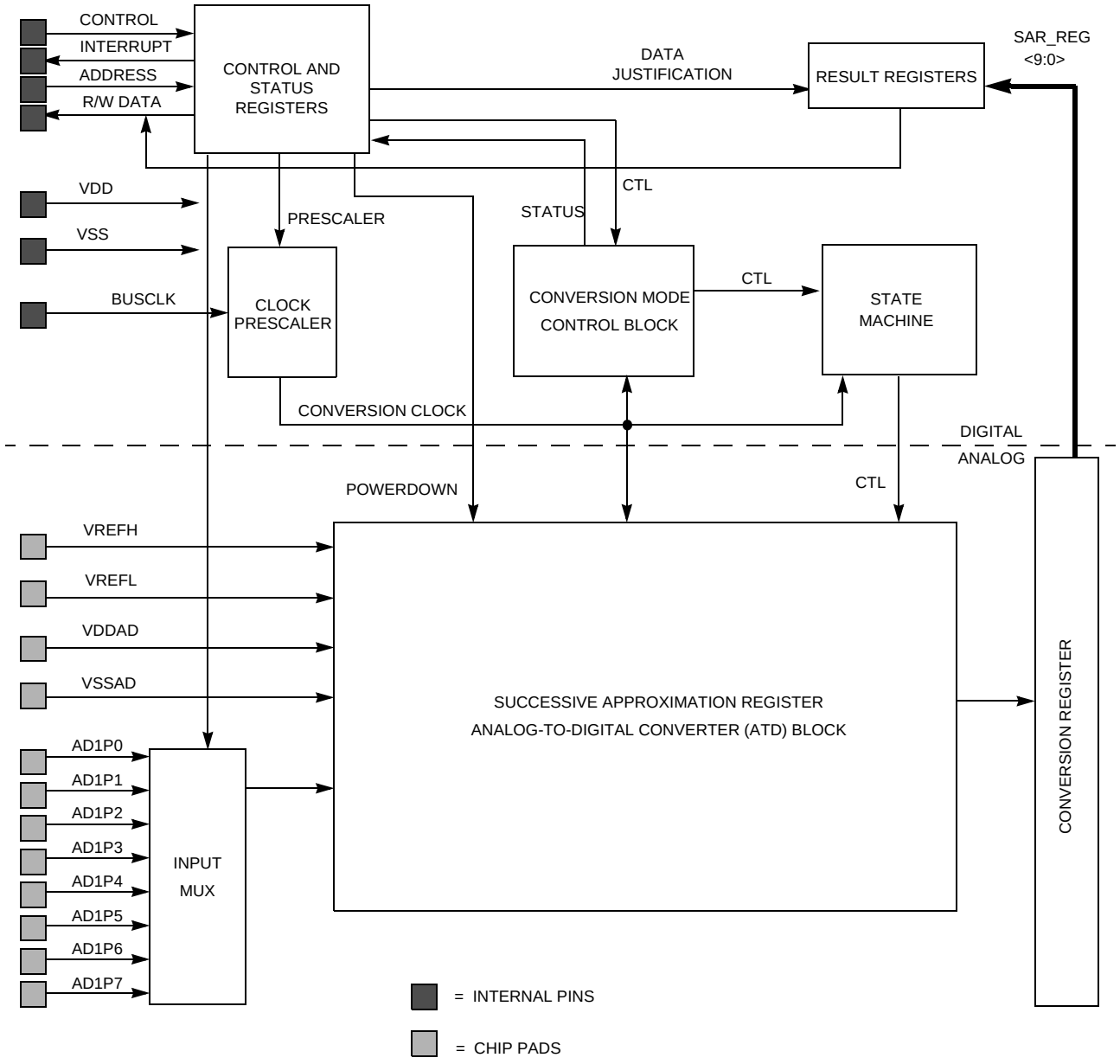


Figure 25. ATD Block Diagram

5.7.8 Development Support

Development support systems in the include the background debug controller (BDC) and the on-chip debug module (DBG). The BDC provides a single-wire debug interface to the target MCU that provides a convenient interface for programming the on-chip FLASH and other non-volatile memories. The BDC is also the primary debug interface for development and allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

Address and data bus signals are not available on external pins (not even in test modes). Debug is done through commands fed into the MCU via the single-wire background debug interface. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals.

The alternate BDC clock source for HCS08 is the ICGLCLK.

5.7.8.1 Development Support Features

Features of the background debug controller (BDC) include:

- Single pin for mode selection and background communications
- BDC registers are not located in the memory map
- SYNC command to determine target communications rate
- Non-intrusive commands for memory access
- Active background mode commands for CPU register access
- GO and TRACE1 commands
- BACKGROUND command can wake CPU from stop or wait modes
- One hardware address breakpoint built into BDC
- Oscillator runs in stop mode, if BDC enabled
- COP watchdog disabled while in active background mode

Features of the debug module (DBG) include:

- Two trigger comparators:
  - — Two address + read/write (R/W) or
  - — One full address + data + R/W
- Flexible 8-word by 16-bit FIFO (first-in, first-out) buffer for capture information:
  - — Change-of-flow addresses or
  - — Event-only data
- Two types of breakpoints:
  - — Tag breakpoints for instruction opcodes
  - — Force breakpoints for any address access
- Nine trigger modes:

— A-only
— A OR B
— A then B
— A AND B data (full mode)
— A AND NOT B data (full mode)
— Event-only B (store data)
— A then event-only B (store data)
— Inside range (A ≤ address ≤ B)
— Outside range (address < A or address > B)

6 System Electrical Specification

This section details maximum ratings for the 71 pin LGA package and recommended operating conditions, DC characteristics, and AC characteristics for the modem, and the MCU.

6.1 SiP LGA Package Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum rating is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 6 shows the maximum ratings for the 71 Pin LGA package.

Table 6. LGA Package Maximum Ratings

Rating	Symbol	Value	Unit
Maximum Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	-55 to 125	°C
Power Supply Voltage	V_{BATT}, V_{DDINT}	-0.3 to 3.6	Vdc
Digital Input Voltage	Vin	-0.3 to (V_{DDINT} + 0.3)	
RF Input Power	P_{max}	10	dBm
Maximum Current into V_{DD}	I_{DD}	120	mA
Instantaneous Maximum Current (Single Pin Limit)[1, 2, 3]	I_D	± 25	mA

Note: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

Note: Meets Human Body Model (HBM) = 2 kV. RF input/output pins have no ESD protection.

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

6.2 802.15.4 Modem Electrical Characteristics

6.2.1 Modem Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage ($V_{BATT} = V_{DDINT}$)[1]	V_{BATT}, V_{DDINT}	2.0	2.7	3.4	Vdc
Input Frequency	f_{in}	2.405	-	2.480	GHz
Operating Temperature Range	T_A	-40	25	85	°C
Logic Input Voltage Low	V_{IL}	0	-	30% V_{DDINT}	V
Logic Input Voltage High	V_{IH}	70% V_{DDINT}	-	V_{DDINT}	V
SPI Clock Rate	f_{SPI}	-	-	8.0	MHz
RF Input Power	P_{max}	-	-	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	f_{ref}	16 MHz Only			

[1] If the supply voltage is produced by a switching DC-DC converter, ripple should be less than 100 mV peak-to-peak.

6.2.2 Modem DC Electrical Characteristics

Table 8. DC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_{BATT} + V_{DDINT}) Off[1] Hibernate[1] Doze (No CLKO)[1 2] Idle Transmit Mode (0 dBm nominal output power) Receive Mode	 $I_{leakage}$ I_{CCH} I_{CCD} I_{CCI} I_{CCT} I_{CCR}	 - - - - - -	 0.2 1.0 35 500 30 37	 1.0 6.0 102 800 35 42	 µA µA µA µA mA mA
Input Current (V_{IN} = 0 V or V_{DDINT}) (All digital inputs)	I_{IN}	-	-	±1	µA
Input Low Voltage (All digital inputs)	V_{IL}	0	-	30% V_{DDINT}	V
Input High Voltage (all digital inputs)	V_{IH}	70% V_{DDINT}	-	V_{DDINT}	V
Output High Voltage (I_{OH} = -1 mA) (All digital outputs)	V_{OH}	80% V_{DDINT}	-	V_{DDINT}	V
Output Low Voltage (I_{OL} = 1 mA) (All digital outputs)	V_{OL}	0	-	20% V_{DDINT}	V

1 To attain specified low power current, all GPIO and other digital IO must be handled properly. See Section 7.2, “Low Power Considerations.

2 CLKO frequency at default value of 32.786 kHz.

6.2.3 Modem AC Electrical Characteristics

NOTE

All AC parameters measured with SPI Registers at default settings except where noted.

Table 9. Receiver AC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, f_{ref} = 16 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% Packet Error Rate (PER) (-40 to +85 °C)	$SENS_{per}$	-	-92	-	dBm
Sensitivity for 1% Packet Error Rate (PER) (+25 °C)		-	-92	-87	dBm
Saturation (maximum input level)	$SENS_{max}$	-	10	-	dBm
Channel Rejection for 1% PER (desired signal -82 dBm) +5 MHz (adjacent channel) -5 MHz (adjacent channel) +10 MHz (alternate channel) -10 MHz (alternate channel) >= 15 MHz	 	 - - - - -	 34 29 44 44 46	 - - - - -	 dB dB dB dB dB

Table 9. Receiver AC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, f_{ref} = 16 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Error Tolerance		-	-	200	kHz
Symbol Rate Error Tolerance		-	-	80	ppm

Table 10. Transmitter AC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, f_{ref} = 16 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Spectral Density (-40 to +85 °C) Absolute limit		-	-47	-	dBm
Power Spectral Density (-40 to +85 °C) Relative limit		-	47	-	
Nominal Output Power[1]	P_{out}	-4	-1	2	dBm
Maximum Output Power[2]			3		dBm
Error Vector Magnitude	EVM	-	18	35	%
Ouput Power Control Range		-	30	-	dB
Over the Air Data Rate		-	250	-	kbps
2nd Harmonic[3]		-	-43	-	dBc
3rd Harmonic[3]		-	-45	-	dBc

1 SPI Register 12 is default value of 0x00BC which sets output power to nominal (-1 dBm typical).

2 SPI Register 12 programmed to 0xFF which sets output power to maximum.

3 Measurements taken at output of evaluation circuit set for maximum power out.

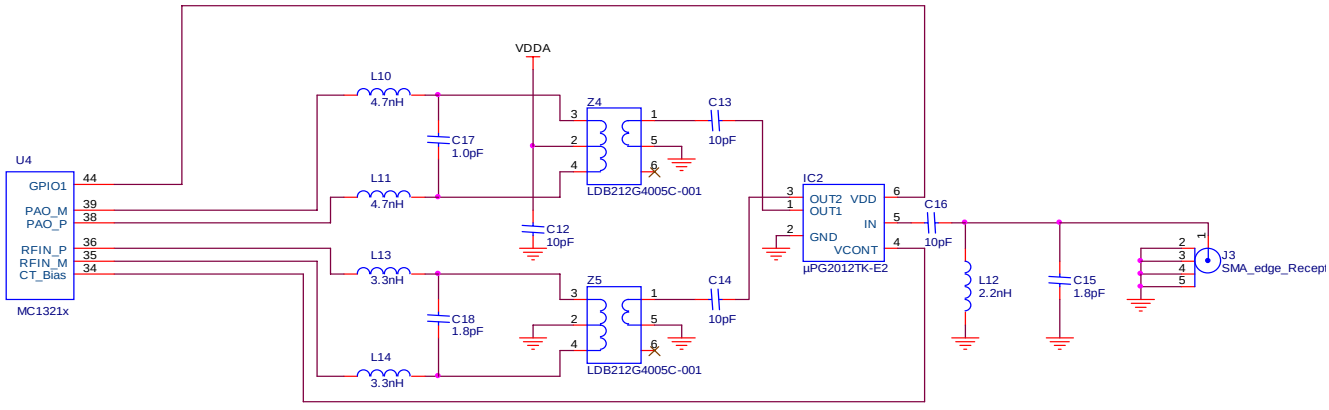


Figure 26. RF Parametric Evaluation Circuit

6.3 MCU Electrical Characteristics

6.3.1 MCU DC Characteristics

Table 11. MCU DC Characteristics
(Temperature Range = –40 to 85°C Ambient)

Parameter	Symbol	Min	Typical[1]	Max	Unit
Supply voltage (run, wait and stop modes.) $0 < f_{Bus} < 8$ MHz $0 < f_{Bus} < 20$ MHz	V_{DD}	 1.8 2.08		 3.6 3.6	V
Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	1.0[2]		—	V
Low-voltage detection threshold — high range (V_{DD} falling) (V_{DD} rising)	V_{LVDH}	 2.08 2.16	 2.1 2.19	 2.2 2.27	V
Low-voltage detection threshold — low range (V_{DD} falling) (V_{DD} rising)	V_{LVDL}	 1.80 1.88	 1.82 1.90	 1.91 1.99	V
Low-voltage warning threshold — high range (V_{DD} falling) (V_{DD} rising)	V_{LVWH}	 2.35 2.35	 2.40 2.40	2.5	V
Low-voltage warning threshold — low range (V_{DD} falling) (V_{DD} rising)	V_{LVWL}	 2.08 2.16	 2.1 2.19	 2.2 2.27	V
Power on reset (POR) re-arm voltage(2) Mode = stop Mode = run and Wait	V_{Rearm}	 0.20 0.50	 0.30 0.80	 0.40 1.2	V
Input high voltage ($V_{DD} > 2.3$ V) (all digital inputs)	V_{IH}	$0.70 \times V_{DD}$		—	V
Input high voltage ($1.8\ V \le V_{DD} \le 2.3$ V) (all digital inputs)	V_{IH}	$0.85 \times V_{DD}$		—	V
Input low voltage ($V_{DD} > 2.3$ V) (all digital inputs)	V_{IL}	—		$0.35 \times V_{DD}$	V
Input low voltage ($1.8\ V \le V_{DD} \le 2.3$ V) (all digital inputs)	V_{IL}	—		$0.30 \times V_{DD}$	V
Input hysteresis (all digital inputs)	V_{hys}	$0.06 \times V_{DD}$		—	V
Input leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS}, all input only pins	$\lvert I_{In} \rvert$	—	0.025	1.0	μA
High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS}, all input/output	$\lvert I_{OZ} \rvert$	—	0.025	1.0	μA
Internal pullup and pulldown resistors[3] (all port pins and IRQ)	R_{PU}	17.5		52.5	kohm
Internal pulldown resistors (Port A4–A7 and IRQ)	R_{PD}	17.5		52.5	kohm

Table 11. MCU DC Characteristics (continued)
(Temperature Range = –40 to 85°C Ambient)

Parameter	Symbol	Min	Typical[1]	Max	Unit
Output high voltage ($V_{DD} \geq 1.8$ V) I_{OH} = –2 mA (ports A, B, D, E, and G)	V_{OH}	V_{DD} – 0.5		—	V
Output high voltage (ports C and F) I_{OH} = –10 mA ($V_{DD} \geq 2.7$ V) I_{OH} = –6 mA ($V_{DD} \geq 2.3$ V) I_{OH} = –3 mA ($V_{DD} \geq 1.8$ V)		V_{DD} – 0.5		— — —	
Maximum total I_{OH} for all port pins	$\lvert I_{OHT} \rvert$	—		60	mA
Output low voltage ($V_{DD} \geq 1.8$ V) I_{OL} = 2.0 mA (ports A, B, D, E, and G)	V_{OL}	—		0.5	V
Output low voltage (ports C and F) I_{OL} = 10.0 mA ($V_{DD} \geq 2.7$ V) I_{OL} = 6 mA ($V_{DD} \geq 2.3$ V) I_{OL} = 3 mA ($V_{DD} \geq 1.8$ V)		— — —		0.5 0.5 0.5	
Maximum total I_{OL} for all port pins	I_{OLT}	—		60	mA
dc injection current[4, 5, 6, 7, 8] $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins	$\lvert I_{IC} \rvert$	 — —		 0.2 5	 mA mA
Input capacitance (all non-supply pins)(2)	C_{In}	—		7	pF

1 Typicals are measured at 25°C.

2 This parameter is characterized and not tested on each device.

3 Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

4 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 This parameter is characterized and not tested on each device.

8 IRQ does not have a clamp diode to V_{DD}. Do not drive IRQ above V_{DD}.

6.3.2 MCU Supply Current Characteristics

Table 12. MCU Supply Current Characteristics
(Temperature Range = –40 to 85°C Ambient)

Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Temp. (°C)
Run supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	RI_{DD}	3	1.1 mA	2.1 mA(4) 2.1 mA(4) 2.1 mA(4)	55 70 85
		2	0.8 mA	1.8 mA(4) 1.8 mA(4) 1.8 mA(4)	55 70 85
Run supply current (3) measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)	RI_{DD}	3	6.5 mA	7.5 mA(4) 7.5 mA(4) 7.5 mA(5)	55 70 85
		2	4.8 mA	5.8 mA(4) 5.8 mA(4) 5.8 mA(4)	55 70 85
Stop1 mode supply current	$S1I_{DD}$	3	25 nA	0.6 μA(4) 1.8 μA(4) 4.0 μA(5)	55 70 85
		2	20 nA	500 nA(4) 1.5 μA(4) 3.3 μA(4)	55 70 85
Stop2 mode supply current	$S2I_{DD}$	3	550 nA	3.0 μA(4) 5.5 μA(4) 11 μA(5)	55 70 85
		2	400 nA	2.4 μA(4) 5.0 μA(4) 9.5 μA(4)	55 70 85
Stop3 mode supply current	$S3I_{DD}$	3	675 nA	4.3 μA(4) 7.2 μA(4) 17.0 μA(5)	55 70 85
		2	500 nA	3.5 μA(4) 6.2 μA(4) 15.0 μA(4)	55 70 85
RTI adder to Stop2 or Stop3[6]		3	300 nA		55 70 85
		2	300 nA		55 70 85

Table 12. MCU Supply Current Characteristics (continued)
(Temperature Range = –40 to 85°C Ambient)

Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Temp. (°C)
LVI adder to Stop3 (LVDSE = LVDE = 1)		3	70 μA		55 70 85
		2	60 μA		55 70 85
Adder to Stop3 for oscillator enabled[7] (OSCSTEN = 1)		3	5 μA		55 70 85
		2	5 μA		55 70 85
Adder for loss-of-clock enabled		3	9 μA		55 70 85

1 Typicals are measured at 25°C.

2 Values given here are preliminary estimates prior to completing characterization.

3 All modules except ATD active, ICG configured for FBE, and does not include any dc loads on port pins

4 Values are characterized but not tested on every part.

5 Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

6 Most customers are expected to find that auto-wakeup from Stop2 or Stop3 can be used instead of the higher current wait mode. Wait mode typical is 560 μA at 3 V and 422 μA at 2V with f_{Bus} = 1 MHz.

7 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0), clock monitordisabled (LOCD = 1)

6.3.3 MCU ATD Characteristics

Table 13. MCU ATD Electrical Characteristics (Operating)

Num	Characteristic	Condition	Symbol	Min	Typical	Max	Unit
1	ATD supply[1]		V_{DDAD}	1.80	—	3.6	V
2	ATD supply current	Enabled	$I_{DDADrun}$	—	0.7	1.2	mA
		Disabled (ATDPU = 0 or STOP)	$I_{DDADstop}$	—	0.02	0.6	μA
3	Differential supply voltage	V_{DD}–V_{DDAD}	$\|V_{DDLT}\|$	—	—	100	mV
4	Differential ground voltage	V_{SS}–V_{SSAD}	$\|V_{SDLT}$	—	—	100	mV
5	Reference potential, low		$\|V_{REFL}\|$	—	—	V_{SSAD}	V
	Reference potential, high	$2.08V \leq V_{DDAD} \leq 3.6V$	V_{REFH}	2.08	—	V_{DDAD}	V
		$1.80V \leq V_{DDAD} < 2.08V$		V_{DDAD}	—	V_{DDAD}	
6	Reference supply current (V_{REFH} to V_{REFL})	Enabled	I_{REF}	—	200	300	μA
		Disabled (ATDPU = 0 or STOP)	I_{REF}	—	<0.01	0.02	
7	Analog input voltage[2]		V_{INDC}	V_{SSAD} – 0.3	—	V_{DDAD} + 0.3	V

[1] V_{DDAD} must be at same potential as V_{DD}.

[2] Maximum electrical operating range, not valid conversion range.

Table 14. ATD Timing/Performance Characteristics[1]

Num	Characteristic	Symbol	Condition	Min	Typ	Max	Unit
1	ATD conversion clock frequency	f_{ATDCLK}	$2.08V \le V_{DDAD} \le 3.6V$	0.5	—	2.0	MHz
			$1.80V \le V_{DDAD} < 2.08V$	0.5	—	1.0	
2	Conversion cycles (continuous convert)[2]	CCP		28	28	<30	ATDCLK cycles
3	Conversion time	T_{conv}	$2.08V \le V_{DDAD} \le 3.6V$	14.0	—	60.0	μS
			$1.80V \le V_{DDAD} < 2.08V$	28.0	—	60.0	
4	Source impedance at input[3]	R_{AS}		—	—	10	kΩ
5	Analog Input Voltage[4]	V_{AIN}		V_{REFL}		V_{REFH}	V
6	Ideal resolution (1 LSB)[5]	RES	$2.08V \le V_{DDAD} \le 3.6V$	2.031	—	3.516	mV
			$1.80V \le V_{DDAD} < 2.08V$	1.758	—	2.031	
7	Differential non-linearity[6]	DNL	$1.80V \le V_{DDAD} \le 3.6V$	—	$\pm$0.5	$\pm$1.0	LSB
8	Integral non-linearity[7]	INL	$1.80\ V \le V_{DDAD} \le 3.6V$	—	$\pm$0.5	$\pm$1.0	LSB
9	Zero-scale error[8]	E_{ZS}	$1.80V \le V_{DDAD} \le 3.6V$	—	$\pm$0.4	$\pm$1.0	LSB
10	Full-scale error[9]	E_{FS}	$1.80V \le V_{DDAD} \le 3.6V$	—	$\pm$0.4	$\pm$1.0	LSB
11	Input leakage error [10]	E_{IL}	$1.80V \le V_{DDAD} \le 3.6V$	—	$\pm$0.05	$\pm$5	LSB
12	Total unadjusted error[11]	E_{TU}	$1.80V \le V_{DDAD} \le 3.6V$	—	$\pm$1.1	$\pm$2.5	LSB

1 All ACCURACY numbers are based on processor and system being in WAIT state (very little activity and no IO switching) and that adequate low-pass filtering is present on analog input pins (filter with 0.01 μF to 0.1 μF capacitor between analog input and V_{REFL}). Failure to observe these guidelines may result in system or microcontroller noise causing accuracy errors which will vary based on board layout and the type and magnitude of the activity.

2 This is the conversion time for subsequent conversions in continuous convert mode. Actual conversion time for single conversions or the first conversion in continuous mode is extended by one ATD clock cycle and 2 bus cycles due to starting the conversion and setting the CCF flag. The total conversion time in Bus Cycles for a conversion is:

SC Bus Cycles = ((PRS+1)*2) * (28+1) + 2 CC Bus Cycles = ((PRS+1)*2) * (28)

3 R_{AS} is the real portion of the impedance of the network driving the analog input pin. Values greater than this amount may not fully charge the input circuitry of the ATD resulting in accuracy error.

4 Analog input must be between V_{REFL} and V_{REFH} for valid conversion. Values greater than V_{REFH} will convert to $3FF less the full scale error (E_{FS}).

5 The resolution is the ideal step size or 1LSB = $(V_{REFH}–V_{REFL})/1024$

6 Differential non-linearity is the difference between the current code width and the ideal code width (1LSB). The current code width is the difference in the transition voltages to and from the current code.

7 Integral non-linearity is the difference between the transition voltage to the current code and the adjusted ideal transition voltage for the current code. The adjusted ideal transition voltage is $(Current\ Code–1/2)*(1/((V_{REFH}+E_{FS})–(V_{REFL}+E_{ZS})))$.

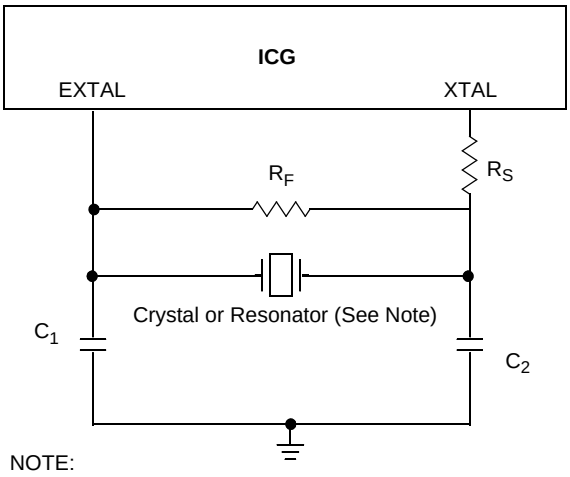
8 Zero-scale error is the difference between the transition to the first valid code and the ideal transition to that code. The Ideal transition voltage to a given code is $(Code–1/2)*(1/(V_{REFH}–V_{REFL}))$.

9 Full-scale error is the difference between the transition to the last valid code and the ideal transition to that code. The ideal transition voltage to a given code is $(Code–1/2)*(1/(V_{REFH}–V_{REFL}))$.

10 Input leakage error is error due to input leakage across the real portion of the impedance of the network driving the analog pin. Reducing the impedance of the network reduces this error.

[11] Total unadjusted error is the difference between the transition voltage to the current code and the ideal straight-line transfer function. This measure of error includes inherent quantization error (1/2LSB) and circuit error (differential, integral, zero-scale, and full-scale) error. The specified value of E_T assumes zero E_{IL} (no leakage or zero real source impedance).

6.3.4 MCU Internal Clock Generation Module Characteristics



NOTE:
Use fundamental mode crystal or ceramic resonator only.

Figure 27. ICG Clock Basic Schematic

Table 15. MCU ICG DC Electrical Specifications (Temperature Range = –40 to 85°C Ambient)

Characteristic	Symbol	Min	Typ[1]	Max	Unit
Load capacitors	C_1 C_2		[2]		
Feedback resistor Low range (32k to 100 kHz) High range (1M – 16 MHz)	R_F		 10 1		 MΩ MW
Series Resistor	R_S		0		Ω

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

[2] See crystal or resonator manufacturer's recommendation.

6.3.5 MCU ICG Frequency Specifications

Table 16. MCU ICG Frequency Specifications
(V_{DDA} = V_{DDA} (min) to V_{DDA} (max), Temperature Range = –40 to 85°C Ambient)

Characteristic	Symbol	Min	Typical	Max	Unit
Oscillator crystal or resonator (REFS = 1) (Fundamental mode crystal or ceramic resonator) Low range High range , FLL bypassed external (CLKS = 10) High range , FLL engaged external (CLKS = 11)	 f_{lo} f_{hi_byp} f_{hi_eng}	 32 2 2	 — — —	 100 16 10	 kHz MHz MHz
Input clock frequency (CLKS = 11, REFS = 0) Low range High range	 f_{lo} f_{hi_eng}	 32 2	 — —	 100 10	 kHz MHz
Input clock frequency (CLKS = 10, REFS = 0)	f_{Extal}	0	—	40	MHz
Internal reference frequency (untrimmed)	$f_{ICGIRCLK}$	182.25	243	303.75	kHz
Duty cycle of input clock [4] (REFS = 0)	t_{dc}	40	—	60	%
Output clock ICGOUT frequency CLKS = 10, REFS = 0 All other cases	f_{ICGOUT}	 f_{Extal} (min) f_{lo} (min)		 f_{Extal} (max) $f_{ICGDCLKmax}$(max)	MHz
Minimum DCO clock (ICGDCLK) frequency	$f_{ICGDCLKmin}$	8	—		MHz
Maximum DCO clock (ICGDCLK) frequency	$f_{ICGDCLKmax}$		—	40	MHz
Self-clock mode (ICGOUT) frequency [1]	f_{Self}	$f_{ICGDCLKmin}$		$f_{ICGDCLKmax}$	MHz
Self-clock mode reset (ICGOUT) frequency	f_{Self_reset}	5.5	8	10.5	MHz
Loss of reference frequency [2] Low range High range	f_{LOR}	 5 50		 25 500	kHz
Loss of DCO frequency [3]	f_{LOD}	 0.5		 1.5	MHz
Crystal start-up time [4, 5] Low range High range	 t_{CSTL} t_{CSTH}	 — —	 430 4	 — —	 ms
FLL lock time [4, 6] Low range High range	 t_{Lockl} t_{Lockh}	 — —		 2 2	ms
FLL frequency unlock range	n_{Unlock}	–4*N		4*N	counts
FLL frequency lock range	n_{Lock}	–2*N		2*N	counts

Table 16. MCU ICG Frequency Specifications (continued)
(V_{DDA} = V_{DDA} (min) to V_{DDA} (max), Temperature Range = –40 to 85°C Ambient)

Characteristic	Symbol	Min	Typical	Max	Unit
ICGOUT period jitter, [4, 7] measured at f_{ICGOUT} Max Long term jitter (averaged over 2 ms interval)	C_{Jitter}	 —		 0.2	% f_{ICG}
Internal oscillator deviation from trimmed frequency V_{DD} = 1.8 – 3.6 V, (constant temperature) V_{DD} = 3.0 V ±10%, –40° C to 85° C	ACC_{int}	 — —	 ±0.5 ±0.5	 ±2 ±2	%

1 Self-clocked mode frequency is the frequency that the DCO generates when the FLL is open-loop.

2 Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.

3 Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.

4 This parameter is characterized before qualification rather than 100% tested.

5 Proper PC board layout procedures must be followed to achieve specifications.

6 This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{ICGOUT}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDA} and V_{SSA} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

6.4 MCU AC Peripheral Characteristics

This section describes ac timing characteristics for each peripheral system.

6.4.1 MCU Control Timing

Table 17. MCU Control Timing

Parameter	Symbol	Min	Typical	Max	Unit
Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
Real-time interrupt internal oscillator period	t_{RTI}	700		1300	µs
External reset pulse width[1]	t_{extrst}	1.5 x f_{Self_reset}		—	ns
Reset low drive[2]	t_{rstdrv}	34 x f_{Self_reset}		—	ns
Active background debug mode latch setup time	t_{MSSU}	25		—	ns
Active background debug mode latch hold time	t_{MSH}	25		—	ns
IRQ pulse width[3]	t_{ILIH}	1.5 x t_{cyc}		—	ns
Port rise and fall time (load = 50 pF)[4] Slew rate control disabled Slew rate control enabled	t_{Rise}, t_{Fall}	 — —	 3 30		ns

1 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

2 When any reset is initiated, internal circuitry drives the reset pin low for about 34 cycles of f_{Self_reset} and then samples the level on the reset pin about 38 cycles later to distinguish external reset requests from internal requests.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

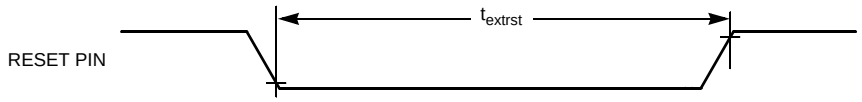


Figure 28. Control Reset Timing

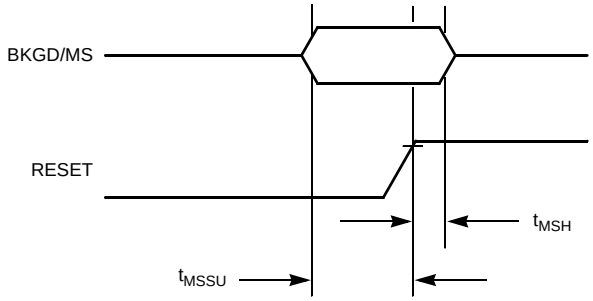


Figure 29. Control Active Background Debug Mode Latch Timing

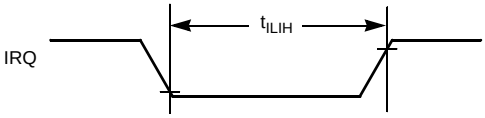


Figure 30. Control IRQ Timing

6.4.2 MCU Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM Input Timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
External clock period	t_{TPMext}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

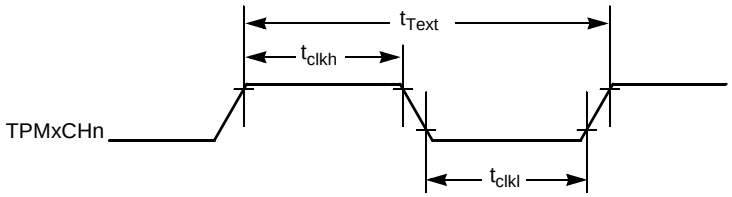


Figure 31. Timer External Clock

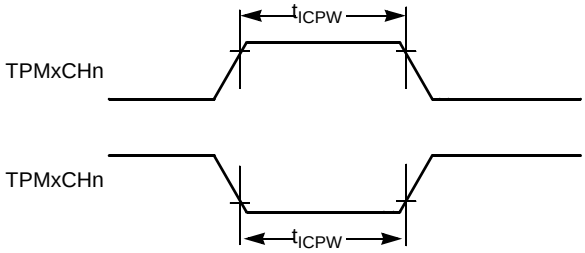


Figure 32. Timer Input Capture Pulse

6.4.3 System SPI Timing

Table 19 describes the timing requirements for the SPI system.

Table 19. SPI Timing

No.	Function	Symbol	Min	Max	Unit
	Operating frequency Master	f_{op}	$f_{Bus}/2048$	$f_{Bus}/2$ = 8 MHz	Hz
1	SCK period Master	t_{SCK}	2	2048	t_{cyc}
2	Enable lead time Master	t_{Lead}	1/2	—	t_{SCK}
3	Enable lag time Master	t_{Lag}	1/2	—	t_{SCK}
4	Clock (SCK) high or low time Master	t_{WSCK}	62.5	1024 t_{cyc}	ns
5	Data setup time (inputs) Master	t_{SU}	15	—	ns
6	Data hold time (inputs) Master	t_{HI}	0	—	ns
7	Data valid (after SCK edge) Master	t_{v}	—	25	ns
8	Data hold time (outputs) Master	t_{HO}	0	—	ns
9	Rise time Input Output	 t_{RI} t_{RO}	 — —	 t_{cyc} – 25 25	 ns ns
10	Fall time Input Output	 t_{FI} t_{FO}	 — —	 t_{cyc} – 25 25	 ns ns

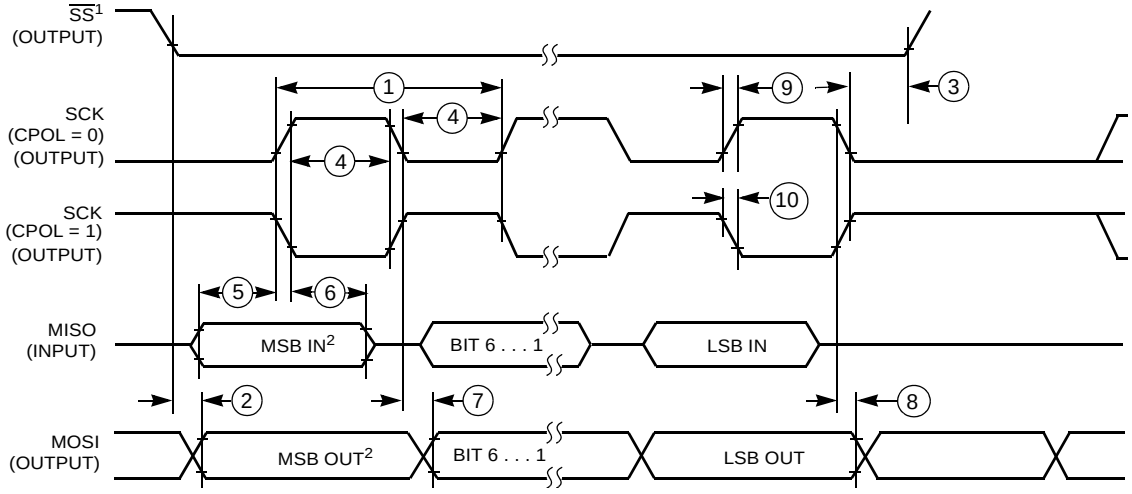


Figure 33. SPI Master Timing (CPHA = 0)

6.4.4 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the FLASH memory. Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 20. FLASH Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage for program/erase	$V_{prog/erase}$	2.1		3.6	V
Supply voltage for read operation $0 < f_{Bus} < 8$ MHz $0 < f_{Bus} < 20$ MHz	V_{Read}	 1.8 2.08		 3.6 3.6	V
Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
Page erase time[2]	t_{Page}	4000			t_{Fcyc}
Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
Program/erase endurance[3] T_L to T_H = –40°C to + 85°C T = 25°C		10,000	 100,000	 —	cycles
Data retention[4]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for FLASH** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Non-volatile Memory.*

7 Application Considerations

The following sections describe crystal requirements and RF port options for end user applications.

7.1 Crystal Oscillator Reference Frequency

The 802.15.4 Standard requires that several frequency tolerances be kept within ± 40 ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will still result in acceptable performance. The MC1321x transceiver provides onboard crystal trim capacitors to assist in meeting this performance. The primary determining factor in meeting the 802.15.4 Standard, is the tolerance of the crystal oscillator reference frequency. A number of factors can contribute to this tolerance and a crystal specification will quantify each of them:

1. The initial (or make) tolerance of the crystal resonant frequency itself.
2. The variation of the crystal resonant frequency with temperature.
3. The variation of the crystal resonant frequency with time, also commonly known as aging.
4. The variation of the crystal resonant frequency with load capacitance, also commonly known as pulling. This is affected by:
   a) The external load capacitor values - initial tolerance and variation with temperature.
   b) The internal trim capacitor values - initial tolerance and variation with temperature.
   c) Stray capacitance on the crystal pin nodes - including stray on-chip capacitance, stray package capacitance and stray board capacitance; and its initial tolerance and variation with temperature.
5. Whether or not a frequency trim step will be performed in production

7.1.1 Crystal Oscillator Design Considerations

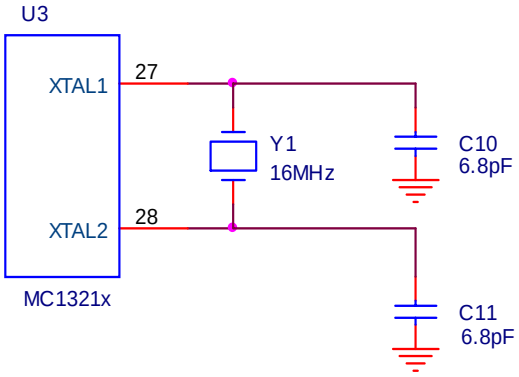
Freescale requires that a 16 MHz crystal with a <9 pF load capacitance is used. The MC1321x does not contain a reference divider, so 16 MHz is the only frequency that can be used. A crystal requiring higher load capacitance is prohibited because a higher load on the amplifier circuit may compromise its performance. The crystal manufacturer defines the load capacitance as that total external capacitance seen across the two terminals of the crystal. The oscillator amplifier configuration used in the MC1321x requires two balanced load capacitors from each terminal of the crystal to ground. As such, the capacitors are seen to be in series by the crystal, so each must be <18 pF for proper loading.

In the Figure 34 crystal reference schematic, the external load capacitors are shown as 6.8 pF each, used in conjunction with a crystal that requires an 8 pF load capacitance. The default internal trim capacitor value (2.4 pF) and stray capacitance total value (6.8 pF) sum up to 9.2 pF giving a total of 16 pF. The value for the stray capacitance was determined empirically assuming the default internal trim capacitor value and for a specific board layout. A different board layout may require a different external load capacitor value. The on-chip trim capability may be used to determine the closest standard value by adjusting the trim value via the SPI and observing the frequency at CLKO. Each internal trim load capacitor has a trim range of approximately 5 pF in 20 fF steps.

Initial tolerance for the internal trim capacitance is approximately ±15%.

Since the MC1321x contains an on-chip reference frequency trim capability, it is possible to trim out virtually all of the initial tolerance factors and put the frequency within 0.12 ppm on a board-by-board basis. Individual trimming of each board in a production environment allows use of the lowest cost crystal, but requires that each board go through a trimming procedure. This step can be avoided by using/specifying a crystal with a tighter stability tolerance, but the crystal will be slightly higher in cost.

A tolerance analysis budget may be created using all the previously stated factors. It is an engineering judgment whether the worst case tolerance will assume that all factors will vary in the same direction or if the various factors can be statistically rationalized using RSS (Root-Sum-Square) analysis. The aging factor is usually specified in ppm/year and the product designer can determine how many years are to be assumed for the product lifetime. Taking all of the factors into account, the product designer can determine the needed specifications for the crystal and external load capacitors to meet the 802.15.4 Standard.



Y1 = Daishinku KDS - DSX321G ZD00882

Figure 34. MC1321x Modem Crystal Circuit

7.1.2 Crystal Requirements

The suggested crystal specification for the MC1321x is shown in Table 21. A number of the stated parameters are related to desired package, desired temperature range and use of crystal capacitive load trimming. For more design details and suggested crystals, see application note *AN3251, Reference Oscillator Crystal Requirements for MC1319x, MC1320x, and MC1321x.*

Table 21. MC1321x Crystal Specifications[1]

Parameter	Value	Unit	Condition
Frequency	16.000000	MHz	
Frequency tolerance (cut tolerance)[2]	± 10	ppm	at 25 °C
Frequency stability (temperature drift)[3]	± 15	ppm	Over desired temperature range
Aging[4]	± 2	ppm	max
Equivalent series resistance[5]	43	Ω	max
Load capacitance[6]	5 - 9	pF	

Table 21. MC1321x Crystal Specifications[1] (continued)

Parameter	Value	Unit	Condition
Shunt capacitance	<2	pF	max
Mode of oscillation			fundamental

1 User must be sure manufacturer specifications apply to the desired package.

2 A wider frequency tolerance may acceptable if application uses trimming at production final test.

3 A wider frequency stability may be acceptable if application uses trimming at production final test.

4 A wider aging tolerance may be acceptable if application uses trimming at production final test.

5 Higher ESR may be acceptable with lower load capacitance.

6 Lower load capacitance can allow higher ESR and is better for low temperature operation in Doze mode.

7.2 Low Power Considerations

- Program and use the modem IO pins properly for low power operation
  - — All unused modem GPIOx signals must be used one of 2 ways:
    - – If the Off mode is to be used as a long term low power mode, unused GPIO should be tied to ground. The default GPIO mode is an input and there will be no conflict.
    - – If only Hibernate and/or Doze modes are used as long term low power modes, the GPIO should programmed as outputs in the low state.
  - — When modem GPIO are used as outputs:
    - – Pullup resistors should be provided (can be provided by the MCU IO pin if tied to the MCU) if the modem Off condition is to be used as a long term low power mode.
    - – During Hibernate and/or Doze modes, the GPIO will retain its programmed output state.
  - — If the modem GPIO is used as an input, the GPIO should be driven by its source during all low power modes or a pullup resistor should be provided.
  - — Digital outputs $\overline{\text{IRQ}}$, MISO, and CLKO:
    - – MISO - is always an output. During Hibernate, Doze, and active modes, the default condition is for the MISO output to go to tristate when $\overline{\text{CE}}$ is de-asserted, and this can cause a problem with the MCU because one of its inputs can float. Program Control_B Register 07, Bit 11, miso_hiz_en = 0 so that MISO is driven low when $\overline{\text{CE}}$ is de-asserted. As a result, MISO will not float when Doze or Hibernate Mode is enabled.
    - – $\overline{\text{IRQ}}$ - is an open drain output (OD) and should always have a pullup resistor (typically provided by the MCU IO). $\overline{\text{IRQ}}$ acts as the interrupt request output.

NOTE

It is good practice to have the $\overline{\text{IRQ}}$ interrupt input to the MCU disabled during the hardware reset to the modem. After releasing the modem hardware reset, the interrupt request input to the MCU can then be enabled to await the $\overline{\text{IRQ}}$ that signifies the modem is ready and in Idle mode; this can prevent a possible extraneous false interrupt request.

    - – CLKO - is always an output. During Hibernate CLKO retains its output state, but does not toggle. During Doze, CLKO may toggle depending on whether it is being used.

- When the MCU is used in low power modes, be sure that all unused IO are programmed properly for low power operation (typically best case is as outputs in the low state). The MC1321x is commonly used with the Freescale MC9S08GT/GB 8-bit devices. For these MCUs:
  - Use only STOP2 and STOP3 modes (not STOP1) with these devices where the GPIO states are retained. The MCU must retain control of the MC1321x IO during low power operation.
  - As stated above all unused GPIO should be programmed as outputs low for lowest power and no floating inputs.
  - The MCU has IO signals that are not pinned-out on the package. These signals must also be initialized (even though they cannot be used) to prevent floating inputs.

7.3 RF Single Port Application with an F Antenna

Figure 35 shows a typical single port RF application topology in which part count is minimized and a printed copper F antenna is used for low cost. Only the RFIN port of the MC1321x is required because the differential port is bi-directional and uses the on-chip T/R switch. Matching to near 50 Ohms is accomplished with L1, L2, L3, and the traces on the PCB. A balun transforms the differential signal to single-ended to interface with the F antenna.

The proper DC bias to the RFIN_x (PAO_x) pins is provided through the balun. The CT_Bias pin provides the proper bias voltage point to the balun depending on operation, that is, CT_Bias is at VDDA voltage for transmit and is at ground for receive. CT_Bias is switched between these two voltages based on the operation. Capacitor C2 provides some high frequency bypass to the dc bias point. The L3/C1 network provides a simple bandpass filter to limit out-of-band harmonics from the transmitter.

NOTE

Passive component values can vary as a function of circuit board layout as required to obtain best matching and RF performance.

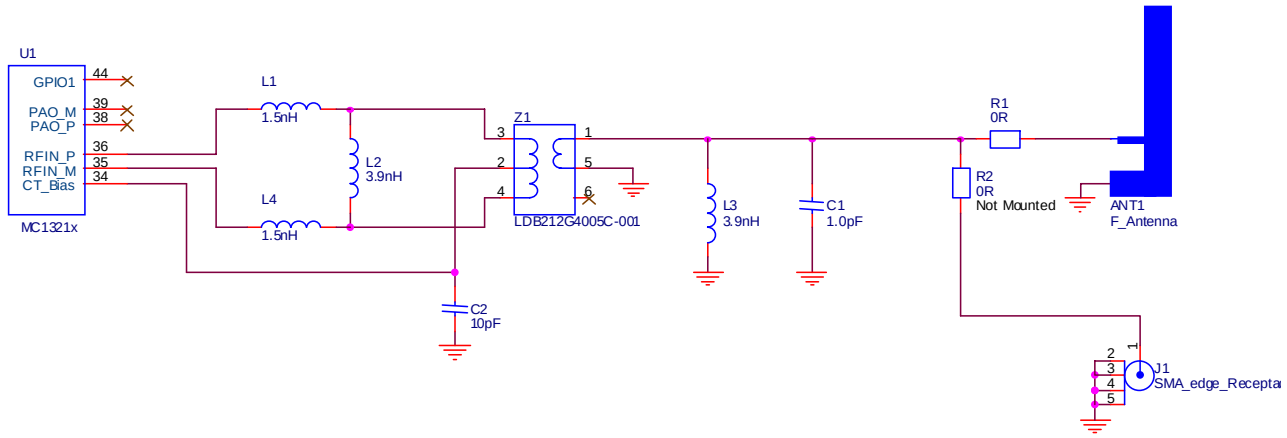


Figure 35. RF Single Port Application with an F-Antenna

7.4 RF Dual Port Application with an F-Antenna

Figure 36 shows a typical dual port application topology which also uses a printed copper F antenna. Both the RFIN and PAO ports are used and the internal T/R switch is bypassed. Matching is provided for both differential ports by L5, L6, L7, and L9 and C4 and C7. A balun is used for both receive and transmit paths which are provided by the external T/R switch, IC1. This implementation, while more complicated, gives better performance due to the reduced loss of the external T/R switch and the more optimum match provided to the PAO and RFIN ports.

The switch control is connected to the CT_Bias pin which serves as its control signal. The CT_Bias signal can be programmed to be active high or active low (depending on TX versus RX) and will switch appropriately based on the radio operation. No interaction with the MCU on an operation-by-operation basis is required.

NOTE

Passive component values can vary as a function of circuit board layout as required to obtain best matching and RF performance.

The VDD voltage to the antenna switch is connected to GPIO1. This is a useful feature when GPIO1 is programmed as an “Out of Idle” status indicator. When the radio is out of Idle (or active), the antenna switch is powered. In this manner, the antenna switch only consumes current when it needs to be active. The GPIO1 can only be used as a VDD source for a very low current load.

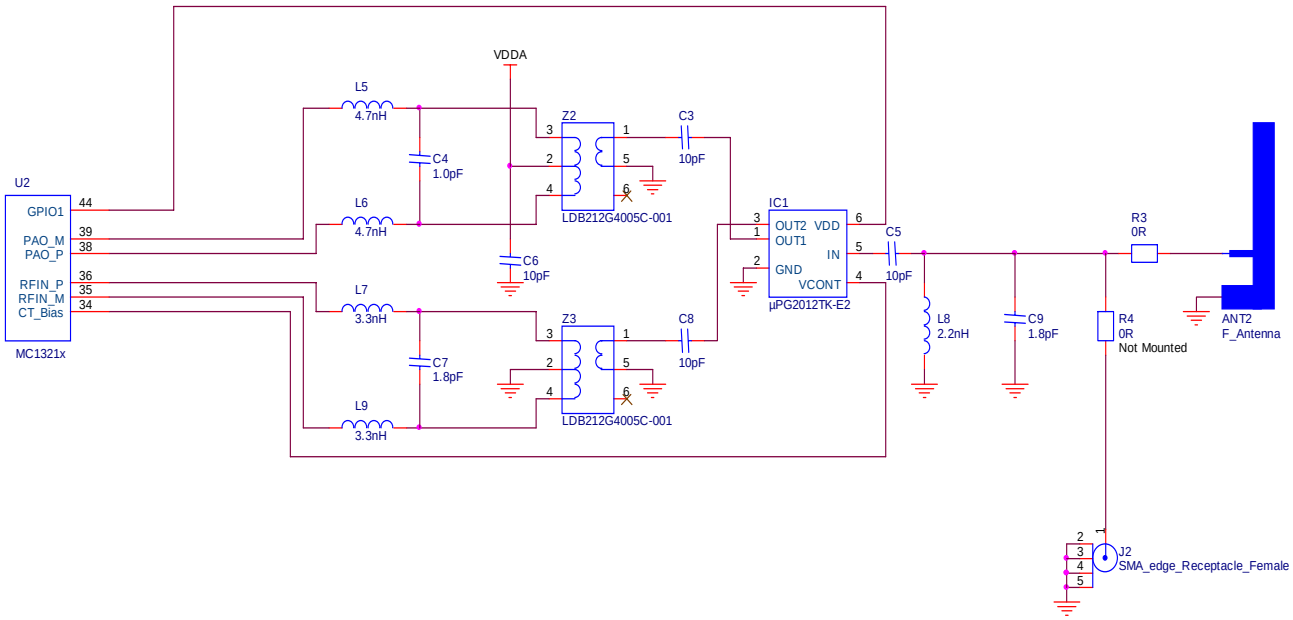


Figure 36. RF Dual Port Application with an F-Antenna

8 Mechanical Diagrams

Figure 37 and Figure 38 show the MC1321x mechanical information.

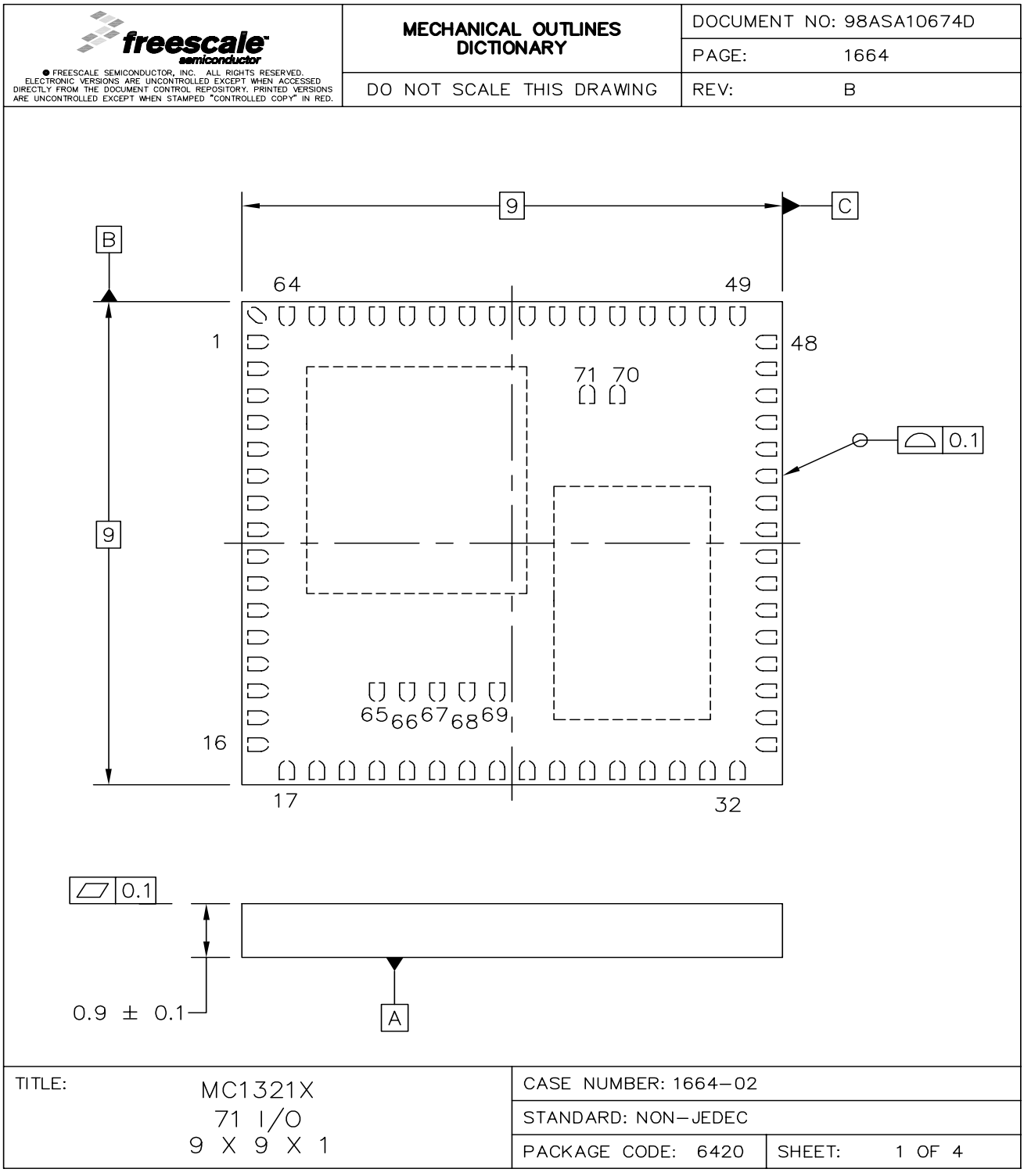
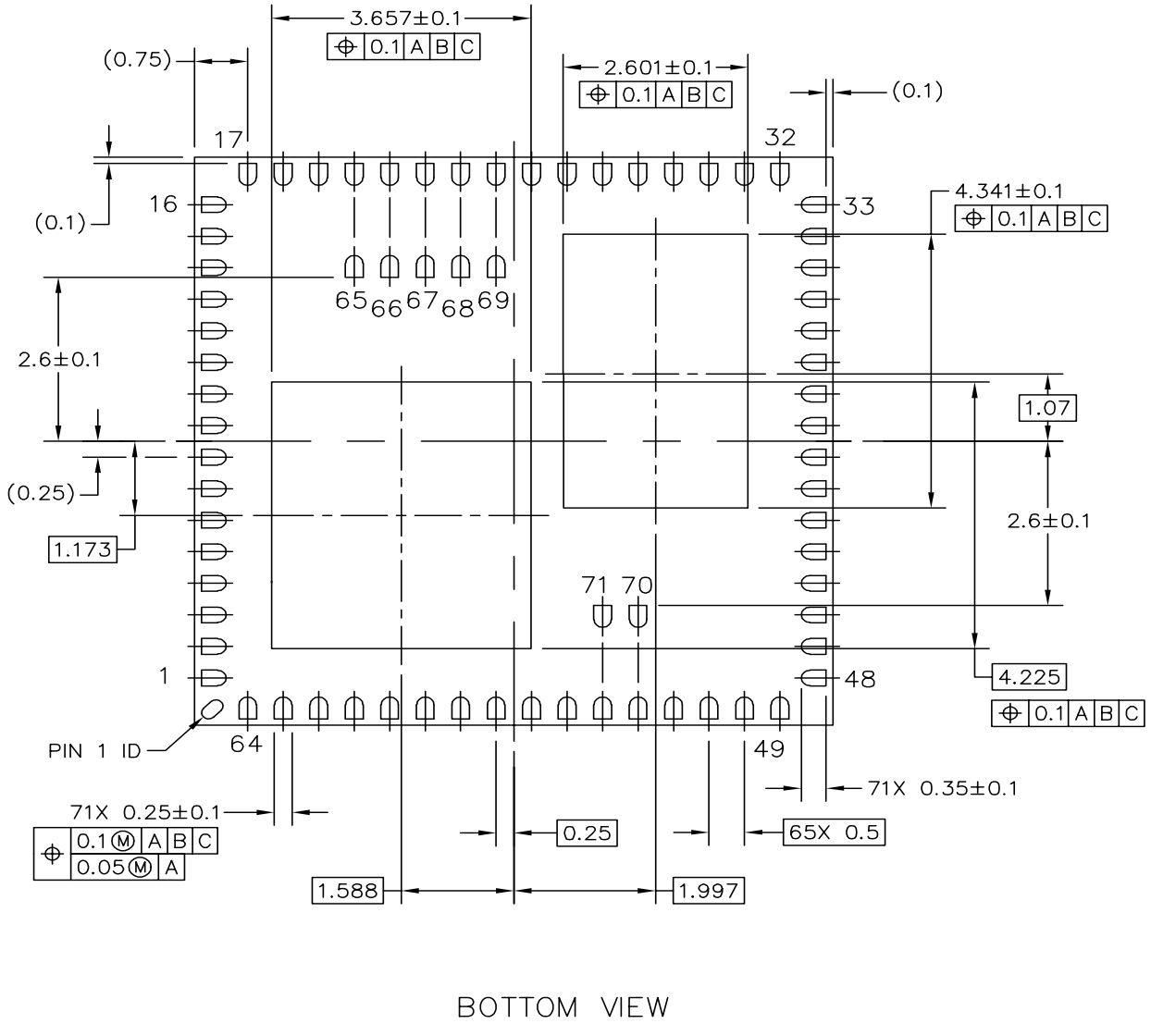


Figure 37. MC1321x Mechanical (1 of 2)

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA10674D
	PAGE: 1664
DO NOT SCALE THIS DRAWING	REV: B



TITLE: MC1321X 71 I/O 9 X 9 X 1	CASE NUMBER: 1664–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 6420	SHEET: 2

Figure 38. MC1321x Mechanical (2 of 2)

NOTES

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
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