AK4396

Advanced Multi-Bit 192kHz 24-Bit ΔΣ DAC

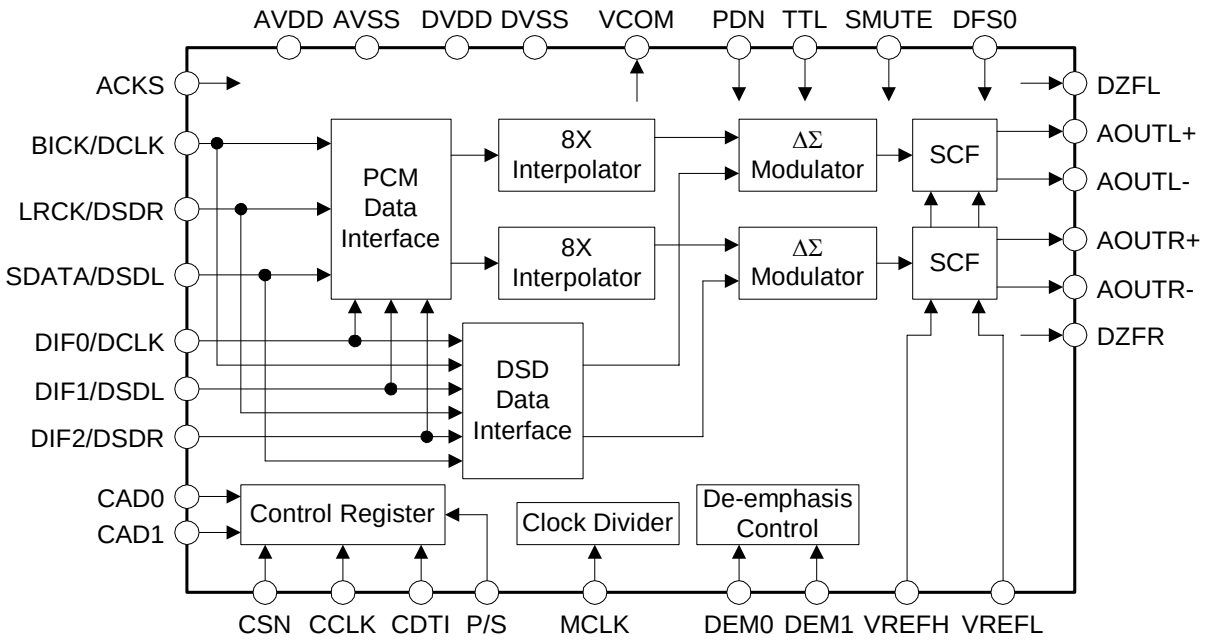
GENERAL DESCRIPTION

The AK4396 is a high performance stereo DAC for the 192kHz sampling mode of DVD-Audio including a 24bit digital filter. Using AKM's multi bit architecture for its modulator the AK4396 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4396 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4396 accepts 192kHz PCM data and 1-bit DSD data, ideal for a wide range of applications including DVD-Audio and SACD. The AK4396 has a fully functional compatibility with the AK4393/4/5 and lower power dissipation.

FEATURES

- **128x Oversampling**
- **Sampling Rate: 30kHz ~ 216kHz**
- **24Bit 8x Digital Filter (Slow-roll-off option)**
  Ripple: ±0.005dB, Attenuation: 75dB
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **DSD data input available**
- **Digital de-emphasis for 32, 44.1, 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (Linear 256 steps)**
- **THD+N: –100dB**
- **DR, S/N: 120dB**
- **I/F format : MSB justified, 16/20/24bit LSB justified, I^2S**
- **Master Clock: Normal Speed: 256fs, 384fs, 512fs, 768fs or 1152fs**
  Double Speed: 128fs, 192fs, 256fs or 384fs
  Quad Speed: 128fs or 192fs
  DSD: 512fs or 768fs
- **Power Supply: 5V ± 5% (Analog), 3.0 ~ 5.25V (Digital)**
- **CMOS or TTL Level Digital I/F**
- **Package: 28pin VSOP**
- **Pin Compatible with AK4393/4/5**

■ Block Diagram

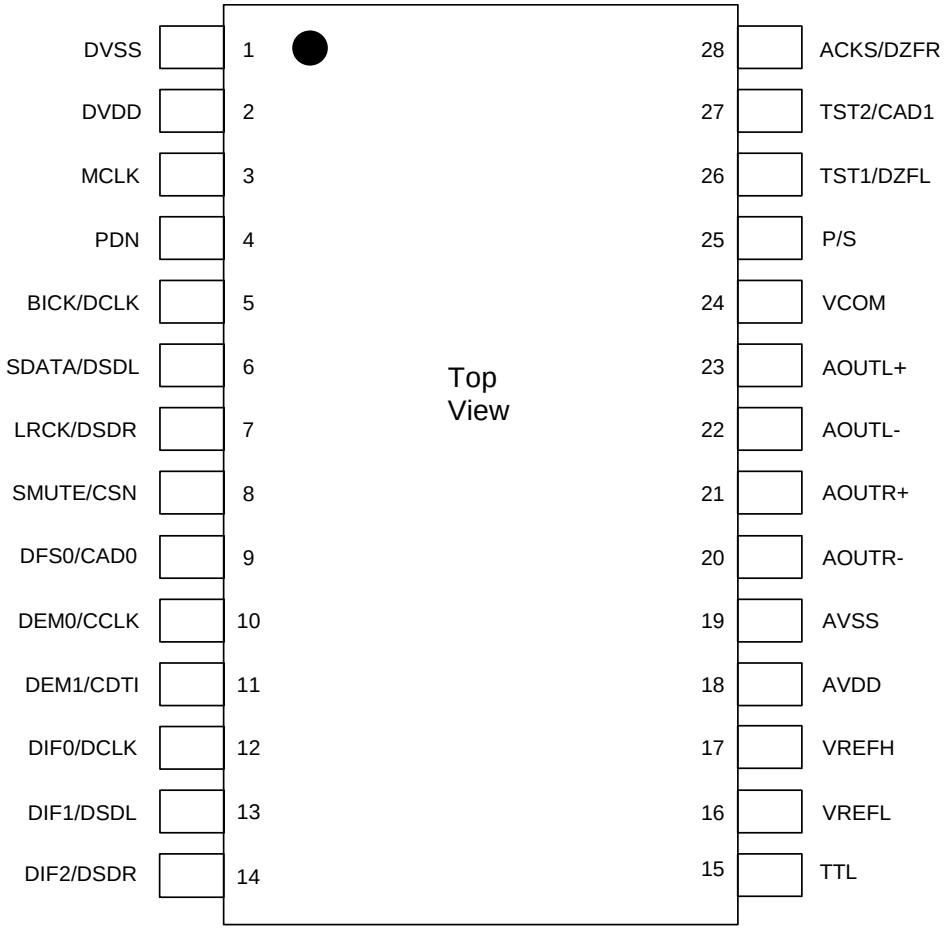


Block Diagram

■ Ordering Guide

AK4396VF	–40 ~ +85°C	28pin VSOP (0.65mm pitch)
AKD4396	Evaluation Board for AK4396	

■ Pin Layout



■ Compatibility with AK4393/4/5

1. Function & Performance

	AK4393	AK4394	AK4395	AK4396
fs (max)	108kHz	216kHz	216kHz	216kHz
DVDD	3~5.25V	4.75~5.25V	4.75~5.25V	3~5.25V
Power Dissipation	310mW	325mW	335mW	200mW
Digital Input Level	CMOS	TTL	TTL	CMOS/TTL
DF Stopband Attenuation	75dB	75dB	110dB	75dB
Digital Volume	Not available	Not available	256 levels, 0.5dB	256 levels, Linear
μP I/F Address Pin	Not available	Not available	CAD0/1	CAD0/1
De-emphasis Filter	32k, 44.1k, 48k, 96k	32k, 44.1k, 48k, 96k	32k, 44.1k, 48k	32k, 44.1k, 48k
Optional DF	Not available	Slow Roll-off	Slow Roll-off	Slow Roll-off
Zero Detection Pin	Not available	DZFL/R	DZFL/R	DZFL/R
DSD Mode	No	No	No	Yes
Pin #15	BVSS	BVSS	BVSS	TTL
Pin #26 (Serial mode)	CKS0	DZFL	DZFL	DZFL
Pin #28 (Serial mode)	CKS2	DZFR	DZFR	DZFR

2. Pin Configuration

Pin#	AK4393	AK4394	AK4395	AK4396
1	DVSS	DVSS	DVSS	DVSS
2	DVDD	DVDD	DVDD	DVDD
3	MCLK	MCLK	MCLK	MCLK
4	PDN	PDN	PDN	PDN
5	BICK	BICK	BICK	BICK
6	SDATA	SDATA	SDATA	SDATA
7	LRCK	LRCK	LRCK	LRCK
8	SMUTE/CSN	SMUTE/CSN	SMUTE/CSN	SMUTE/CSN
9	DFS0	DFS0	DFS0/CAD0	DFS0/CAD0
10	DEM0/CCLK	DEM0/CCLK	DEM0/CCLK	DEM0/CCLK
11	DEM1/CDTI	DEM1/CDTI	DEM1/CDTI	DEM1/CDTI
12	DIF0	DIF0	DIF0	DIF0
13	DIF1	DIF1	DIF1	DIF1
14	DIF2	DIF2	DIF2	DIF2
15	BVSS	BVSS	BVSS	TTL
16	VREFL	VREFL	VREFL	VREFL
17	VFEFH	VFEFH	VFEFH	VFEFH
18	AVDD	AVDD	AVDD	AVDD
19	AVSS	AVSS	AVSS	AVSS
20	AOUTR-	AOUTR-	AOUTR-	AOUTR-
21	AOUTR+	AOUTR+	AOUTR+	AOUTR+
22	AOUTL-	AOUTL-	AOUTL-	AOUTL-
23	AOUTL+	AOUTL+	AOUTL+	AOUTL+
24	VCOM	VCOM	VCOM	VCOM
25	P/S	P/S	P/S	P/S
26	CKS0	CKS0/DZFL	CKS0/DZFL	TST1/DZFL
27	CKS1	CKS1	CKS1/CAD1	TST2/CAD1
28	CKS2	CKS2/DZFR	ACKS/DZFR	ACKS/DZFR

TST1-2: Don't care at parallel mode.

3. Compatibility of master clock select in parallel mode

AK4393/4/5					AK4396		
CKS2	CKS1	CKS0	DFS0=0	DFS0=1	ACKS	DFS0=0	DFS0=1
0	0	0	256fs	128fs	0	256fs	128fs
0	0	1	256fs	256fs	0	256fs	256fs
0	1	0	384fs	192fs	0	384fs	192fs
0	1	1	384fs	384fs	0	384fs	384fs
1	0	0	512fs	256fs	1	512fs	256fs
1	0	1	512fs	N/A	1	512fs	N/A
1	1	0	768fs	384fs	1	768fs	384fs
1	1	1	768fs	N/A	1	768fs	N/A

: The setting of DFS0 is ignored.

4. Register map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	***DIF1***	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	***DEM0***	SMUTE
02H	Control 3	D/P	DSDM	DCKS	DCKB	0	DZFB	0	0
03H	Lch ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

: Changing points from AK4393's register.
Italic means the default value differs from AK4393.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	***DIF1***	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	***DEM0***	SMUTE
02H	Control 3	D/P	DSDM	DCKS	DCKB	0	DZFB	0	0
03H	Lch ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

: Changing points from AK4394's register.
Italic means the default value differs from AK4394.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	***ACKS***	0	0	0	DIF2	***DIF1***	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	D/P	DSDM	DCKS	DCKB	0	DZFB	0	0
03H	Lch ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

: Changing points from AK4395's register.
Italic means the default value differs from AK4395.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVSS	-	Digital Ground Pin
2	DVDD	-	Digital Power Supply Pin, 3.3V or 5.0V
3	MCLK	I	Master Clock Input Pin
4	PDN	I	Power-Down Mode Pin When at "L", the AK4396 is in power-down mode and is held in reset. The AK4396 should always be reset upon power-up.
5	BICK	I	Audio Serial Data Clock Pin in PCM mode
	DCLK	I	DSD Clock Pin in DSD mode
6	SDATA	I	Audio Serial Data Input Pin in PCM mode
	DSDL	I	DSD Lch Data Input Pin in DSD mode
7	LRCK	I	L/R Clock Pin in PCM mode
	DSDR	I	DSD Rch Data Input Pin in DSD mode
8	SMUTE	I	Soft Mute Pin in parallel mode When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CSN	I	Chip Select Pin in serial mode
9	DFS0	I	Sampling Speed Mode Select Pin in parallel mode (Internal pull-down pin)
	CAD0	I	Chip Address 0 Pin in serial mode (Internal pull-down pin)
10	DEM0	I	De-emphasis Enable 0 Pin in parallel mode
	CCLK	I	Control Data Clock Pin in serial mode
11	DEM1	I	De-emphasis Enable 1 Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode
12	DIF0	I	Digital Input Format 0 Pin in PCM mode
	DCLK	I	DSD Clock Pin in DSD mode
13	DIF1	I	Digital Input Format 1 Pin in PCM mode
	DSDL	I	DSD Lch Data Input Pin in DSD mode
14	DIF2	I	Digital Input Format 2 Pin in PCM mode
	DSDR	I	DSD Rch Data Input Pin in DSD mode

Note: All input pins except internal pull-up/down pins should not be left floating.

15	TTL	I	CMOS/TTL Level Select Pin (Internal pull-up pin) "L" : CMOS Level, "H" : TTL Level
16	VREFL	I	Low Level Voltage Reference Input Pin
17	VREFH	I	High Level Voltage Reference Input Pin
18	AVDD	-	Analog Power Supply Pin, 5.0V
19	AVSS	-	Analog Ground Pin
20	AOUTR–	O	Rch Negative Analog Output Pin
21	AOUTR+	O	Rch Positive Analog Output Pin
22	AOUTL–	O	Lch Negative Analog Output Pin
23	AOUTL+	O	Lch Positive Analog Output Pin
24	VCOM	O	Common Voltage Output Pin, AVDD/2
25	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial Mode, "H": Parallel Mode
26	TST1	O	Test 1 Pin in parallel mode (Don't Care)
	DZFL	O	Lch Zero Input Detect Pin in serial mode
27	TST2	I	Test 2 Pin in parallel mode (Internal pull-down pin)
	CAD1	I	Chip Address 1 Pin in serial mode (Internal pull-down pin)
28	ACKS	I	Master Clock Auto Setting Mode Pin in parallel mode
	DZFR	O	Rch Zero Input Detect Pin in serial mode

Note: All input pins except internal pull-up/down pins should not be left floating.
Note: TST1 pin outputs Hi-Z in parallel mode.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

(1) Parallel mode (PCM mode only)

Classification	Pin Name	Setting
Analog	AOUTL+, AOUTL–	These pins should be open.
	AOUTR+, AOUTR–	These pins should be open.
Digital	SMUTE	This pin should be connected to DVSS.
	TST1	This pin should be open.
	TST2	This pin should be connected to DVSS.

(2) Serial mode

1. PCM mode

Classification	Pin Name	Setting
Analog	AOUTL+, AOUTL–	These pins should be open.
	AOUTR+, AOUTR–	These pins should be open.
Digital	DIF2, DIF1, DIF0	These pins should be connected to DVSS.
	DZFL, DZFR	These pins should be open.

2. DSD mode

- In case of using #5(DCLK), #6(DSDL) and #7(DSDR) pins

Classification	Pin Name	Setting
Analog	AOUTL+, AOUTL–	These pins should be open.
	AOUTR+, AOUTR–	These pins should be open.
Digital	DCLK(#12), DSDL(#13), DSDR(#14)	These pins should be connected to DVSS.
	DZFL, DZFR	These pins should be open.

- In case of using #12(DCLK), #13(DSDL) and #14(DSDR) pins

Classification	Pin Name	Setting
Analog	AOUTL+, AOUTL–	These pins should be open.
	AOUTR+, AOUTR–	These pins should be open.
Digital	DCLK(#5), DSDL(#6), DSDR(#7)	These pins should be connected to DVSS.
	DZFL, DZFR	These pins should be open.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS = 0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	6.0	V
	|AVSS – DVSS| (Note 2)	Δ GND	-	0.3	V
Input Current, Any pin Except Supplies		IIN	-	±10	mA
Input Voltage		VIND	–0.3	DVDD+0.3	V
Ambient Operating Temperature		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog	AVDD	4.75	5.0	5.25	V
(Note 3)	Digital	DVDD	3.0	5.0	5.25	V
Voltage Reference	"H" voltage reference	VREFH	AVDD-0.5	-	AVDD	V
(Note 4)	"L" voltage reference	VREFL	AVSS	-	-	V
	VREFH-VREFL	Δ VREF	3.0	-	AVDD	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD and DVDD is not critical.
Note 4. Analog output voltage scales with the voltage of (VREFH – VREFL).
AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp×(VREFH – VREFL)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=5.0V; AVSS=DVSS=0V; VREFH=AVDD, VREFL=AVSS; Input data=24bit; $R_L \geq 1k\Omega$; BICK=64fs; Input Signal Frequency = 1kHz; Sampling frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Figure 17; unless otherwise specified.)

Parameter			min	typ	max	Units
Resolution					24	Bits
Dynamic Characteristics (Note 5)						
THD+N	fs=44.1kHz	0dBFS		–100	–90	dB
	BW=20kHz	–60dBFS		–57	-	dB
	fs=96kHz	0dBFS		–97	-	dB
	BW=40kHz	–60dBFS		–54	-	dB
	fs=192kHz	0dBFS		–97	-	dB
	BW=40kHz	–60dBFS		–54	-	dB
	BW=80kHz	–60dBFS		–51	-	dB
Dynamic Range (–60dBFS with A-weighted)		(Note 6)	114	120		dB
S/N (A-weighted)		(Note 7)	114	120		dB
Interchannel Isolation (1kHz)			100	120		dB
DC Accuracy						
Interchannel Gain Mismatch				0.15	0.3	dB
Gain Drift		(Note 8)		20	-	ppm/°C
Output Voltage		(Note 9)	±2.65	±2.8	±2.95	Vpp
Load Capacitance					25	pF
Load Resistance		(Note 10)	1			kΩ
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H")		(Note 11)				
AVDD				32	47	mA
DVDD (fs ≤ 96kHz)				8	-	mA
DVDD (fs = 192kHz)				13	19	mA
Power down (PDN pin = "L")		(Note 12)				
AVDD+DVDD				10	100	μA
Power Supply Rejection		(Note 13)		50		dB

Note 5. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual.
Note 6. By Figure 17. External LPF Circuit Example 2.101dB at 16bit data and 118dB at 20bit data.
Note 7. By Figure 17. External LPF Circuit Example 2. S/N does not depend on input bit length.
Note 8. The voltage on (VREFH – VREFL) is held +5V externally.
Note 9. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFH – VREFL).
AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFH – VREFL)/5.
Note 10. For AC-load. 1.5kΩ for DC-Load
Note 11. typ. 5mA (@ DVDD=3.3V, fs ≤ 96kHz), typ. 8mA (@ DVDD=3.3V, fs = 192kHz)
Note 12. In the power-down mode. P/S pin = TTL pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.
Note 13. PSR is applied to AVDD, DVDD with 1kHz, 100mVpp. VREFH pin is held +5V.

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V, DVDD=3.0 ~ 5.25V; Normal Speed Mode; DEM=OFF; SLOW bi ="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 15)	±0.01dB	PB	0		20.0	kHz
	–6.0dB		-	22.05	-	kHz
Stopband (Note 14)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 15)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	±0.2	-	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V, DVDD=3.0 ~ 5.25V; Double Speed Mode; DEM=OFF; SLOW bit="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 14)	±0.01dB	PB	0		43.5	kHz
	–6.0dB		-	48.0	-	kHz
Stopband (Note 14)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 15)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	±0.3	-	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V, DVDD=3.0 ~ 5.25V; Quad Speed Mode; DEM=OFF; SLOW bit="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 14)	±0.01dB	PB	0		87.0	kHz
	–6.0dB		-	96.0	-	kHz
Stopband (Note 14)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 15)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0/–1	-	dB

Note 14. The passband and stopband frequencies scale with fs. For example, PB = 0.4535×fs (@±0.01dB), SB = 0.546×fs.

Note 15. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V, DVDD=3.0 ~ 5.25V; Normal Speed Mode; DEM=OFF; SLOW bit="1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 16)	±0.04dB	PB	0		8.1	kHz
	–3.0dB		-	18.2	-	kHz
Stopband (Note 16)		SB	39.2			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	72			dB
Group Delay (Note 15)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	+0/–5	-	dB

SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V, DVDD=3.0 ~ 5.25V; DEM=OFF; SLOW bit="1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 16)	±0.04dB	PB	0		17.7	kHz
	–3.0dB		-	39.6	-	kHz
Stopband (Note 15)		SB	85.3			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	72			dB
Group Delay (Note 14)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	+0/–4	-	dB

SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V, DVDD=3.0 ~ 5.25V; Quad Speed Mode; DEM=OFF; SLOW bit="1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 16)	±0.04dB	PB	0		35.5	kHz
	–3.0dB		-	79.1	-	kHz
Stopband (Note 16)		SB	171			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	72			dB
Group Delay (Note 15)		GD	-	28	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0/–5	-	dB

Note 16. The passband and stopband frequencies scale with fs. For example, PB = 0.185×fs (@±0.04dB), SB = 0.888×fs.

DC CHARACTERISTICS (CMOS Level Mode)

(Ta=25°C; AVDD=4.75 ~ 5.25V, DVDD=3.0 ~ 5.25V; TTL pin = "L")

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout = –100μA)	VOH	DVDD–0.5	-	-	V
Low-Level Output Voltage (Iout = 100μA)	VOL	-	-	0.5	V
Input Leakage Current (Note 17)	Iin	-	-	±10	μA

DC CHARACTERISTICS (TTL Level Mode)

(Ta=25°C; AVDD=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; TTL pin = "H")

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (TTL pin)	VIH	70%DVDD	-	-	V
(All pins except TTL pin)	VIH	2.2	-	-	V
Low-Level Input Voltage (TTL pin)	VIL	-	-	30%DVDD	V
(All pins except TTL pin)	VIL	-	-	0.8	V
High-Level Output Voltage (Iout = –100μA)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage (Iout = 100μA)	VOL	-	-	0.5	V
Input Leakage Current (Note 17)	Iin	-	-	± 10	μA

Note 17. DFS0, TTL, P/S and TST2 pins have internal pull-down or pull-up devices, nominally 100kΩ.

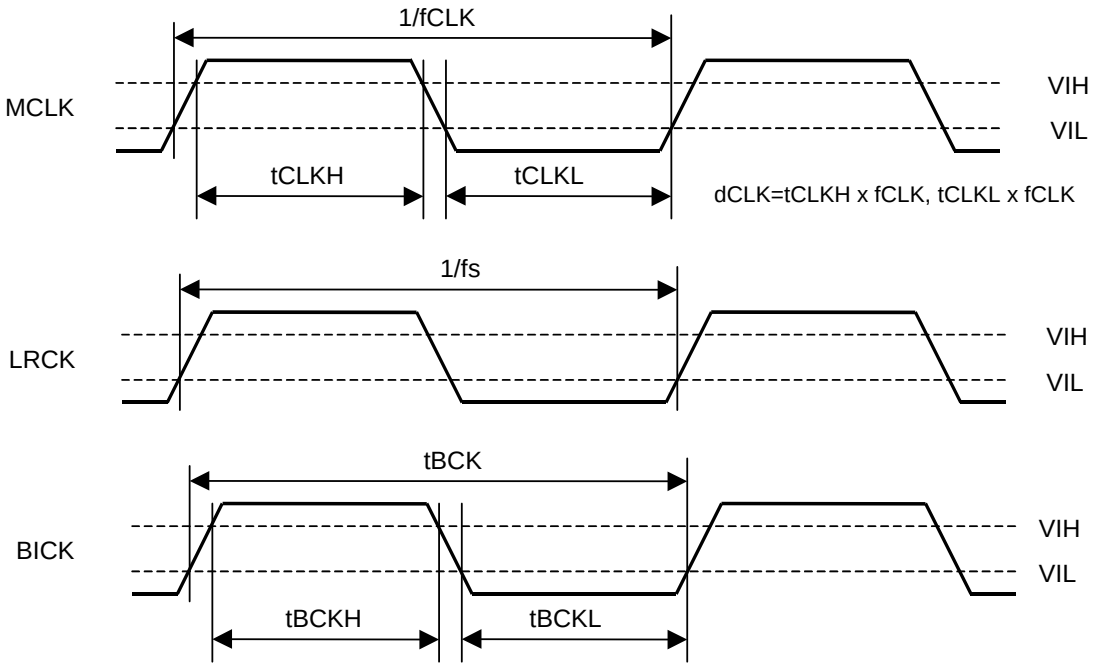
SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=4.75 ~ 5.25V, DVDD=3.0 ~ 5.25V)

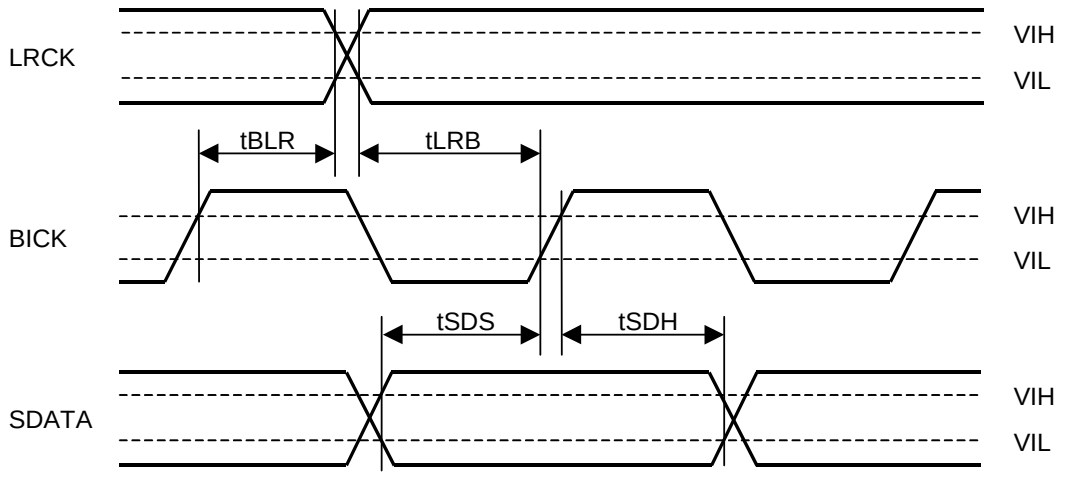
Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	7.7		41.472	MHz
Duty Cycle		dCLK	40		60	%
LRCK Frequency	(Note 18)					
Normal Speed Mode		fsn	30		54	kHz
Double Speed Mode		fsd	54		108	kHz
Quad Speed Mode		fsq	108		216	kHz
Duty Cycle		Duty	45		55	%
PCM Audio Interface Timing						
BICK Period						
Normal Speed Mode		tBCK	1/128fn			ns
Double Speed Mode		tBCK	1/64fd			ns
Quad Speed Mode		tBCK	1/64fq			ns
BICK Pulse Width Low		tBCKL	30			ns
BICK Pulse Width High		tBCKH	30			ns
BICK "↑" to LRCK Edge	(Note 19)	tBLR	20			ns
LRCK Edge to BICK "↑"	(Note 19)	tLRB	20			ns
SDATA Hold Time		tSDH	20			ns
SDATA Setup Time		tSDS	20			ns
DSD Audio Interface Timing						
DCLK Period		tDCK	1/64fs			ns
DCLK Pulse Width Low		tDCKL	160			ns
DCLK Pulse Width High		tDCKH	160			ns
DCLK Edge to DSDL/R	(Note 20)	tDDD	–20		20	ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	50			ns
CDTI Hold Time		tCDH	50			ns
CSN High Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 21)	tPD	150			ns

Note 18. When the normal/double/quad speed modes are switched, AK4396 should be reset by PDN pin or RSTN bit.
Note 19. BICK rising edge must not occur at the same time as LRCK edge.
Note 20. DSD data transmitting device must meet this time.
Note 21. The AK4396 can be reset by bringing PDN pin "L" to "H". When the states of or DFS1-0 bits change, the AK4396 should be reset by RSTN bit.

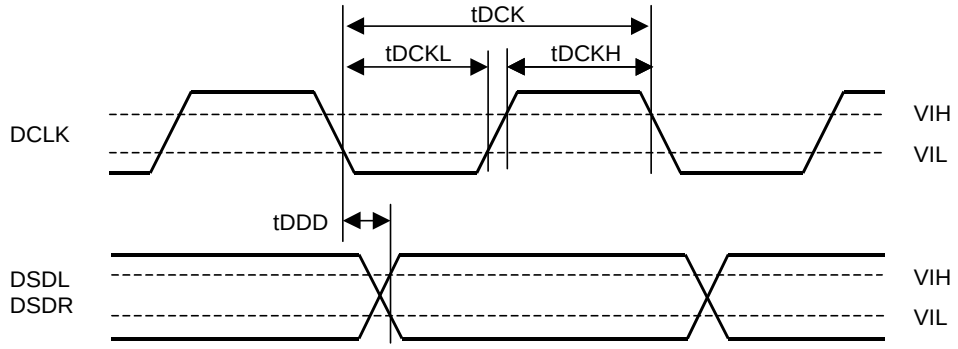
■ **Timing Diagram**



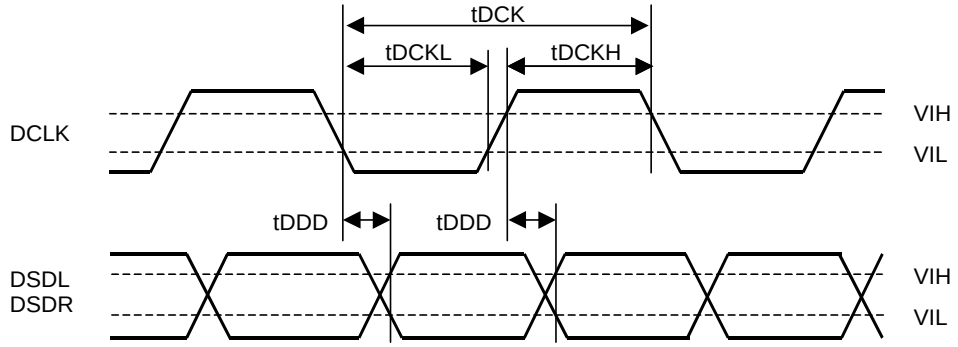
Clock Timing



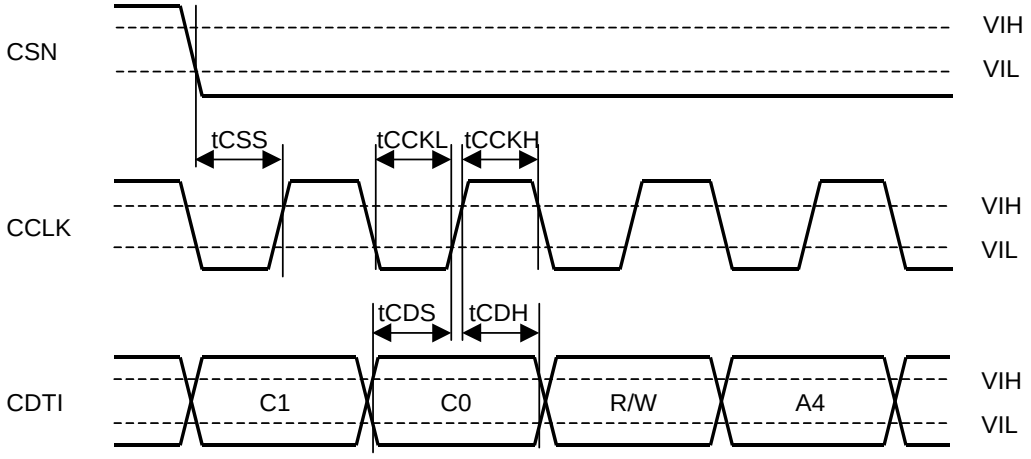
Audio Interface Timing (PCM Mode)



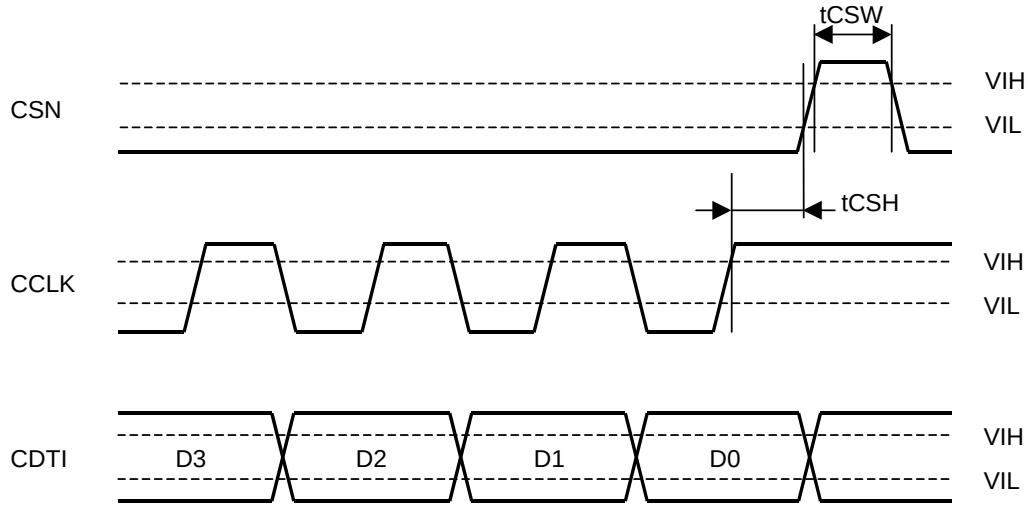
Audio Serial Interface Timing (DSD Normal Mode, DCKB bit = "0")



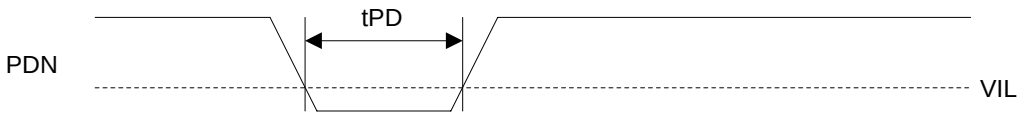
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")



WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing

OPERATION OVERVIEW

■ D/A Conversion Mode

In serial mode, the AK4396 can perform D/A conversion for either PCM data or DSD data. The D/P bit controls PCM/DSD mode. When DSD mode, DSD data can be input from DCLK, DSDL and DSDR pins. When PCM mode, PCM data can be input from BICK, LRCK and SDATA pins. When PCM/DSD mode changes by D/P bit, the AK4396 should be reset by RSTN bit. It takes about 2/fs to 3/fs to change the mode. In parallel mode, the AK4396 performs for only PCM data.

D/P bit	Interface
0	PCM
1	DSD

Table 1. PCM/DSD Mode Control

■ System Clock

[1] PCM Mode

The external clocks, which are required to operate the AK4396, are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. When external clocks are changed, the AK4396 should be reset by PDN pin or RSTN bit.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4396 is in normal operation mode (PDN pin = "H"). If these clocks are not provided, the AK4396 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4396 should be in the power-down mode (PDN pin = "L") or in the reset mode (RSTN bit = "0"). After exiting reset (PDN pin = "L" → "H") at power-up etc., the AK4396 is in power-down mode until MCLK is supplied.

(1) Parallel Mode (P/S pin = "H")

1. Manual Setting Mode (ACKS pin = "L")

MCLK frequency is detected automatically and the sampling speed is set by DFS0 pin (Table 2). The MCLK frequency corresponding to each sampling speed should be provided (Table 3). DFS1 bit is fixed to "0". When DFS0 pin is changed, the AK4396 should be reset by PDN pin. Quad speed mode is not supported in this mode.

DFS0 pin	Sampling Rate (fs)	
L	Normal Speed Mode	30kHz ~ 54kHz
H	Double Speed Mode	54kHz ~ 108kHz

Table 2. Sampling Speed (Manual Setting Mode @Parallel Mode)

LRCK	MCLK (MHz)							BICK
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	64fs
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	3.0720MHz
88.2kHz	11.2896	16.9344	22.5792	33.8688	N/A	N/A	N/A	5.6448MHz
96.0kHz	12.2880	18.4320	24.5760	36.8640	N/A	N/A	N/A	6.1440MHz

Table 3. System Clock Example (Manual Setting Mode @Parallel Mode)

2. Auto Setting Mode (ACKS pin = “H”)

MCLK frequency and the sampling speed are detected automatically (Table 4) and DFS0 pin is ignored. DFS0 pin should be fixed to DVSS or DVDD.

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 4. Sampling Speed (Auto Setting Mode @Parallel Mode)

LRCK	MCLK (MHz)							Sampling
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	Speed
32.0kHz	N/A	N/A	N/A	N/A	16.3840	24.5760	36.8640	Normal
44.1kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	N/A	
48.0kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	N/A	
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	

Table 5. System Clock Example (Auto Setting Mode @Parallel Mode)

(2) Serial Mode (P/S pin = “L”)

1. Manual Setting Mode (ACKS bit = “0”)

MCLK frequency is detected automatically and the sampling speed is set by DFS1-0 bits (Table 6). The MCLK frequency corresponding to each sampling speed should be provided (Table 7). The AK4396 is set to Manual Setting Mode at power-up (PDN pin = “L” → “H”). When DFS1-0 bits are changed, the AK4396 should be reset by RSTN bit.

DFS1 bit	DFS0 bit	Sampling Rate (fs)		
0	0	Normal Speed Mode	30kHz ~ 54kHz	Default
0	1	Double Speed Mode	54kHz ~ 108kHz	
1	0	Quad Speed Mode	120kHz ~ 216kHz	

Table 6. Sampling Speed (Manual Setting Mode @Serial Mode)

LRCK	MCLK (MHz)							BICK
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	64fs
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	3.0720MHz
88.2kHz	11.2896	16.9344	22.5792	33.8688	N/A	N/A	N/A	5.6448MHz
96.0kHz	12.2880	18.4320	24.5760	36.8640	N/A	N/A	N/A	6.1440MHz
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	11.2896MHz
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	12.2880MHz

Table 7. System Clock Example (Manual Setting Mode @Serial Mode)

2. Auto Setting Mode (ACKS bit = “1”)

MCLK frequency and the sampling speed are detected automatically (Table 8) and DFS1-0 bits are ignored. The MCLK frequency corresponding to each sampling speed should be provided (Table 9).

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 8. Sampling Speed (Auto Setting Mode @Serial Mode)

LRCK	MCLK (MHz)							Sampling
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	Speed
32.0kHz	N/A	N/A	N/A	N/A	16.3840	24.5760	36.8640	Normal
44.1kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	N/A	
48.0kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	N/A	
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A	

Table 9. System Clock Example (Auto Setting Mode @Serial Mode)

[2] DSD Mode

The external clocks, which are required to operate the AK4396, are MCLK and DCLK. MCLK should be synchronized with DCLK but the phase is not critical. The frequency of MCLK is set by DCKS bit.

All external clocks (MCLK, DCLK) should always be present whenever the AK4396 is in the normal operation mode (PDN pin = “H”). If these clocks are not provided, the AK4396 may draw excess current because the device utilizes dynamic refreshed logic internally. The AK4396 should be reset by PDN pin = “L” after these clocks are provided. If the external clocks are not present, the AK4396 should be in the power-down mode (PDN pin = “L”). After exiting reset(PDN pin = “L” → “H”) at power-up etc., the AK4396 is in the power-down mode until MCLK is input.

DCKS bit	MCLK Frequency	DCLK Frequency	
0	512fs	64fs	Default
1	768fs	64fs	

Table 10. System Clock (DSD Mode)

■ Audio Interface Format

[1] PCM Mode

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Five data formats are supported and selected by the DIF2-0 pins (Parallel mode) or DIF2-0 bits (Serial mode) as shown in Table 11. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	Input Format	BICK	Figure	
0	0	0	0	16bit LSB justified	≥ 32fs	Figure 1	
1	0	0	1	20bit LSB justified	≥ 48fs	Figure 2	
2	0	1	0	24bit MSB justified	≥ 48fs	Figure 3	Default
3	0	1	1	24bit I^2S Compatible	≥ 48fs	Figure 4	
4	1	0	0	24bit LSB justified	≥ 48fs	Figure 2	

Table 11. Audio Interface Format

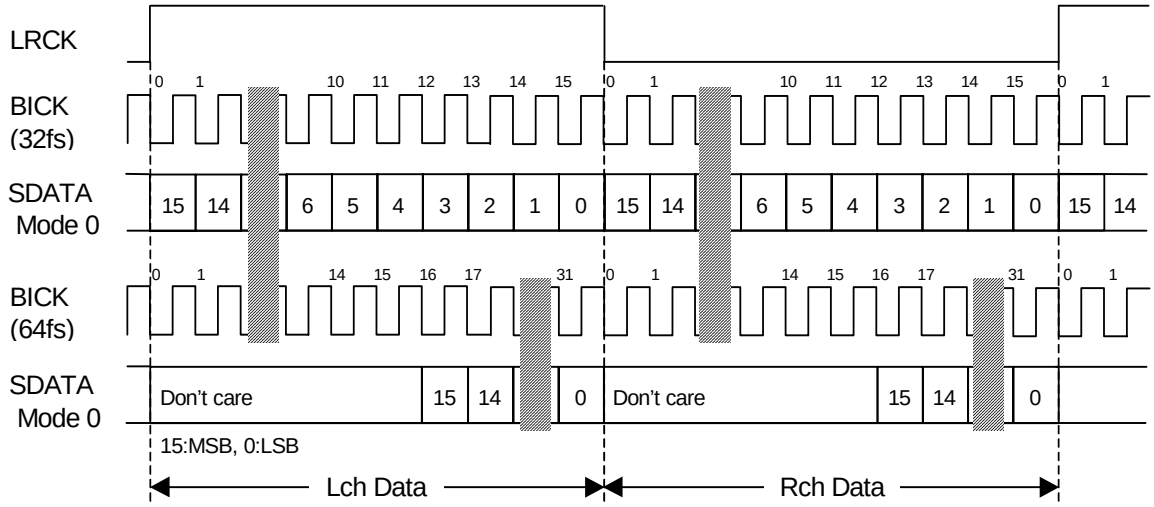


Figure 1. Mode 0 Timing

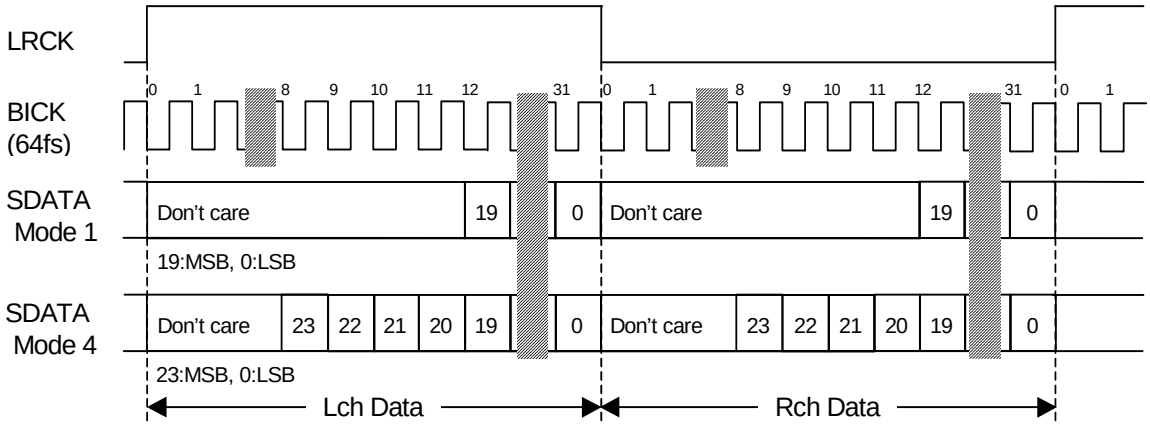


Figure 2. Mode 1, 4 Timing

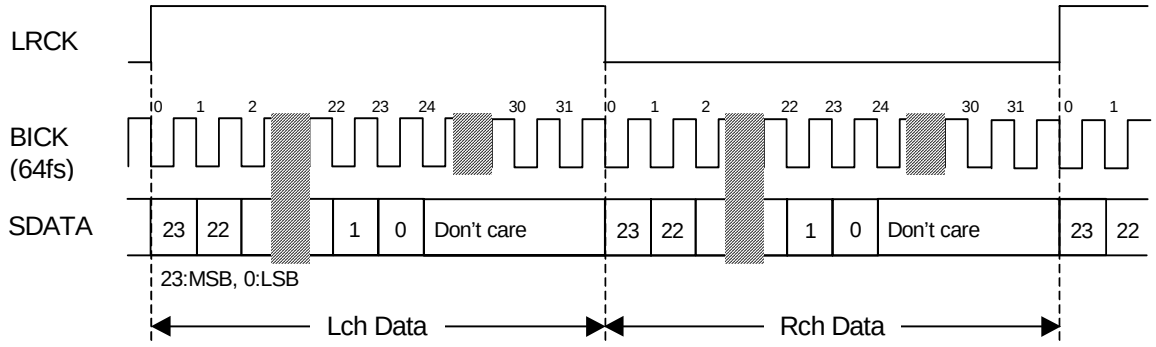


Figure 3. Mode 2 Timing

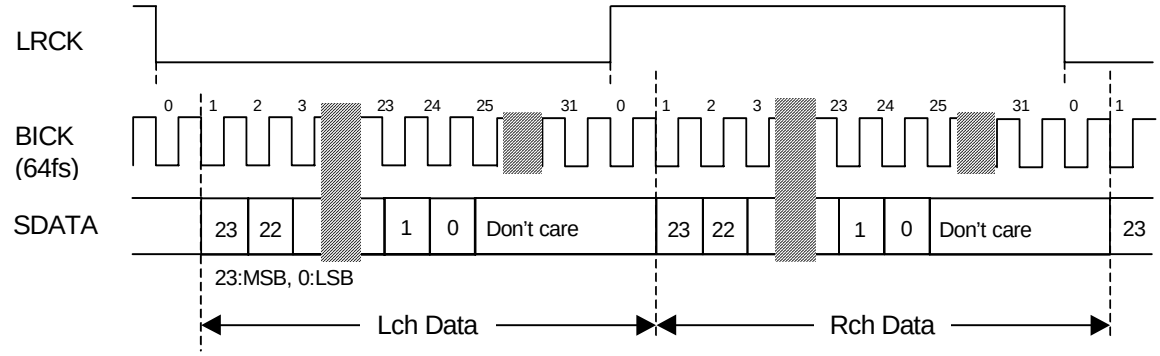


Figure 4. Mode 3 Timing

[2] DSD Mode

In case of DSD mode, DIF2-0 pins and DIF2-0 bits are ignored. The frequency of DCLK is fixed to 64fs. DCKB bit can invert the polarity of DCLK.

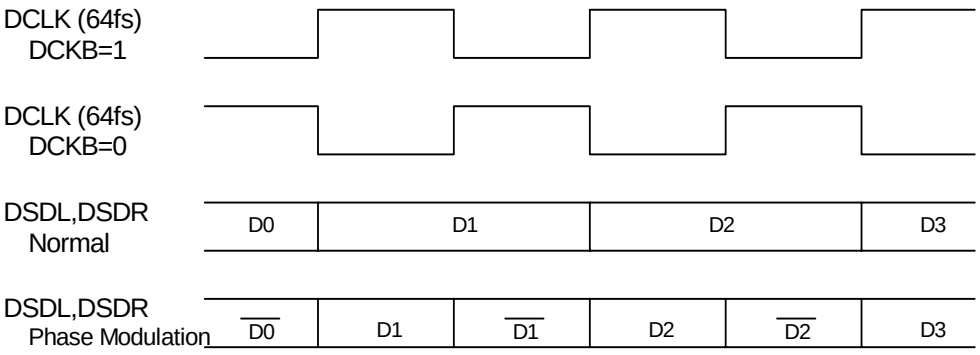


Figure 5. DSD Mode Timing

■ D/A conversion mode switching timing

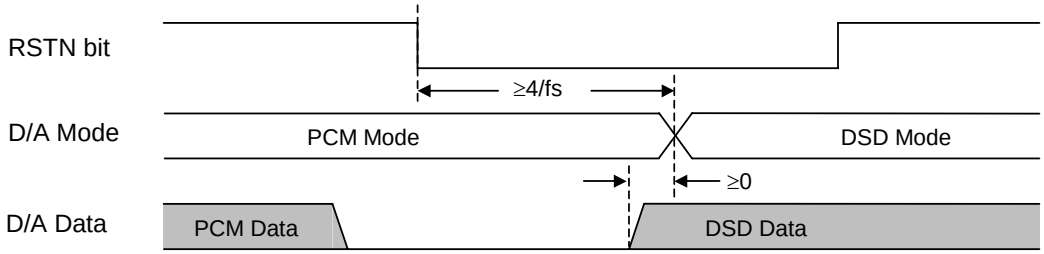


Figure 6. D/A Mode Switching Timing (PCM to DSD)

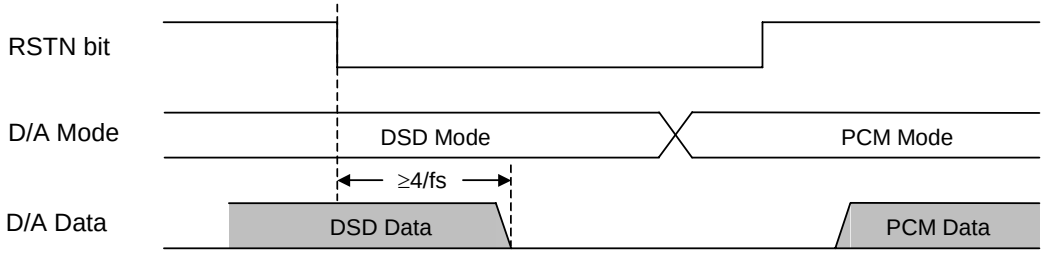


Figure 7. D/A Mode Switching Timing (DSD to PCM)

Caution: In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

■ De-emphasis Filter

A digital de-emphasis filter is available for 32kHz, 44.1kHz or 48kHz sampling rates (tc = 50/15μs) and is enabled or disabled with DEM1-0 pins or DEM1-0 bits. In case of double speed and quad speed mode, the digital de-emphasis filter is always off. When DSD mode, DEM1-0 bits are ignored. The setting value is held even if PCM mode and DSD mode are switched.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 12. De-emphasis Control (Normal Speed Mode)

■ Output Volume

The AK4396 includes channel independent digital output volumes (ATT) with 256 levels at linear step including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to –48dB and mute. When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. The transition time of 1 level and all 256 levels is shown in Table 13.

Sampling Speed	Transition Time	
	1 Level	255 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

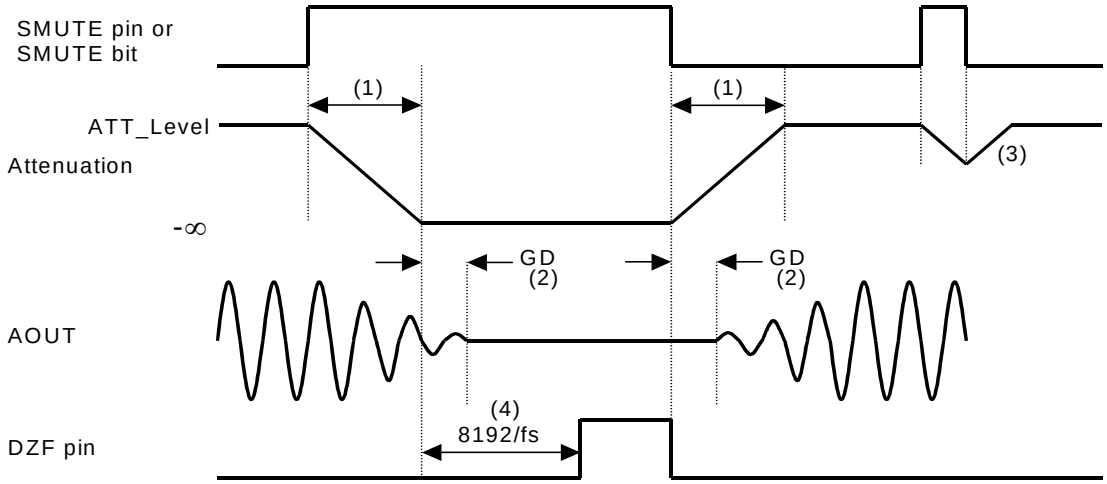
Table 13. ATT Transition Time

■ Zero Detection

The AK4396 has channel-independent zeros detect function. When the input data at each channel is continuously zeros for 8192 LRCK cycles, DZF pin of each channel goes to "H". DZF pin of each channel immediately goes to "L" if input data of each channel is not zero after going DZF pin "H". If RSTN bit is "0", DZF pins of both channels go to "H". DZF pins of both channels go to "L" at 4 ~ 5/fs after RSTN bit returns to "1". If DZFM bit is set to "1", DZF pins of both channels go to "H" only when the input data at both channels are continuously zeros for 8192 LRCK cycles. Zero detect function can be disabled by DZFE bit. In this case, DZF pins of both channels are always "L". DZFB bit can invert the polarity of DZF pin.

■ Soft Mute operation

Soft mute operation is performed at digital domain. When SMUTE pin goes to "H" or SMUTE bit goes to "1", the output signal is attenuated by –∞ during ATT_DATA × ATT transition time (Table 13) from the current ATT level. When SMUTE pin is returned to "L" or SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time. If the soft mute is cancelled before attenuating –∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA × ATT transition time (Table 13). For example, this time is 1020LRCK cycles (1020/fs) at ATT_DATA=255 in Normal Speed Mode.
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled before attenuating –∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.
(4) When the input data at each channel is continuously zeros for 8192 LRCK cycles, DZF pin of each channel goes to "H". DZF pin immediately goes to "L" if input data are not zero after going DZF pin "H".

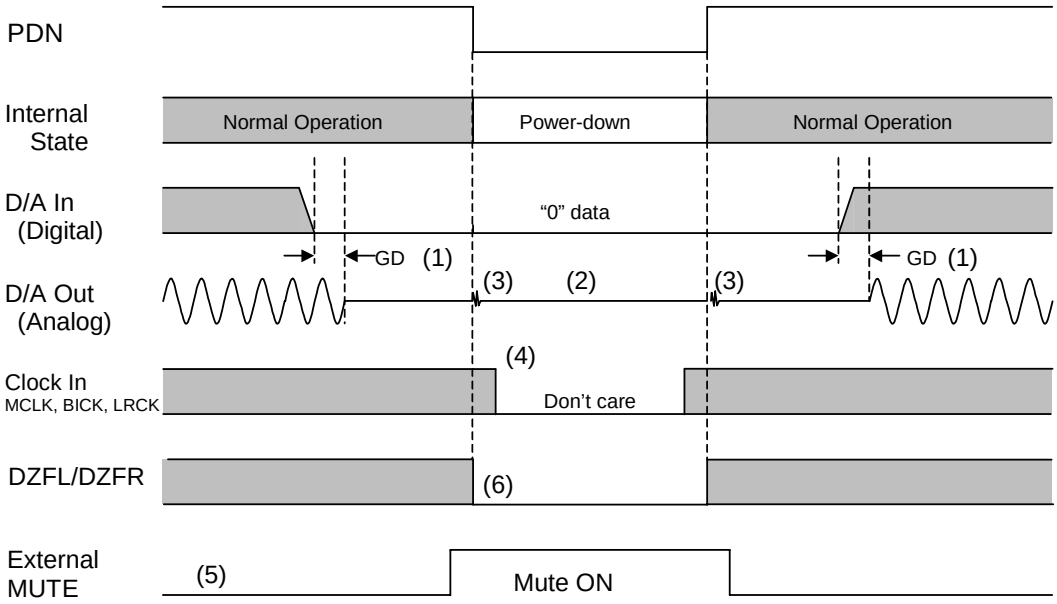
Figure 8. Soft Mute and Zero Detection

■ System Reset

The AK4396 should be reset once by bringing PDN pin = "L" upon power-up. The analog section exits power-down mode by MCLK input and then the digital section exits power-down mode after the internal counter counts MCLK during 4/fs.

■ Power-Down

The AK4396 is placed in the power-down mode by bringing PDN pin "L" and the anlog outputs are floating (Hi-Z). Figure 9 shows an example of the system timing at the power-down and power-up.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge ("↑ ↓") of PDN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN pin = "L").
(5) Please mute the analog output externally if the click noise (3) influences system application.
The timing example is shown in this figure.
(6) DZF pins are "L" in the power-down mode (PDN pin = "L").

Other:

After exiting power-down mode (PDN pin: "L" → "H"), AOUT pins go to VCOM voltage (VA/2). This time is set by a capacitor connected to VCOM pin and the internal resistor of VCOM pin.

E.g. C = 10μF

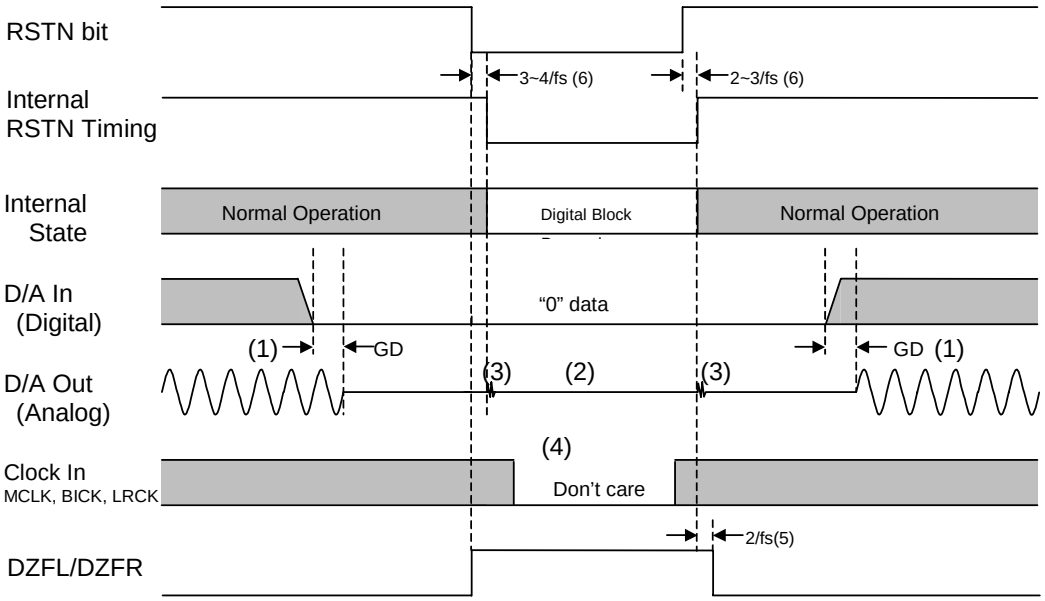
1 τ (typ) = 10μF x 0.75kΩ = 7.5ms, 5τ (typ) = 37.5ms

1 τ (max) = 10μF x 0.975kΩ = 9.75ms, 5τ (max) = 48.75ms

Figure 9. Power-down/up sequence example

■ Reset Function

When RSTN bit = "0", the AK4396's digital section is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage and DZF pins of both channels go to "H". Figure 10 shows the example of reset by RSTN bit.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs go to VCOM voltage.
(3) Click noise occurs at the edges ("↑ ↓") of the internal timing of RSTN bit.
This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode (RSTN bit = "L").
(5) DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 2/fs after RSTN bit becomes "1".
(6) There is a delay, 3 ~ 4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2 ~ 3/fs from RSTN bit "1" to the internal RSTN bit "1".

Figure 10. Reset sequence example

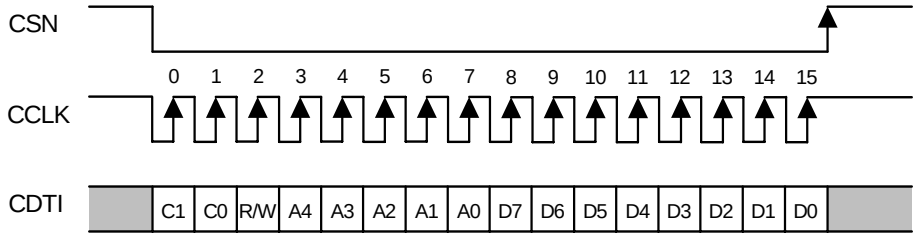
■ Register Control Interface

Pins (parallel control mode) or registers (serial control mode) can control each functions of the AK4396. In parallel mode, the register setting is ignored and the pin setting is ignored in serial mode. When the state of P/S pin is changed, the AK4396 should be reset by PDN pin. The serial control interface is enabled by the P/S pin = "L". In this mode, pin setting must be all "L". Internal registers may be written by 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2bits, CAD0/1), Read/Write (1bit; fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). The AK4396 latches the data on the rising edge of CCLK, so data should be clocked in on the falling edge. The writing of data becomes valid by CSN "↑". The clock speed of CCLK is 5MHz (max).

Function	Parallel mode	Serial mode
Auto Setting Mode	O	O
Manual Setting Mode	O	O
Audio Format	O	O
De-emphasis	O	O
SMUTE	O	O
DSD Mode	X	O
Zero Detection	X	O
Slow roll-off response	X	O
Digital Attenuator	X	O

Table 14. Function List (O: Available, X: Not available)

PDN pin = "L" resets the registers to their default values. In serial mode, the internal timing circuit is reset by RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (C1=CAD1, C0=CAD0)
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 11. Control I/F Timing

* The AK4396 does not support the read command.
* When the AK4396 is in the power down mode (PDN pin = "L") or the MCLK is not provided, writing into the control register is inhibited.
* The control data can not be written when the CCLK rising edge is 15times or less or 17times or more during CSN is "L".

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	D/P	DSDM	DCKS	DCKB	0	DZFB	0	0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Notes:
For addresses from 05H to 1FH, data must not be written.
When PDN pin goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the only internal timing is reset and the registers are not initialized to their default values.
When the state of P/S pin is changed, the AK4396 should be reset by PDN pin.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	DIF1	DIF0	RSTN
Default		0	0	0	0	0	1	0	1

RSTN: Internal timing reset
0 : Reset. All registers are not initialized.
1 : Normal Operation (Default)
When the states of DFS1-0 bits change, the AK4396 should be reset by PDN pin or RSTN bit.

DIF2-0: Audio data interface modes (see Table 11)
Initial value is “010” (Mode 2: 24bit MSB justified).

ACKS: Master Clock Frequency Auto Setting Mode Enable (PCM only)
0 : Disable : Manual setting mode (Default)
1 : Enable : Auto setting mode
When ACKS bit = “1”, MCLK frequency and the sampling frequency are detected automatically.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
Default		0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable
0 : Normal operation (Default)
1 : DAC outputs soft-muted.

DEM1-0: De-emphasis response (Table 12)
Initial value is “01” (OFF).

DFS1-0: Sampling Speed Control (Table 6)
Initial value is “00” (Normal speed).
When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs at that time.

SLOW: Slow Roll-off Filter Enable
0 : Sharp roll-off filter (Default)
1 : Slow roll-off filter

DZFM: Data Zero Detect Mode
0 : Channel separated mode (Default)
1 : Channel ANDed mode
If the DZFM bit is set to “1”, the DZF pins of both channels go to “H” only when the input data at both channels are continuously zeros for 8192 LRCK cycles.

DZFE: Data Zero Detect Enable
0 : Disable (Default)
1 : Enable
Zero detect function can be disabled by DZFE bit “0”. In this case, the DZF pins of both channels are always “L”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	D/P	DSDM	DCKS	DCKB	0	DZFB	0	0
Default		0	0	0	0	0	0	0	0

DZFB: Inverting Enable of DZF
0 : DZF pin goes “H” at Zero Detection (Default)
1 : DZF pin goes “L” at Zero Detection

DCKB: Polarity of DCLK (DSD Only)
0 : DSD data is output from DCLK falling edge. (Default)
1 : DSD data is output from DCLK rising edge.

DCKS: Master Clock Frequency Select at DSD mode (DSD only)
0 : 512fs (Default)
1 : 768fs

DSDM: DSD Input Select
0 : Input pin : No.5, 6, 7 (Default)
1 : Input pin : No. 12, 13, 14
When DSDM bit is changed, the AK4396 should be reset by RSTN bit.

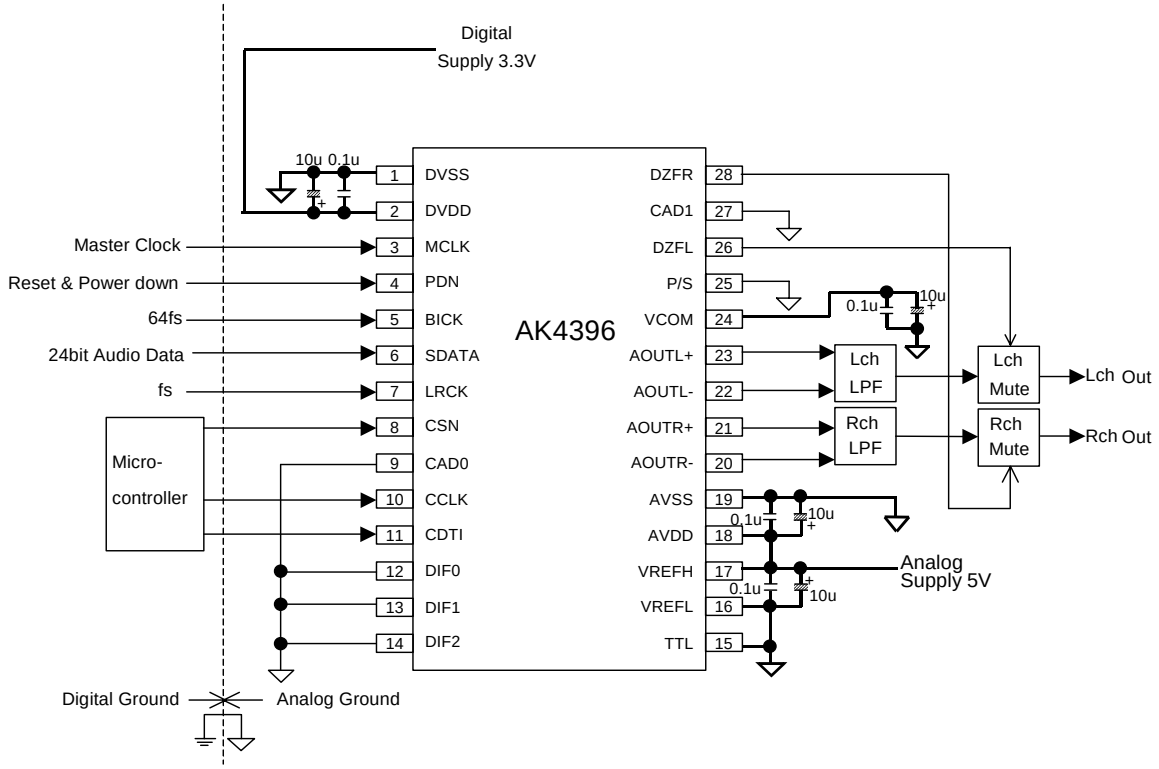
D/P: DSD/PCM Mode Select
0 : PCM mode (Default)
1 : DSD mode
When D/P bit is changed, the AK4396 should be reset by RSTN bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
Default		1	1	1	1	1	1	1	1

ATT7-0: Attenuation Level
ATT = 20 $\log_{10}$(ATT_DATA / 255) [dB]
FFH : 0dB (Default)
00H : Mute

SYSTEM DESIGN

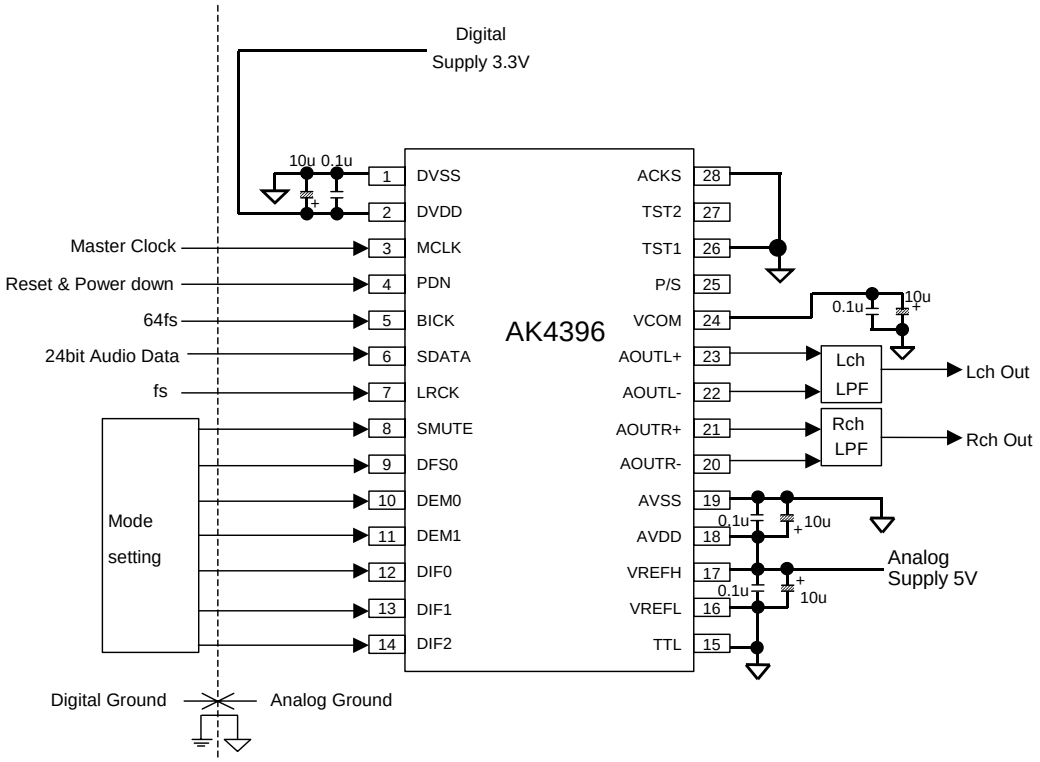
Figure 12, Figure 13 and Figure 14 show the system connection diagram. Figure 16 , Figure 17 and Figure 18 show the analog output circuit examples. An evaluation board (AKD4396) is available which demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:

- Chip Address = "00". LRCK = fs, BICK = 64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

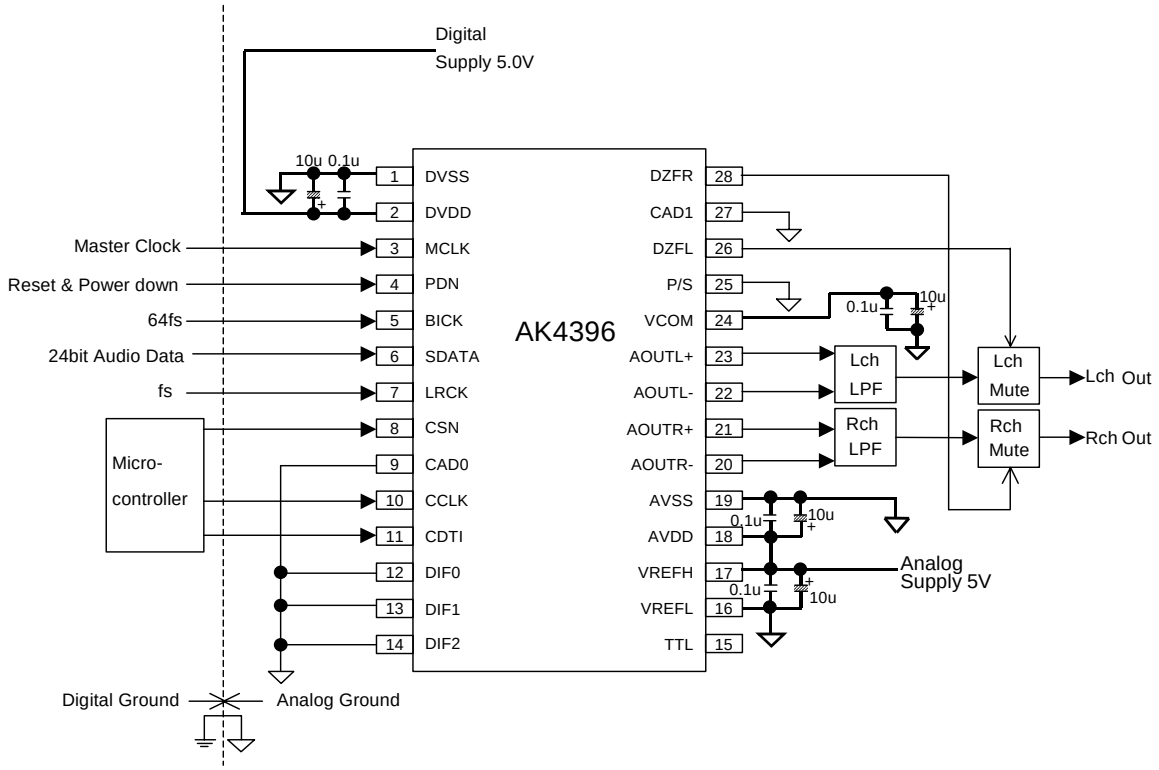
Figure 12. Typical Connection Diagram (AVDD=5V, DVDD=3.3V, Serial mode)



Notes:

- BICK = 64fs, LRCK = fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

Figure 13. Typical Connection Diagram (AVDD = 5V, DVDD = 3.3V, Parallel mode, AK4393 compatible)



Notes:

- TTL pin (BVSS pin in case of AK4394/5) should be open.
- Chip Address = "00", BICK = 64fs, LRCK = fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

Figure 14. Typical Connection Diagram (AVDD=5V, DVDD=5V, Serial mode, AK4394/5 compatible)

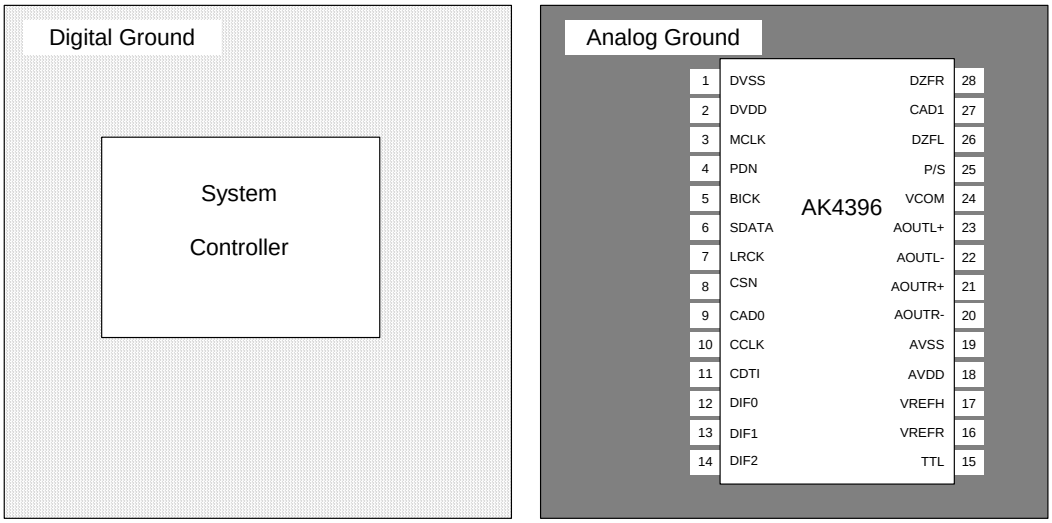


Figure 15. Ground Layout

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from digital supply in system. Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc. The power up sequence between AVDD and DVDD is not critical. **AVSS and DVSS must be connected to analog ground plane.** Decoupling capacitors for high frequency should be placed as near as possible.

2. Voltage Reference

The differential Voltage between VREFH and VREFL set the analog output range. VREFH pin is normally connected to AVDD and VREFL pin is normally connected to AVSS. VREFH and VREFL should be connected with a 0.1µF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH, VREFL and VCOM pins in order to avoid unwanted coupling into the AK4396.

3. Analog Outputs

The analog outputs are full differential outputs and 2.8Vpp (typ, VREFH – VREFL = 5V) centered around VCOM. The differential outputs are summed externally, V_{AOUT} = (AOUT+) – (AOUT–) between AOUT+ and AOUT–. If the summing gain is 1, the output range is 5.6Vpp (typ, VREFH – VREFL = 5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage (V_{AOUT}) is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal V_{AOUT} is 0V for 000000H(@24bit).

The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Figure 16 shows an example of external LPF circuit summing the differential outputs by an op-amp. Figure 17 shows an example of differential outputs and LPF circuit example by three op-amps.

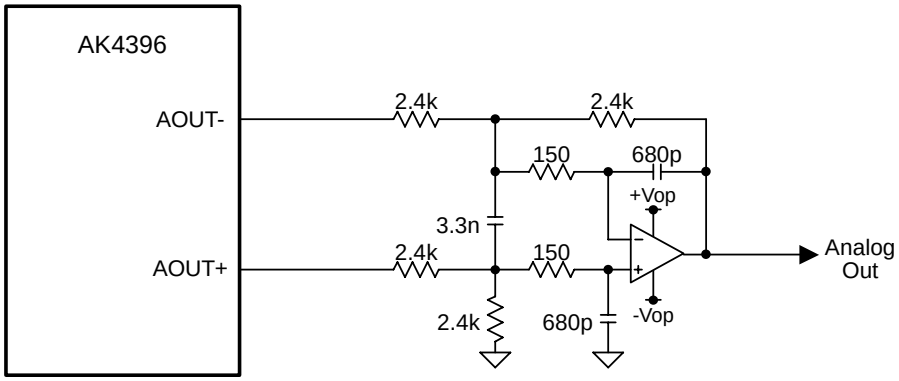


Figure 16. External LPF Circuit Example 1 for PCM (fc = 125kHz, Q=0.692)

Frequency Response	Gain
20kHz	–0.012dB
40kHz	–0.083dB
80kHz	–0.799dB

Table 15. Filter Response of External LPF Circuit Example 1 for PCM

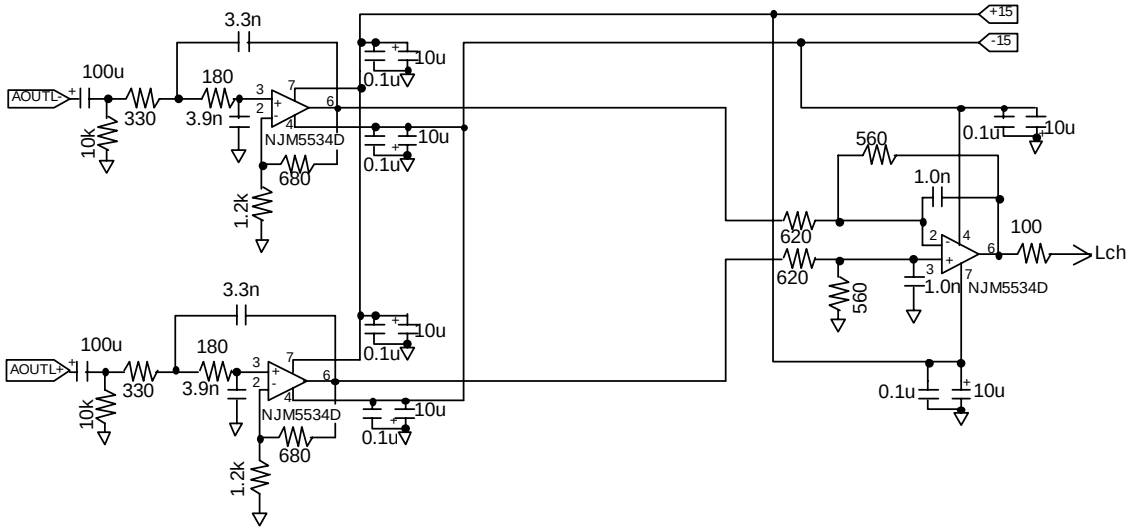


Figure 17. External LPF Circuit Example 2 for PCM

		1st Stage	2nd Stage	Total
Cut-off Frequency		182kHz	284kHz	-
Q		0.637	-	-
Gain		+3.9dB	-0.88dB	+3.02dB
Frequency Response	20kHz	-0.025	-0.021	-0.046dB
	40kHz	-0.106	-0.085	-0.191dB
	80kHz	-0.517	-0.331	-0.848dB

Table 16. Filter Response of External LPF Circuit Example 2 for PCM

It is recommended by SACD format book (Scarlet Book) that the filter response at SACD playback is an analog low pass filter with a cut-off frequency of maximum 50kHz and a slope of minimum 30dB/Oct. The AK4396 can achieve this filter response by combination of the internal filter (Table 17) and an external filter (Figure 18).

Frequency	Gain
20kHz	–0.4dB
50kHz	–2.8dB
100kHz	–15.5dB

Table 17. Internal Filter Response at DSD mode

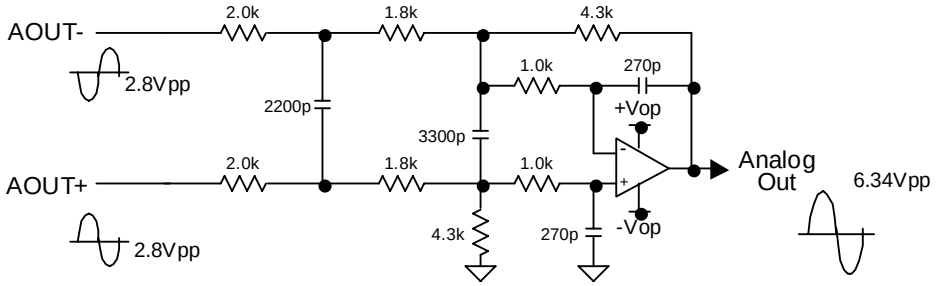


Figure 18. External 3rd order LPF Circuit Example for DSD

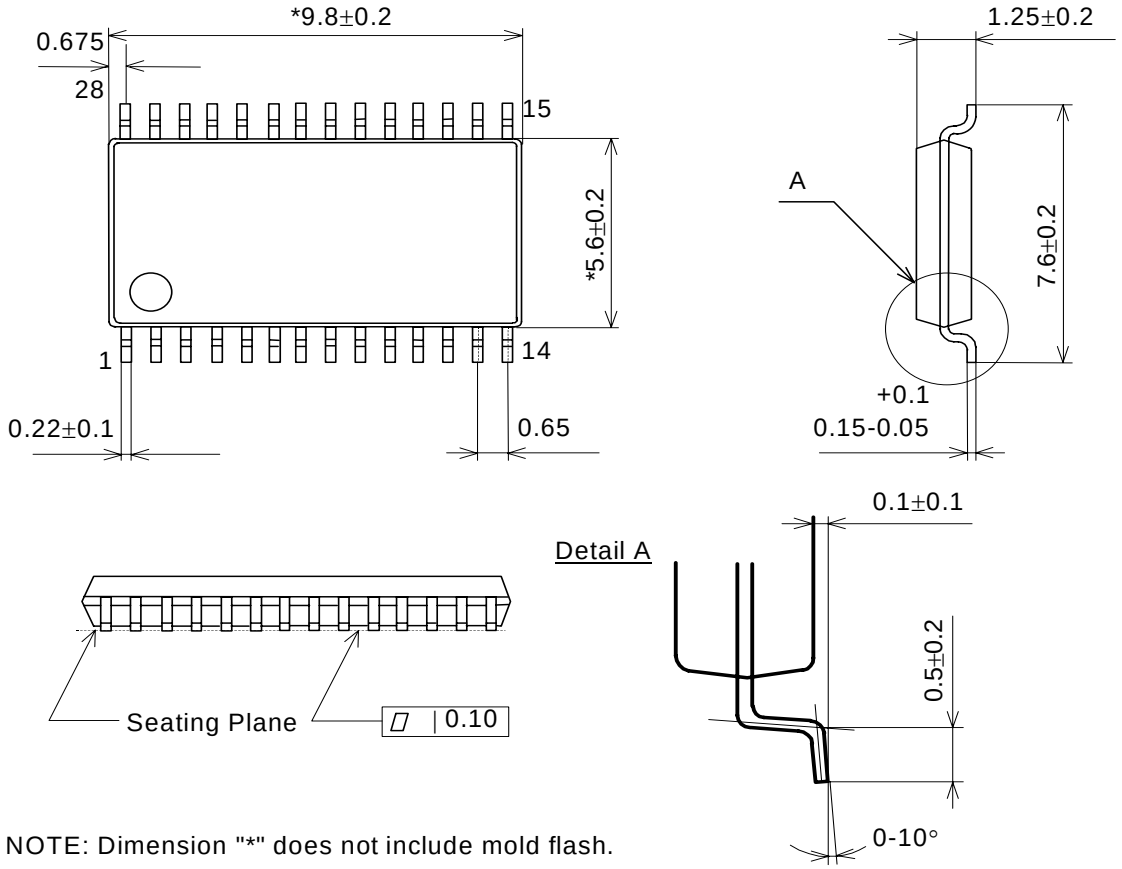
Frequency	Gain
20kHz	–0.05dB
50kHz	–0.51dB
100kHz	–16.8dB

DC gain = 1.07dB

Table 18. 3rd order LPF (Figure 18) Response

PACKAGE

28pin VSOP (Unit: mm)

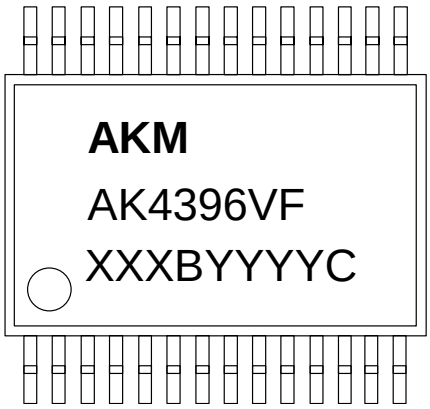


NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXXBYYYYC: Date code identifier

XXXB: Lot number (X : Digit number, B : Alpha character)
YYYYC: Assembly date (Y : Digit number C : Alpha character)

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
04/08/31	00	First Edition		