Ordering number:ENN4145

Monolithic Linear IC

LA5318M

Variable Divided Voltage Generator for LCD Use

Overview

The LA5318M is a variable divided voltage generator IC for multiple drive of LCD matrix.

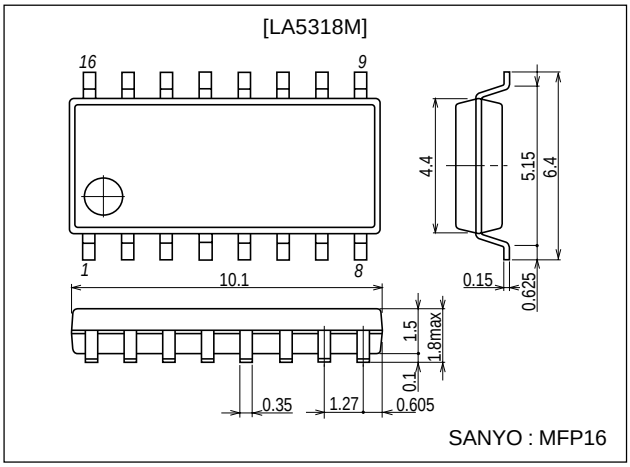
Features

- Power supply for variable bias LCD division drive (1/5 to 1/19 bias available by built-in resistances).
- Four operational amplifiers to deliver 5 voltage outputs.
- Low current drain (0.35mA typ).
- V1, V2 output current source side variable pin.
- Output on/off function V_{REF} control pins.
- Miniflat package.

Package Dimensions

unit:mm

3035A-MFP16



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{EE} max	V_{CC}-V_{EE}	36	V
Maximum output current	I_{OUT} max	V1 to V4	Internal *	mA
Allowable power dissipation	Pd max		330	mW
Operating temperature	Topr		–20 to +75	˚C
Storage temperature	Tstg		–30 to +135	˚C

Note : 1. Continuous operation (nonbreakdown) is guaranteed when operated at the maximum ratings shown above.

2. *The maximum output current is a value specified under the conditions otherwise specified separately.

3. Output pins V1 to V4 to V_{CC}, GND short circuit not lasting more than 1ms is acceptable ($|V_{CC} - V_{EE}| < 35V$).

Operating Conditions at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{EE}	$V_{REF} \geq V_{EE}$	–35.5 to –6	V
Input voltage	V_{REF}		–35 to –6	V
Input current	I_{INR}		–0.2 to 0	mA
Output current	I_{OUTR}		0 to +50	mA
	$I_{OUT1, 2}$		–5 to +5	mA
	$I_{OUT3, 4}$		–10 to +5	mA

Note : 4. Set V_{CC} and V_{EE} so that | V1 | and | V_{EE}-V4 | become 1V or greater.

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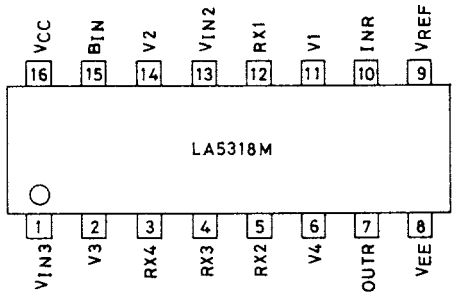
Operating Characteristics at Ta = 25˚C, V_{CC}–V_{EE}=20V, V_{REF}=V_{EE}, R_X=8R, B_{IN}=Open

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}, I_{EE}	V_{CC}–V_{EE}=20V, R_X=8R, INR=V_{CC}		0.35	0.5	mA
Output voltage ratio 1	Ra1	V2/V1	1.96	2.00	2.04	
Output voltage ratio 2	Ra2	(V_{REF}-V3)/(V_{REF}-V4)	1.96	2.00	2.04	
Output voltage ratio 3	Rb1	V_{REF}/V1	11.64	12.00	12.36	
Output voltage ratio 4	Rb2	V_{REF}/V2	5.82	6.00	6.18	
Output voltage ratio 5	Rb3	V_{REF}/(V_{REF}-V3)	5.82	6.00	6.18	
Output voltage ratio 6	Rb4	V_{REF}/(V_{REF}-V4)	11.64	12.00	12.36	
Internal resistance ratio 1	R_X1	R_X1-R_X2 *		8		
Internal resistance ratio 2	R_X2	R_X2-R_X3 *		12		
Internal resistance ratio 3	R_X3	R_X3-R_X4 *		14		
Internal resistance ratio 4	R_X4	R_X4-V_{IN}3 *		15		
Resistance	R	R value when 0.5V is applied across R_X4 and V_{IN}3		30		kΩ
Load regulation 1	ΔV1	+0.1mA<I_{OUT}1<+5mA			±20	mV
Load regulation 2	ΔV2	+0.1mA<I_{OUT}2<+5mA			±20	mV
Load regulation 3	ΔV3	+0.1mA<I_{OUT}3<+5mA			±20	mV
Load regulation 4	ΔV4	+0.1mA<I_{OUT}4<+5mA			±20	mV
Load regulation –1A	–ΔV1A	–0.5mA<I_{OUT}1<–0.1mA			±20	mV
Load regulation –2A	–ΔV2A	–0.5mA<I_{OUT}2<–0.1mA			±20	mV
Load regulation –3	–ΔV3	–10mA<I_{OUT}3<–0.1mA			±20	mV
Load regulation –4	–ΔV4	–10mA<I_{OUT}4<–0.1mA			±20	mV
Load regulation –1B	–ΔV1B	–5mA<I_{OUT}1<–0.1mA, B_{IN}=GND			±20	mV
Load regulation –2B	–ΔV2B	–5mA<I_{OUT}2<–0.1mA, B_{IN}=GND			±20	mV
OUTR saturation voltage	V_{OUTR}	I_{OUT}=20mA, V_{CC}–INR=2.7V (Source I_{OUT} is negative (–) and sink. I_{OUT} is positive (+).)			0.5	V

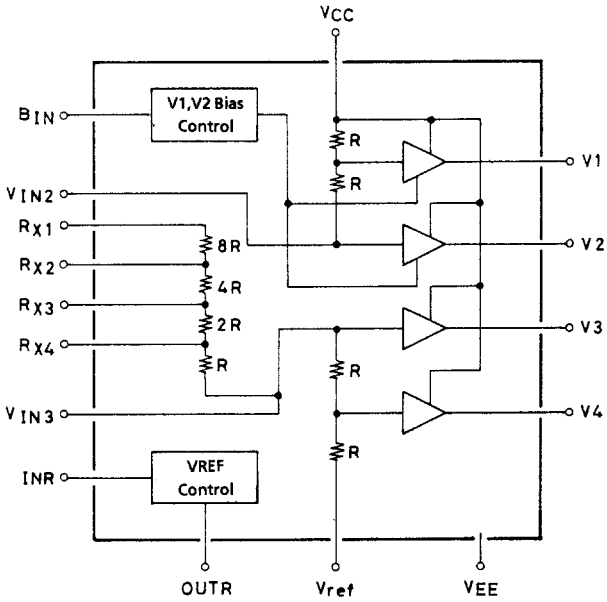
Note* : Referenced to R between R_X4 and V_{IN}3.

Pin Assignment



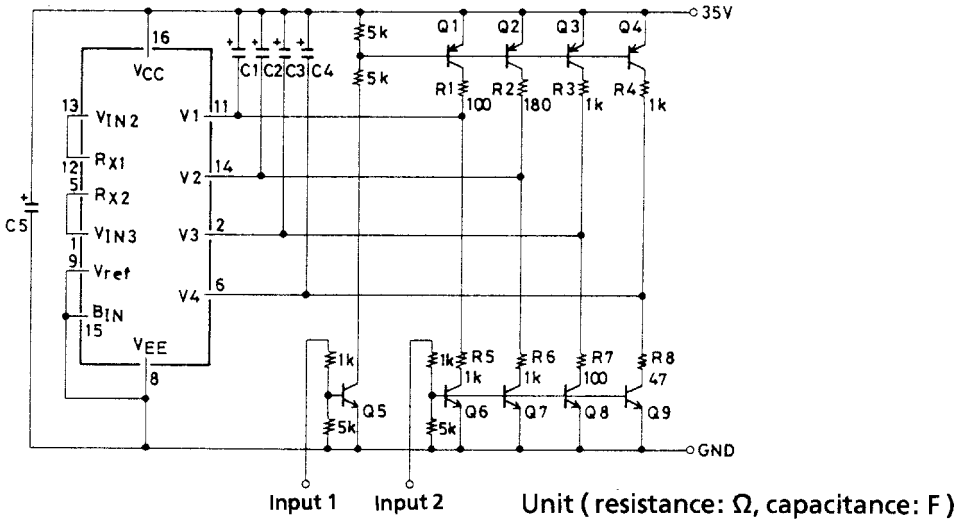
Top view

Block Diagram



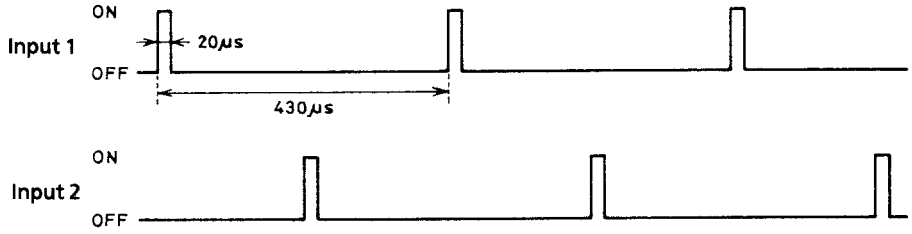
Note : Use the IC so that $V_{RX1} \geq V_{RX2} \geq V_{RX3} \geq V_{RX4}$ must be obeyed.

Maximum Output Current Load Test Conditions



V_{CC}–V_{EE}=35V R_X=8R C1 to C4=10μF C5=33μF R ; 1W or more
Q1 to 4 ; 2SA984 E or F rank
Q5 to 9 ; 2SC2274 E or F rank

Output load resistances R1 to R8 are set in order that current of 25 to 30mA max. (V3, V4 source side : about 60mA) are supplied to both source and sink sides when an on-level input is applied to the inputs 1 or 2.



V_{REF} Control Block

How to calculate the Q1 drive current.

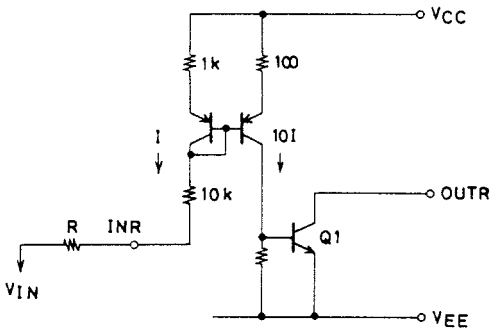
$$I = \frac{V_{CC} - V_{BE} - V_{IN}}{11k + R}$$

($V_{BE} \approx 0.7V$)

Drive current

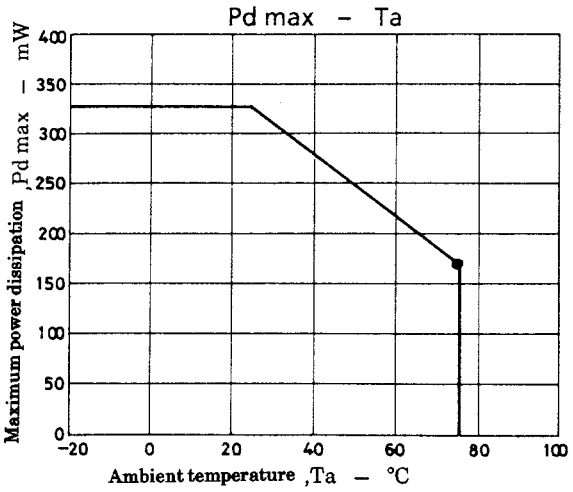
$$I_O \approx 10I = \frac{V_{CC} - 0.7 - V_{IN}}{11k + R} \times 10$$

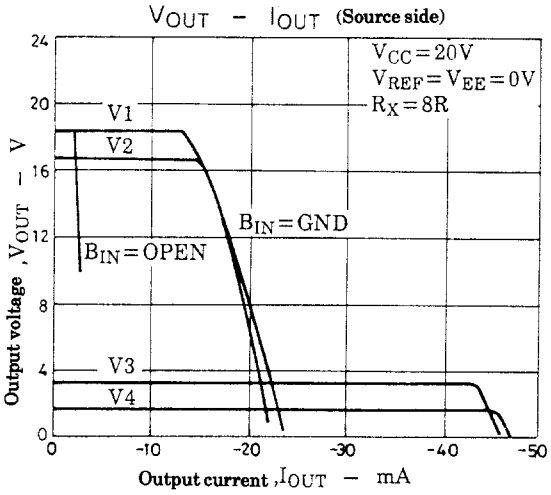
Q1 h_{FE} is assumed to be 50.

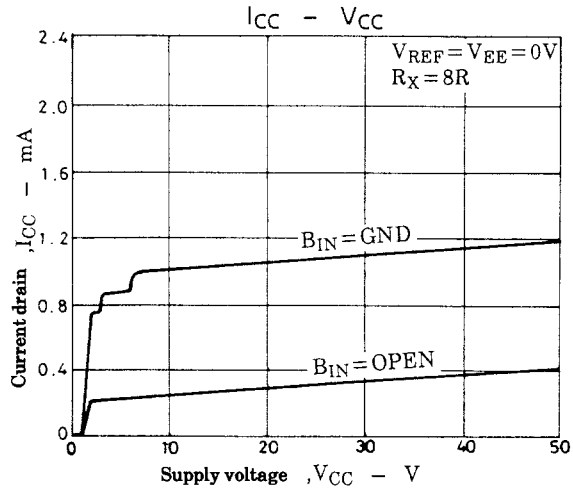


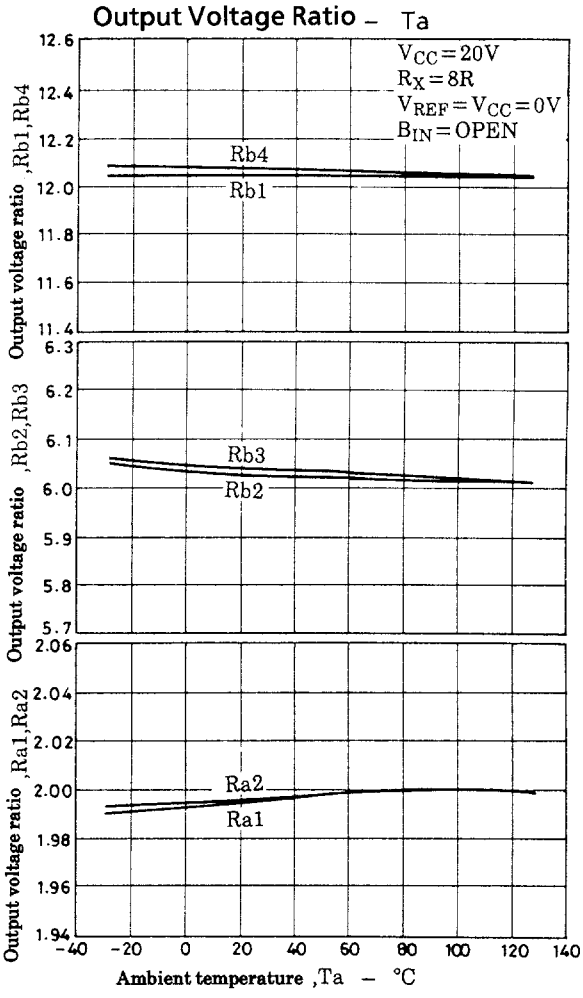
Unit (resistance: Ω)

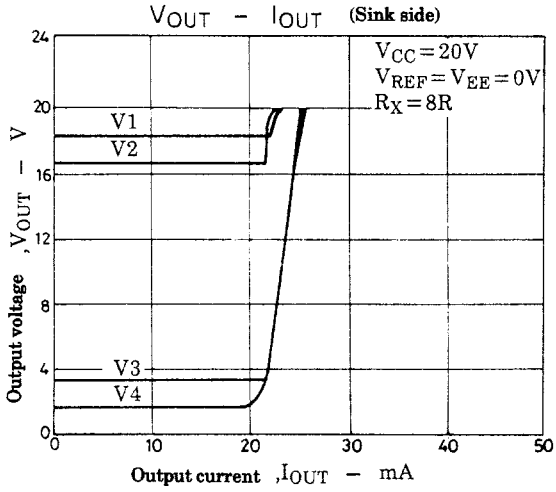
* Set V_{CC}=INR when INR and OUTR are not used.


Pd max – Ta
Maximum power dissipation ,Pd max – mW
400
350
300
250
200
150
100
50
0
–20
0
20
40
60
80
100
Ambient temperature ,Ta – °C


VOUT – IOUT (Source side)
VCC=20V
VREF=VEE=0V
RX=8R
V1
V2
BIN=GND
BIN=OPEN
V3
V4
Output voltage ,VOUT – V
24
20
16
12
8
4
0
0
-10
-20
-30
-40
-50
Output current ,IOUT – mA


ICC – VCC
VREF=VEE=0V
RX=8R
BIN=GND
BIN=OPEN
Current drain ,ICC – mA
2.4
2.0
1.6
1.2
0.8
0.4
0
0
10
20
30
40
50
Supply voltage ,VCC – V


Output Voltage Ratio – Ta
VCC=20V
RX=8R
VREF=VCC=0V
BIN=OPEN
Rb4
Rb1
Output voltage ratio ,Rb1,Rb4
12.6
12.4
12.2
12.0
11.8
11.6
11.4
Rb3
Rb2
Output voltage ratio ,Rb2,Rb3
6.3
6.2
6.1
6.0
5.9
5.8
5.7
Ra2
Ra1
Output voltage ratio ,Ra1,Ra2
2.06
2.04
2.02
2.00
1.98
1.96
1.94
–40
–20
0
20
40
60
80
100
120
140
Ambient temperature ,Ta – °C


VOUT – IOUT (Sink side)
VCC=20V
VREF=VEE=0V
RX=8R
V1
V2
V3
V4
Output voltage ,VOUT – V
24
20
16
12
8
4
0
0
10
20
30
40
50
Output current ,IOUT – mA