



# LA5318M

## Variable Divided Voltage Generator for LCD Use

### Overview

The LA5318M is a variable divided voltage generator IC for multiple drive of LCD matrix.

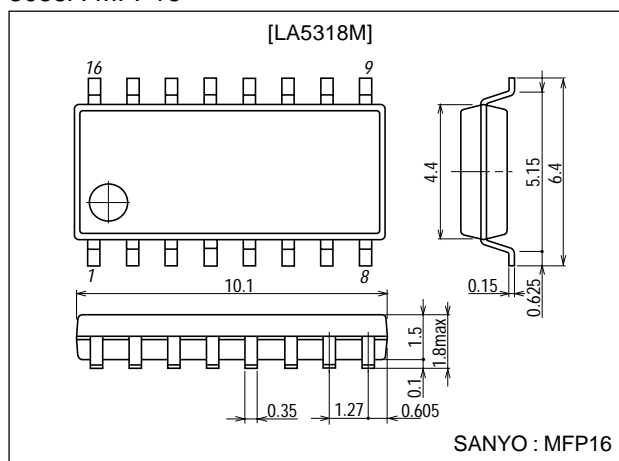
### Features

- Power supply for variable bias LCD division drive (1/5 to 1/19 bias available by built-in resistances).
- Four operational amplifiers to deliver 5 voltage outputs.
- Low current drain (0.35mA typ).
- V1, V2 output current source side variable pin.
- Output on/off function  $V_{REF}$  control pins.
- Miniflat package.

### Package Dimensions

unit:mm

3035A-MFP16



### Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{EE\text{ max}}$	$V_{CC}-V_{EE}$	36	V
Maximum output current	$I_{OUT\text{ max}}$	V1 to V4	Internal *	mA
Allowable power dissipation	$P_d\text{ max}$		330	mW
Operating temperature	$T_{opr}$		-20 to +75	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-30 to +135	$^\circ\text{C}$

Note : 1. Continuous operation (nonbreakdown) is guaranteed when operated at the maximum ratings shown above.

2. \*The maximum output current is a value specified under the conditions otherwise specified separately.

3. Output pins V1 to V4 to  $V_{CC}$ , GND short circuit not lasting more than 1ms is acceptable ( $|V_{CC} - V_{EE}| < 35\text{V}$ ).

**Operating Conditions** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{EE}$	$V_{REF} \geq V_{EE}$	-35.5 to -6	V
Input voltage	$V_{REF}$		-35 to -6	V
Input current	$I_{INR}$		-0.2 to 0	mA
Output current	$I_{OUTR}$		0 to +50	mA
	$I_{OUT1, 2}$		-5 to +5	mA
	$I_{OUT3, 4}$		-10 to +5	mA

Note : 4. Set  $V_{CC}$  and  $V_{EE}$  so that  $|V1|$  and  $|V_{EE}-V4|$  become 1V or greater.

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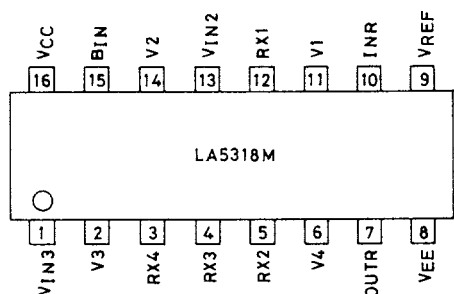
# LA5318M

**Operating Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V_{CC}-V_{EE}=20\text{V}$ ,  $V_{REF}=V_{EE}$ ,  $R_X=8R$ ,  $B_{IN}=\text{Open}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	$I_{CC}, I_{EE}$	$V_{CC}-V_{EE}=20\text{V}$ , $R_X=8R$ , $INR=V_{CC}$		0.35	0.5	mA
Output voltage ratio 1	Ra1	$V_2/V_1$	1.96	2.00	2.04	
Output voltage ratio 2	Ra2	$(V_{REF}-V_3)/(V_{REF}-V_4)$	1.96	2.00	2.04	
Output voltage ratio 3	Rb1	$V_{REF}/V_1$	11.64	12.00	12.36	
Output voltage ratio 4	Rb2	$V_{REF}/V_2$	5.82	6.00	6.18	
Output voltage ratio 5	Rb3	$V_{REF}/(V_{REF}-V_3)$	5.82	6.00	6.18	
Output voltage ratio 6	Rb4	$V_{REF}/(V_{REF}-V_4)$	11.64	12.00	12.36	
Internal resistance ratio 1	$R_{X1}$	$R_{X1}-R_{X2}^*$		8		
Internal resistance ratio 2	$R_{X2}$	$R_{X2}-R_{X3}^*$		12		
Internal resistance ratio 3	$R_{X3}$	$R_{X3}-R_{X4}^*$		14		
Internal resistance ratio 4	$R_{X4}$	$R_{X4}-V_{IN3}^*$		15		
Resistance	R	R value when 0.5V is applied across $R_{X4}$ and $V_{IN3}$		30		k $\Omega$
Load regulation 1	$\Delta V_1$	$+0.1\text{mA} < I_{OUT1} < +5\text{mA}$			$\pm 20$	mV
Load regulation 2	$\Delta V_2$	$+0.1\text{mA} < I_{OUT2} < +5\text{mA}$			$\pm 20$	mV
Load regulation 3	$\Delta V_3$	$+0.1\text{mA} < I_{OUT3} < +5\text{mA}$			$\pm 20$	mV
Load regulation 4	$\Delta V_4$	$+0.1\text{mA} < I_{OUT4} < +5\text{mA}$			$\pm 20$	mV
Load regulation -1A	$-\Delta V_{1A}$	$-0.5\text{mA} < I_{OUT1} < -0.1\text{mA}$			$\pm 20$	mV
Load regulation -2A	$-\Delta V_{2A}$	$-0.5\text{mA} < I_{OUT2} < -0.1\text{mA}$			$\pm 20$	mV
Load regulation -3	$-\Delta V_3$	$-10\text{mA} < I_{OUT3} < -0.1\text{mA}$			$\pm 20$	mV
Load regulation -4	$-\Delta V_4$	$-10\text{mA} < I_{OUT4} < -0.1\text{mA}$			$\pm 20$	mV
Load regulation -1B	$-\Delta V_{1B}$	$-5\text{mA} < I_{OUT1} < -0.1\text{mA}$ , $B_{IN}=\text{GND}$			$\pm 20$	mV
Load regulation -2B	$-\Delta V_{2B}$	$-5\text{mA} < I_{OUT2} < -0.1\text{mA}$ , $B_{IN}=\text{GND}$			$\pm 20$	mV
OUTR saturation voltage	$V_{OUTR}$	$I_{OUT}=20\text{mA}$ , $V_{CC}-INR=2.7\text{V}$ (Source $I_{OUT}$ is negative (-) and sink. $I_{OUT}$ is positive (+).)			0.5	V

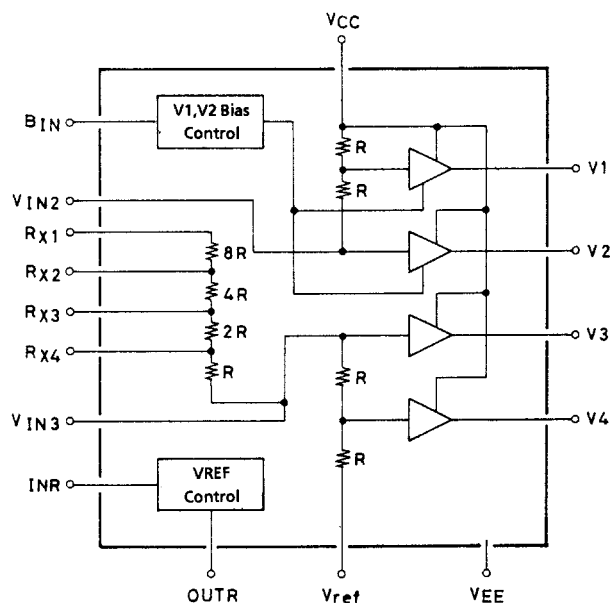
Note\* : Referenced to R between  $R_{X4}$  and  $V_{IN3}$ .

## Pin Assignment



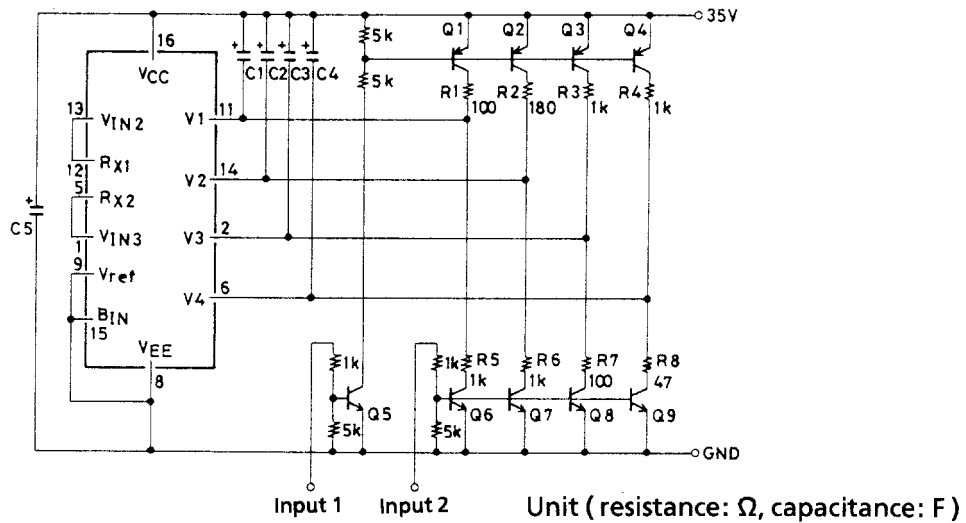
Top view

## Block Diagram



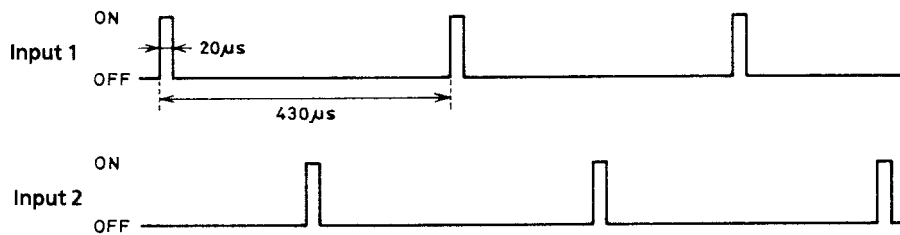
Note : Use the IC so that  $V_{RX1} \geq V_{RX2} \geq V_{RX3} \geq V_{RX4}$  must be obeyed.

## Maximum Output Current Load Test Conditions



$V_{CC}-V_{EE}=35V$   $R_X=8R$   $C1$  to  $C4=10\mu F$   $C5=33\mu F$   $R$  ; 1W or more  
 $Q1$  to  $4$  ; 2SA984 E or F rank  
 $Q5$  to  $9$  ; 2SC2274 E or F rank

Output load resistances  $R1$  to  $R8$  are set in order that current of 25 to 30mA max. ( $V3$ ,  $V4$  source side : about 60mA) are supplied to both source and sink sides when an on-level input is applied to the inputs 1 or 2.



## $V_{REF}$ Control Block

How to calculate the  $Q1$  drive current.

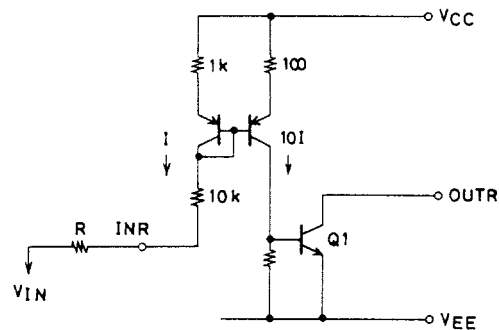
$$I = \frac{V_{CC} - V_{BE} - V_{IN}}{11k + R}$$

$$(V_{BE} \approx 0.7V)$$

Drive current

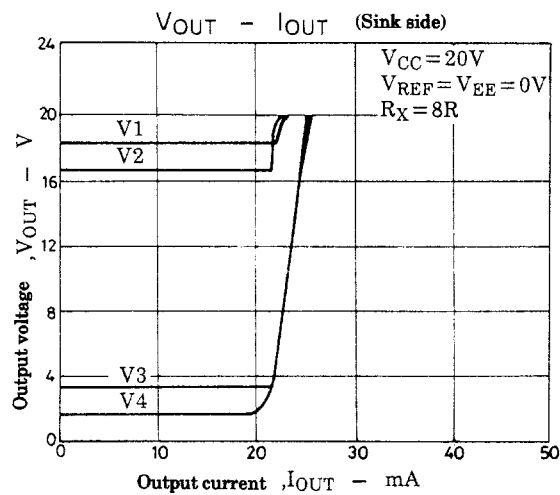
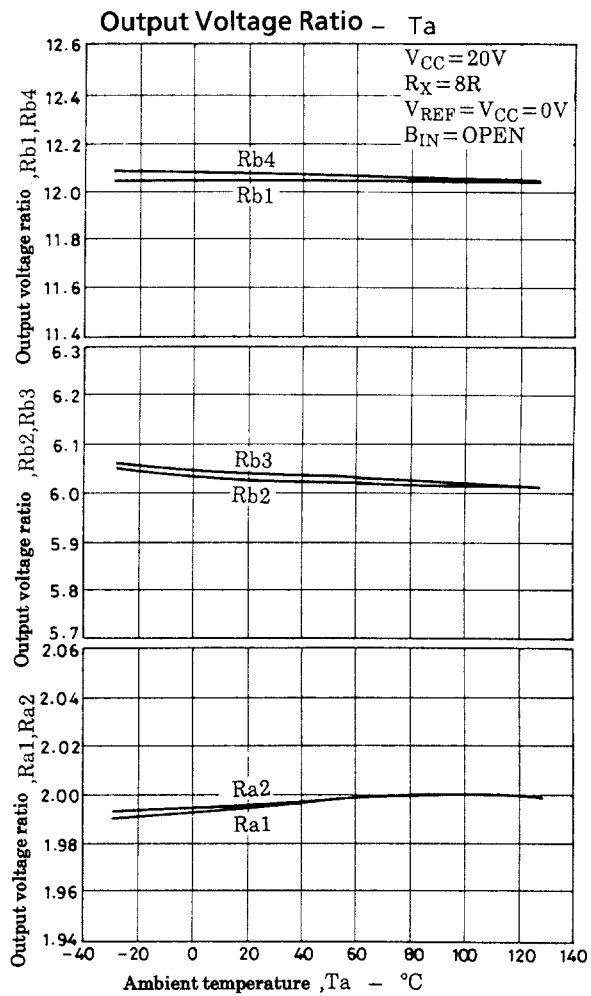
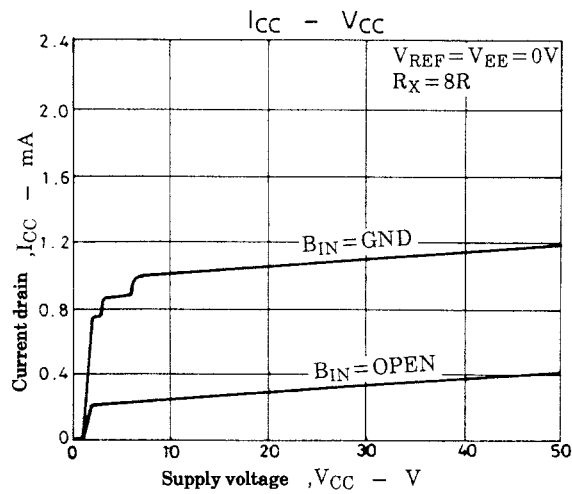
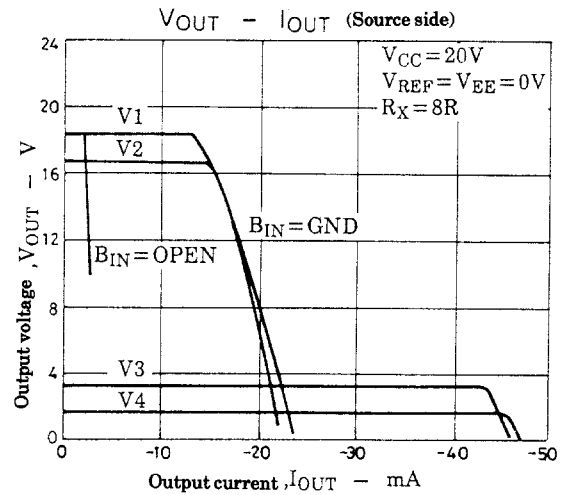
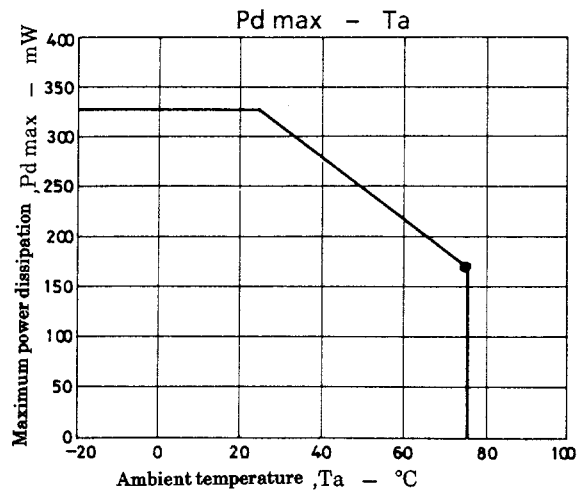
$$I_O \approx 10I = \frac{V_{CC} - 0.7 - V_{IN}}{11k + R} \times 10$$

$Q1$   $h_{FE}$  is assumed to be 50.



Unit ( resistance:  $\Omega$  )

\* Set  $V_{CC}=INR$  when  $INR$  and  $OUTR$  are not used.



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