

Low Power 5V RS232 Dual Driver/Receiver with 0.1 μ F Capacitors

FEATURES

- ESD Protection over $\pm 10\text{kV}$
- Low Cost
- Uses Small Capacitors: 0.1 μF
- CMOS Comparable Low Power: 40mW
- Operates from a Single 5V Supply
- **120kbaud Operation for $R_L = 3\text{k}$, $C_L = 2500\text{pF}$**
- **250kbaud Operation for $R_L = 3\text{k}$, $C_L = 1000\text{pF}$**
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Powered Down
- Absolutely No Latchup
- Available in Narrow SO Package

APPLICATIONS

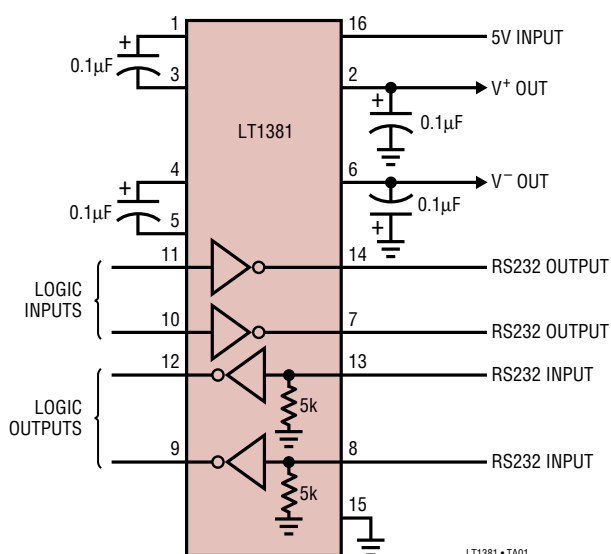
- Portable Computers
- Battery-Powered Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

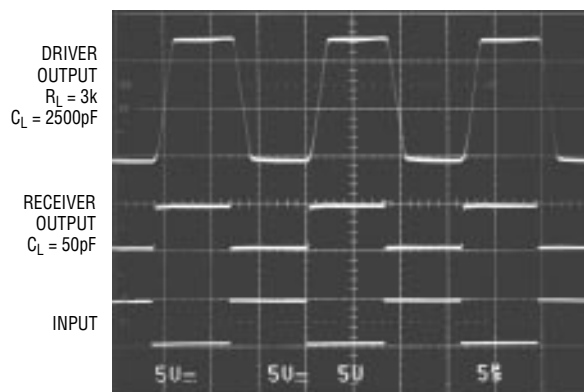
The LT[®]1381 is a dual RS232 driver/receiver pair with integral charge pump to generate RS232 voltage levels from a single 5V supply. The circuit features rugged bipolar design to provide operating fault tolerance and ESD protection unmatched by competing CMOS designs. Using only 0.1 μF external capacitors, the circuit consumes only 40mW of power and can operate to 120kbaud even while driving heavy capacitive loads. New ESD structures on the chip allow the LT1381 to survive multiple $\pm 10\text{kV}$ strikes, eliminating the need for costly TransZorbs[®] on the RS232 line pins. Driver outputs are protected from overload and can be shorted to ground or up to $\pm 25\text{V}$ without damage. During power-off conditions, driver and receiver outputs are in a high impedance state, allowing line sharing.

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 TransZorb[®] is a registered trademark of General Instruments, GSI

TYPICAL APPLICATION



Output Waveforms



LT1381 • TA02

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC})	6V
V^+	13.2V
V^-	-13.2V
Input Voltage	
Driver	V^- to V^+
Receiver	-30V to 30V
ON/OFF	-0.3V to 12V
Output Voltage	
Driver	($V^+ - 30V$) to ($V^- + 30V$)
Receiver	-0.3V to ($V_{CC} + 0.3V$)
Short-Circuit Duration	
V^+	30 sec
V^-	30 sec
Driver Output	Indefinite
Receiver Output	Indefinite
Operating Temperature Range	
LT1381C	0°C to 70°C
LT1381I	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW N PACKAGE 16-LEAD PLASTIC DIP S PACKAGE 16-LEAD PLASTIC SOIC $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 90^{\circ}\text{C/W}$, $\theta_{JC} = 46^{\circ}\text{C/W}$ (N) $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 110^{\circ}\text{C/W}$, $\theta_{JC} = 34^{\circ}\text{C/W}$ (S)	ORDER PART NUMBER	
	LT1381CN LT1381CS LT1381IS	

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Generator					
V^+ Output			7.9		V
V^- Output			-7.0		V
Supply Current (V_{CC})	(Note 3), $T_A = 25^{\circ}\text{C}$		8	14 16	mA mA
Supply Rise Time	$C1 = C2 = C3 = C4 = 0.1\mu\text{F}$		0.2		ms
Oscillator Frequency			130		kHz
Driver					
Output Voltage Swing	Load = 3k to GND	Positive Negative	5.0 -6.3	7.5 -5.0	V V
Logic Input Voltage Level	Input Low Level ($V_{OUT} = \text{High}$) Input High Level ($V_{OUT} = \text{Low}$)		2.0	1.4 1.4	0.8 V V
Logic Input Current	$0.8V \leq V_{IN} \leq 2.0V$		5	20	μA
Output Short-Circuit Current	$V_{OUT} = 0V$		9	17	mA
Output Leakage Current	Power Off $V_{OUT} = \pm 15V$		10	100	μA
Data Rate	$R_L = 3k$, $C_L = 2500pF$ $R_L = 3k$, $C_L = 1000pF$		120 250		kBaud kBaud
Slew Rate	$R_L = 3k$, $C_L = 51pF$ $R_L = 3k$, $C_L = 2500pF$		4	15 6	30 V/ μs V/ μs
Propagation Delay	Output Transition t_{HL} High to Low (Note 4) Output Transition t_{LH} Low to High		0.6 0.5	1.3 1.3	μs μs

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver					
Input Voltage Thresholds	Input Low Threshold ($V_{OUT} = \text{High}$)	0.8	1.3		V
	Input High Threshold ($V_{OUT} = \text{Low}$)		1.7	2.4	V
Hysteresis		0.1	0.4	1.0	V
Input Resistance	(Note 6)	3	5	7	k Ω
Output Voltage	Output Low, $I_{OUT} = -1.6\text{mA}$		0.2	0.4	V
	Output High, $I_{OUT} = 160\mu\text{A}$ ($V_{CC} = 5\text{V}$)	3.5	4.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$		-20	-10	mA
	Sourcing Current, $V_{OUT} = 0\text{V}$	10	20		mA
Propagation Delay	Output Transition t_{HL} High-to-Low (Note 5)		250	600	ns
	Output Transition t_{LH} Low-to-High		350	600	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at $V_{CC} = 5\text{V}$, unless otherwise specified.

Note 3: Supply current is measured as the average over several charge pump cycles. $C^+ = C^- = C1 = C2 = 0.1\mu\text{F}$. All outputs are open, with all driver inputs tied high.

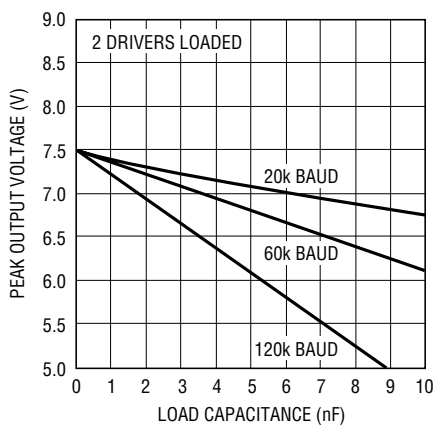
Note 4: For driver delay measurements, $R_L = 3\text{k}$ and $C_L = 51\text{pF}$. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing ($t_{HL} = 1.4\text{V}$ to 0V and $t_{LH} = 1.4\text{V}$ to 0V).

Note 5: For receiver delay measurements, $C_L = 51\text{pF}$. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold ($t_{HL} = 1.3\text{V}$ to 2.4V and $t_{LH} = 1.7\text{V}$ to 0.8V).

Note 6: Tested at $V_{IN} = \pm 10\text{V}$.

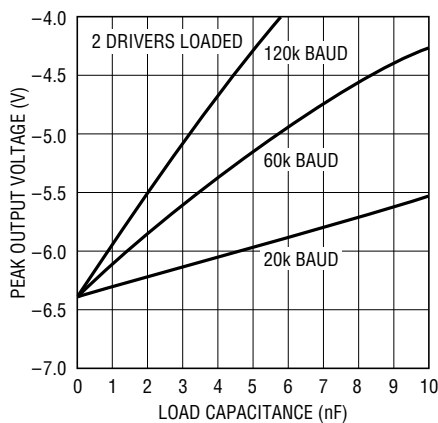
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Maximum Output Voltage vs Load Capacitance



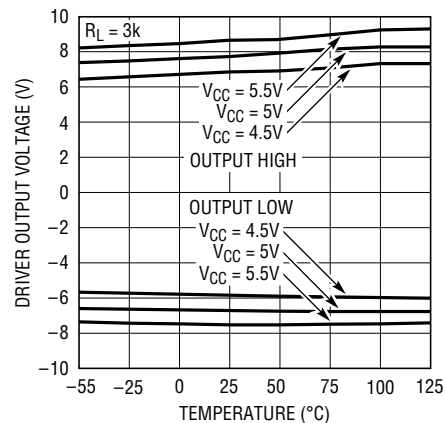
LT1381 • TPC01

Driver Minimum Output Voltage vs Load Capacitance



LT1381 • TPC02

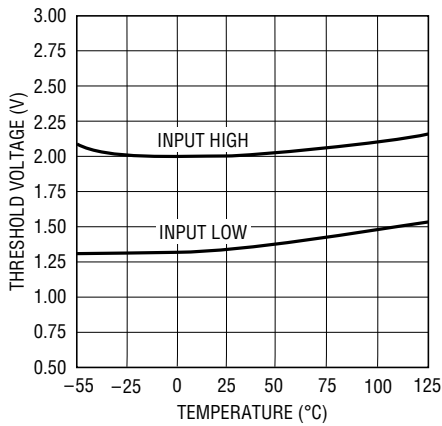
Driver Output Voltage



LT1381 • TPC03

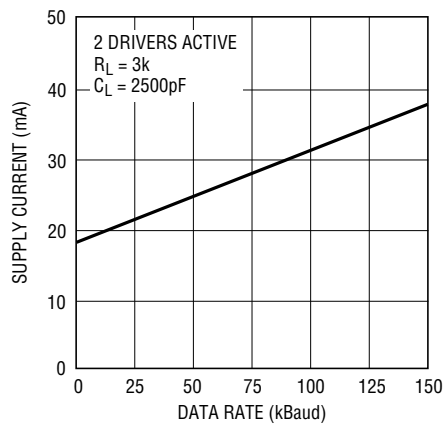
TYPICAL PERFORMANCE CHARACTERISTICS

Receiver Input Threshold



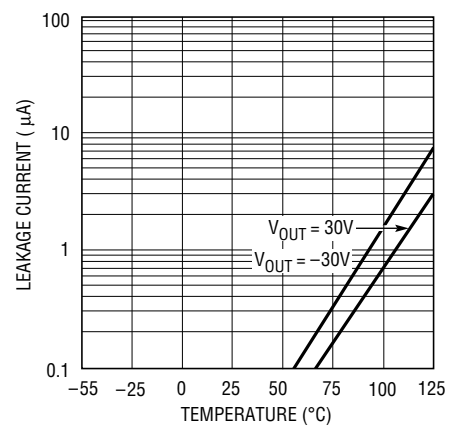
LT1381 • TPC04

Supply Current vs Data Rate



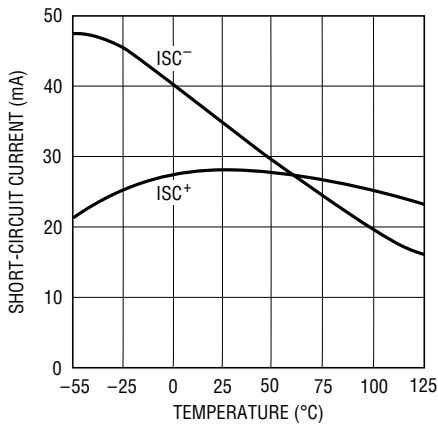
LT1381 • TPC05

Driver Leakage in Shutdown



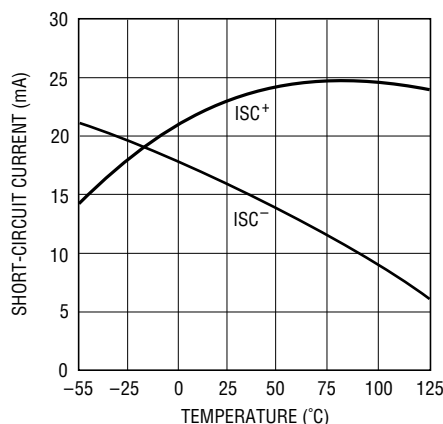
LT1381 • TPC06

Receiver Short-Circuit Current



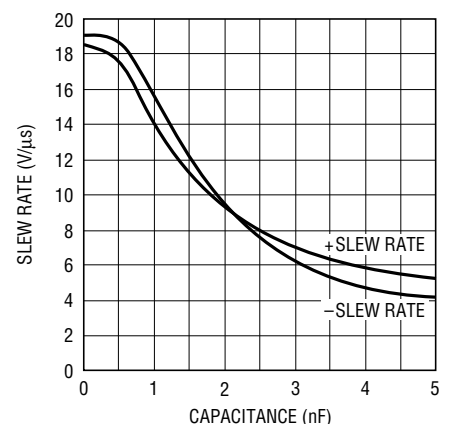
LT1381 • TPC07

Driver Short-Circuit Current



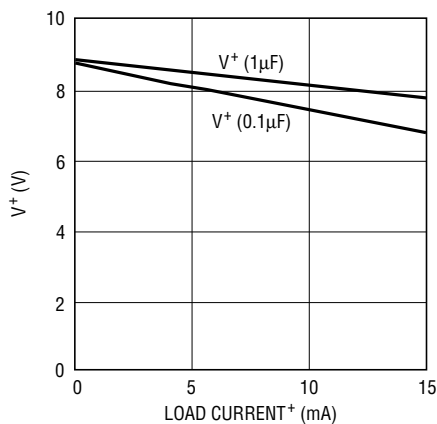
LT1381 • TPC08

Slew Rate vs Load Capacitance



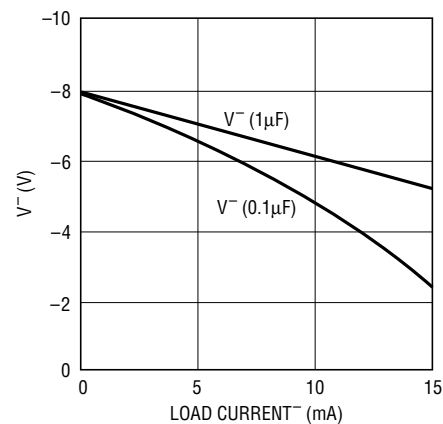
LT1381 • TPC09

V+ Compliance Curve



LT1381 • TPC10

V- Compliance Curve



LT1381 • TPC11

PIN FUNCTIONS

C1⁺, C1⁻, C2⁺, C2⁻ (Pins 1, 3, 4, 5): Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.1\mu\text{F}$: one from C1⁺ to C1⁻ and another from C2⁺ to C2⁻. C1 may be deleted if a separate 12V supply is available and connected to pin C1⁺.

V⁺ (Pin 2): Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5\text{V}$. This pin requires an external charge storage capacitor $C \geq 0.1\mu\text{F}$, tied to ground or V_{CC} . Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V⁺ and V⁻ pins may be paralleled into common capacitors.

V⁻ (Pin 6): Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5\text{V})$. This pin requires an external charge storage capacitor $C \geq 0.1\mu\text{F}$. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V⁺ and V⁻ pins may be paralleled into common capacitors.

TR2 OUT, TR1 OUT (Pin 7, 14): Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when $V_{CC} = 0\text{V}$. Outputs are fully short-circuit protected from $V^- + 25\text{V}$ to $V^+ - 25\text{V}$. Applying

higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to $\pm 10\text{kV}$ for human body model discharges.

REC2 IN, REC1 IN (Pins 8, 13): Receiver Inputs. These pins accept RS232 level signals ($\pm 30\text{V}$) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to $\pm 10\text{kV}$ for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

REC2 OUT, REC1 OUT (Pins 9, 12): Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are fully short-circuit protected to ground or V_{CC} with the power ON or OFF.

TR2 IN, TR1 IN (Pins 10, 11): RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC} .

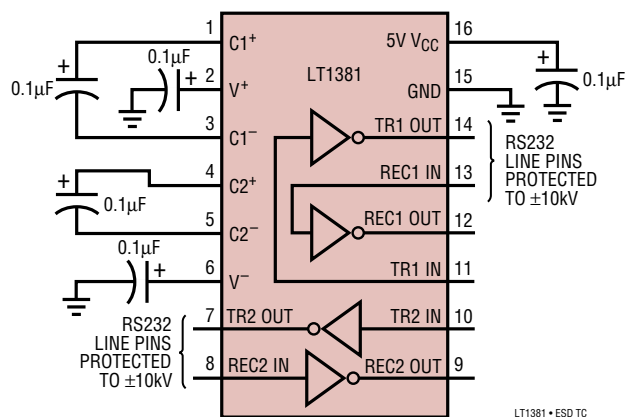
GND (Pin 15): Ground Pin.

V_{CC} (Pin 16): 5V Input Supply Pin. This pin should be decoupled with a $0.1\mu\text{F}$ ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

ESD PROTECTION

The RS232 line inputs of the LT1381 have on-chip protection from ESD transients up to $\pm 10\text{kV}$. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the circuit must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC} , V⁺, V⁻ and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit



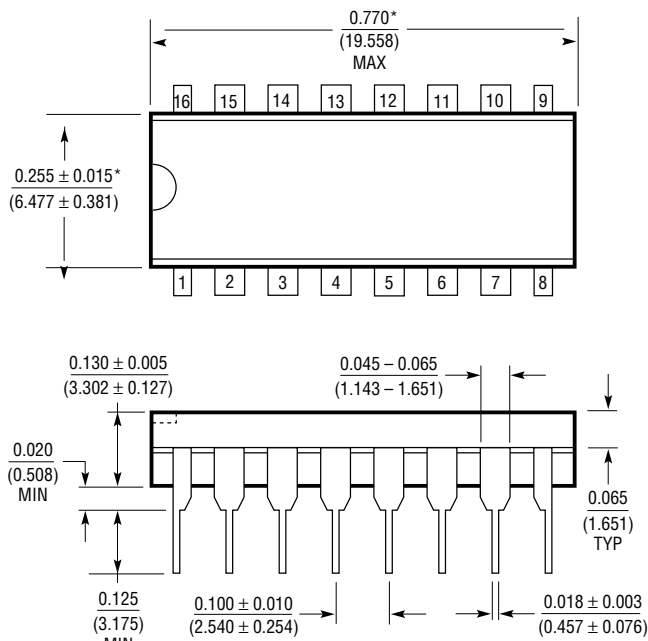
LT1381 • ESD TC

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PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

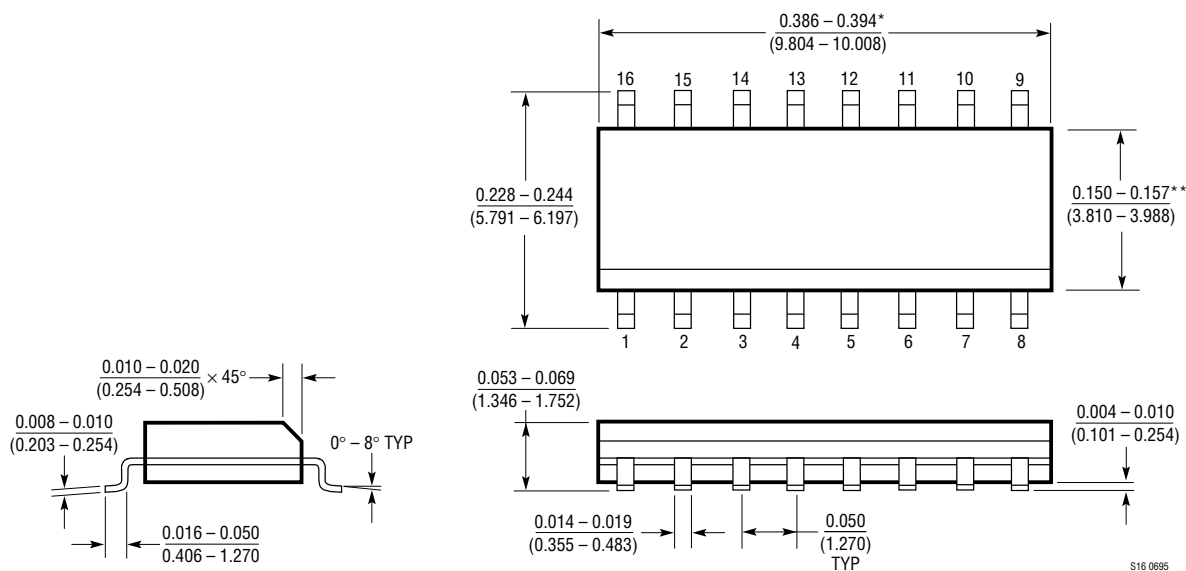
N Package 16-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1197

S Package 16-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S16 0695

The figure contains two circuit diagrams for the LT1381, a monolithic RS232 interface.

Left Diagram (Full Interface): This diagram shows the LT1381 with its full set of pins.

- Power:** Pin 16 is connected to 5V VCC. Pins 2 and 6 are connected to ground. A 0.1µF capacitor is connected between pins 2 and 6.
- RS232 Signals:**
 - Pin 14 (RS232 OUTPUT) is connected to pin 11 (TTL INPUT).
 - Pin 7 (RS232 OUTPUT) is connected to pin 10 (TTL INPUT).
 - Pin 13 (RS232 INPUT) is connected to pin 12 (TTL OUTPUT) through a 5kΩ resistor.
 - Pin 8 (RS232 INPUT) is connected to pin 9 (TTL OUTPUT) through a 5kΩ resistor.
- Capacitors:** Decoupling capacitors C1+ (pin 1), C1- (pin 3), C2+ (pin 4), and C2- (pin 5) are connected to ground. A 0.1µF capacitor is connected between pins 1 and 3, and another 0.1µF capacitor is connected between pins 4 and 5.

Right Diagram (Simplified Interface): This diagram shows a simplified version of the LT1381 interface.

- Power:** Pin 16 is connected to 5V VCC. Pins 2 and 6 are connected to ground. A 0.1µF capacitor is connected between pins 2 and 6.
- RS232 Signals:**
 - Pin 14 (RS232 OUTPUT) is connected to pin 11 (TTL INPUT).
 - Pin 7 (RS232 OUTPUT) is connected to pin 10 (TTL INPUT).
 - Pin 13 (RS232 INPUT) is connected to pin 12 (TTL OUTPUT).
 - Pin 8 (RS232 INPUT) is connected to pin 9 (TTL OUTPUT).
- Capacitors:** Decoupling capacitors C1+ (pin 1), C1- (pin 3), C2+ (pin 4), and C2- (pin 5) are connected to ground. A 0.1µF capacitor is connected between pins 1 and 3, and another 0.1µF capacitor is connected between pins 4 and 5.

PART NUMBER	DESCRIPTION	COMMENTS
LT1180A/LT1181A	5V 2-Driver/2-Receiver RS232 Transceivers	Pin Compatible with LT1280A/LT1280A
LT1280A/LT1281A	5V 2-Driver/2-Receiver RS232 Transceivers	Pin Compatible with LT1180A/LT1181A
LT1780/LT1781	5V 2-Driver/2-Receiver RS232 Transceivers	IEC 1000-4-2 Level 4 Compliance