PLESSEY
Semiconductors

ZN501AJ/ZN502E/CJ

T-51-10-10

10-BIT MICROPROCESSOR COMPATIBLE A-D CONVERTERS

The ZN501 and ZN502 range of successive approximation A-D converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip consists of a current switching array (requiring no trim), successive approximation logic, 2.5V precision reference, reference amplifier, comparator and three-state output buffers.

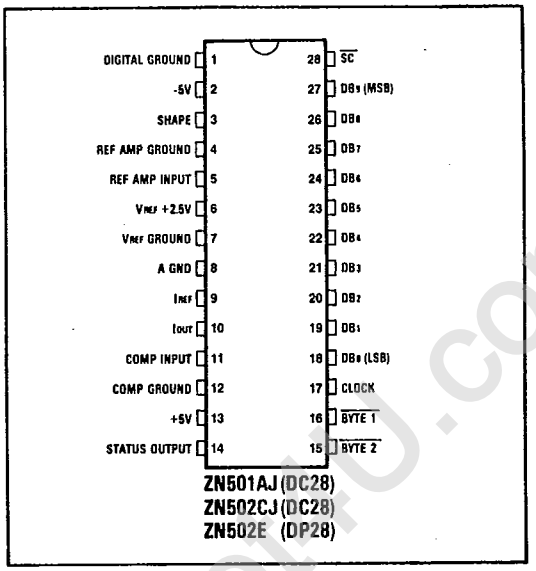
With the aid of $\overline{\text{BYTE 1}}$ and $\overline{\text{BYTE 2}}$ the 10 bits of O/P data can be read as a 10-bit word or as 8- and 2-bit words.

FEATURES

- Choice of Linearity: ½ LSB - ZN501, 1 LSB ZN502
- Three-State Outputs, TTL Compatible
- 15 microseconds Typical, 20 microseconds Guaranteed Conversion Time
- Input Range as Desired
- Asynchronous $\overline{\text{START CONVERT}}$
- +5V, -5V Supplies, Microprocessor and TTL/CMOS Compatible
- Commercial or Military Temperature Ranges
- Full 8- or 16-Bit MICRO-Bus Interface
- Available in Ceramic or Moulded Package

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN502E	0°C to +70°C	DP28
ZN502CJ	0°C to +70°C	DC28
ZN501AJ	-55°C to +125°C	DC28



ZN501AJ (DC28)
ZN502CJ (DC28)
ZN502E (DP28)

Pin connections - top view

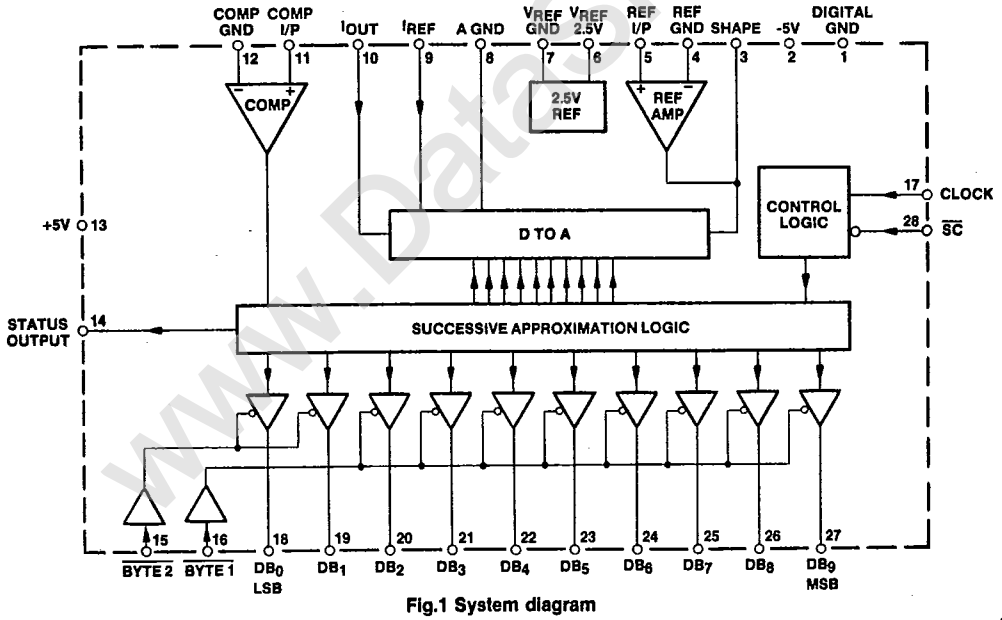


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc+	+7V
Supply voltage Vcc-	-7V
Logic input voltage	+Vcc and 0V
Operating temperature range	0°C to 70°C (ZN502E, ZN502CJ) -55°C to +125°C (ZN501AJ)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at +5 and −5V supplies and internal reference unless otherwise specified).

Parameter	Version	T_{amb} = +25°C Min.	Typ.	Max.	Over Spec Min.	Max.	Units	Conditions
	ZN501AJ							
Linearity error				±0.5		±0.5	LSB	
Diff. linearity error				±0.75		±0.75	LSB	Note 1
Unipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Bipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Gain error			±0.55				LSB	Ext. Ref.*
			±3				LSB	Int. Ref.*
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			7 typ., 10 max.				ppm/°C	Ext. Ref.
			7 typ., 10 max.				ppm/°C	Int. Ref.
Bipolar offset			7 typ., 10 max.				ppm/°C	Ext. Ref.
			7 typ., 10 max				ppm/°C	Int. Ref.
Gain			10 typ.				ppm/°C	Ext. Ref.
			50 typ.				ppm/°C	Int. Ref.
	ZN502CJ							
Linearity error				±1.0		±1.0	LSB	
Diff. linearity error				±1.0		±1.0	LSB	Note 1
Unipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Bipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Gain error			±0.55				LSB	Ext. Ref.*
			±3				LSB	Int. Ref.*

*See note 4

ELECTRICAL CHARACTERISTICS (Cont.) PLESSEY SEMICONDUCTORS T-51-10-10

Parameter	Version	T_{amb} = +25°C Min.	Typ.	Max.	Over Spec Min.	Max.	Units	Conditions
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			15 typ., 20 max.				ppm/°C	Ext. Ref.
			15 typ., 20 max.				ppm/°C	Int. Ref.
Bipolar offset			15 typ., 20 max.				ppm/°C	Ext. Ref.
			15 typ., 20 max.				ppm/°C	Int. Ref.
Gain			20 typ.				ppm/°C	Ext. Ref.*
			50 typ.				ppm/°C	Int. Ref.*
	ZN502E	Parameter values as for ZN502CJ						
	All types							
Resolution		10	–	–	–	–	bits	
Conversion time (min)		10	15	20	15	20	µs	Note 2
DAC reference I_{ref}		0.25	0.5	1.0	0.25	1.0	mA	Note 5
Nominal analogue input range		−2.5	–	+2.5	–	–	V	Note 3
Supply rejection		–	0.1	–	–	–	% per V	
Supply voltage $+V_{CC}$		+4.5	+5	+5.5	+4.5	+5.5	V	
$-V_{CC}$		−4.5	−5	−5.5	−4.5	−5.5	V	
Supply current $+I_{CC}$		–	30	40	–	–	mA	$+V_{CC}$ = +5V
$-I_{CC}$		–	21	28	–	–	mA	$-V_{CC}$ = −5V
Power consumption		–	255	340	–	–	mW	
INTERNAL VOLTAGE REFERENCE								
Output voltage	All types	–	2.480	–	–	–	V	
Output voltage tolerance	ZN501AJ	–	–	±3.0	–	–	%	
	ZN502CJ	–	–	±5.0	–	–	%	
	ZN502E	–	–	±5.0	–	–	%	
V_{REF} temp. coeff.	All types	–	–	–	26	50	ppm/°C	
Slope impedance		–	0.75	–	–	–	Ω	
Max. load current		–	±2.0	–	–	–	mA	
LOGIC	All types							
$\overline{START\ CONVERT}$ SC								
High level inpV V_{ih}		2.0	–	–	2.0	–	V	
Low level inpV V_{il}		–	–	0.8	–	0.8	V	
High level inpl I_{ih}		–	18.0	–	–	–	µA	V_{CC} = ±5.5V V_{in} = 5.5V
High level inpl I_{ih}		–	8.0	–	–	–	µA	V_{CC} ±5.5V V_{in} = 2.4V
Low level inpl I_{il}		–	4.0	–	–	–	µA	V_{CC} ±5.5V V_{in} +0.4V

*See note 4

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Version	$T_{amb} = +25°C$ Min.	Typ.	Max.	Over Spec Min.	Max.	Units	Conditions
LOGIC	All types							
$\overline{BYTE}$ 1 and 2								
High level inpV V_{ih}		2.0	–	–	2.0	–	V	
Low level inpV V_{il}		–	–	0.8	–	0.8	V	
High level inpl I_{ih}		–	18.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$
High level inpl I_{ih}		–	12.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 2.4V$
Low level inpl I_{il}		–	2.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 0.4V$
CLOCK	All types							
CLOCK high period		0.5	–	–	–	–	μs	
Max. clock frequency		550	730	1100	550	730	KHz	
High level inpV V_{ih}		2.0	–	–	2.0	–	V	
Low level inpV V_{il}		–	–	0.8	–	0.8	V	
High level inpl I_{ih}		–	15.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$
High level inpl I_{ih}		–	5.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 2.4V$
Low level inpl I_{il}		–	3.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 0.4V$
High level OPV V_{oh}	All types	2.4	–	–	2.4	–	V	$V_{CC} = \pm 5V$
Low level OPV V_{ol}		–	–	0.4	–	0.4	V	
High level OPI I_{oh}		–	–	−700	–	–	μA	
Low level OPI I_{ol}		–	–	2.0	–	–	mA	
Three-state DISABLE output leakage		–	–	±2.0	–	–	μA	$V_{out} = 1.3V$
$\overline{BYTE}$ input to data output delays		–	200	260	–	–	ns	
ENABLE/DISABLE								
Delay time TE1		100	220	260	–	–	ns	Note 6
TEO		60	80	100	–	–	ns	
TD1		100	120	140	–	–	ns	
TDO		30	60	100	–	–	ns	
$\overline{SC}$ pulse width		100	–	–	–	–	ns	
$\overline{SC}$ input to STATUS		–	180	–	–	–	ns	

Note 1 No missing codes over full temperature range at appropriate accuracy.

Note 2 The maximum conversion time is 20μs. This corresponds to a clock rate of 550KHz based on 11 clock periods per conversion cycle (see timing diagram). This provides an update rate of 50KHz.

Note 3 Single polarity and other input ranges may be provided by different input resistor values.

Note 4 Gain error is trimmable to zero with the aid of R3.

Note 5 The full scale D-A output current $I_{out} = 4$ times I_{ref}. For optimum performance $I_{ref} = 0.5mA$.

Note 6 Refer to Fig. 9.

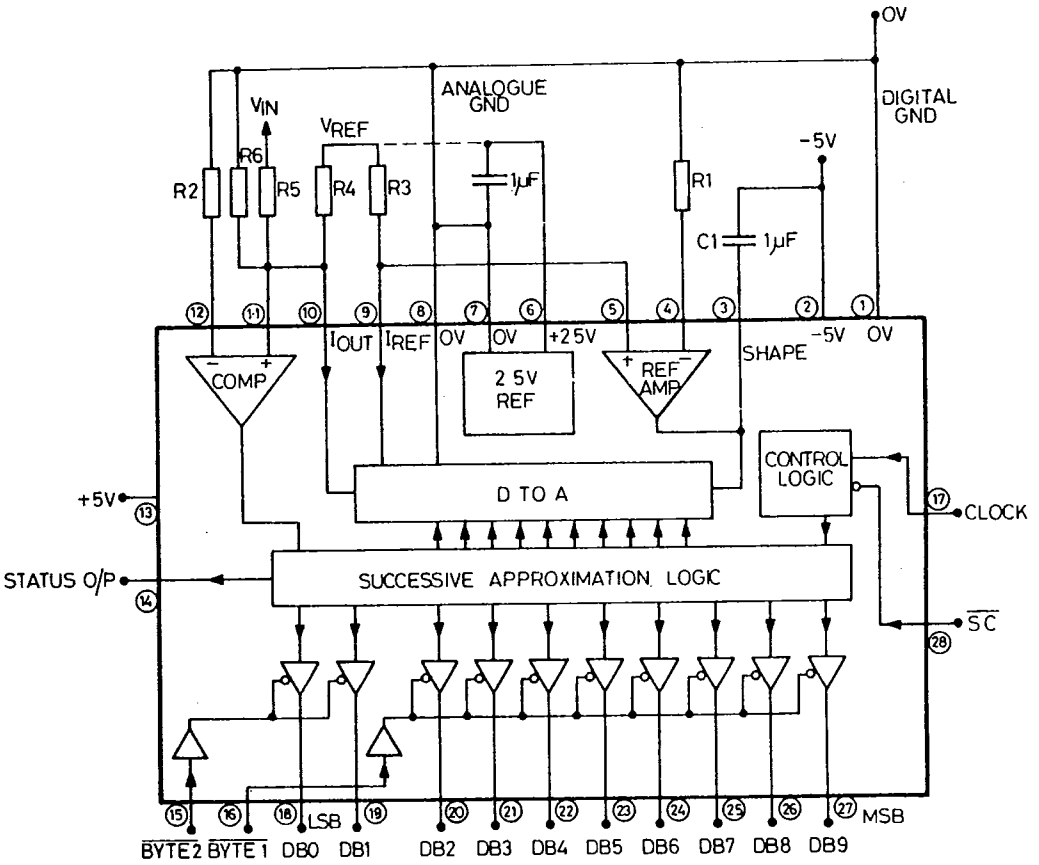


Fig. 2 Typical external components

GENERAL CIRCUIT OPERATION

The ZN501 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{SC}$ input the STATUS output goes low, and the D-A converter input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. So if the analogue input is the larger, the MSB is left in circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all the 10-bits have been compared. On the 11th negative clock edge STATUS goes high indicating that the conversion is complete.

During a conversion $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 will normally be held high to keep the 3-state buffers in their high impedance state. Data can be read out by taking either $\overline{BYTE}$ 1 or $\overline{BYTE}$ 2 low, thus enabling the three-state outputs. $\overline{BYTE}$ 1 controls the 8 MSB's and $\overline{BYTE}$ 2 controls the 2 LSB's. Readout is non-destructive.

CONVERSION TIMING

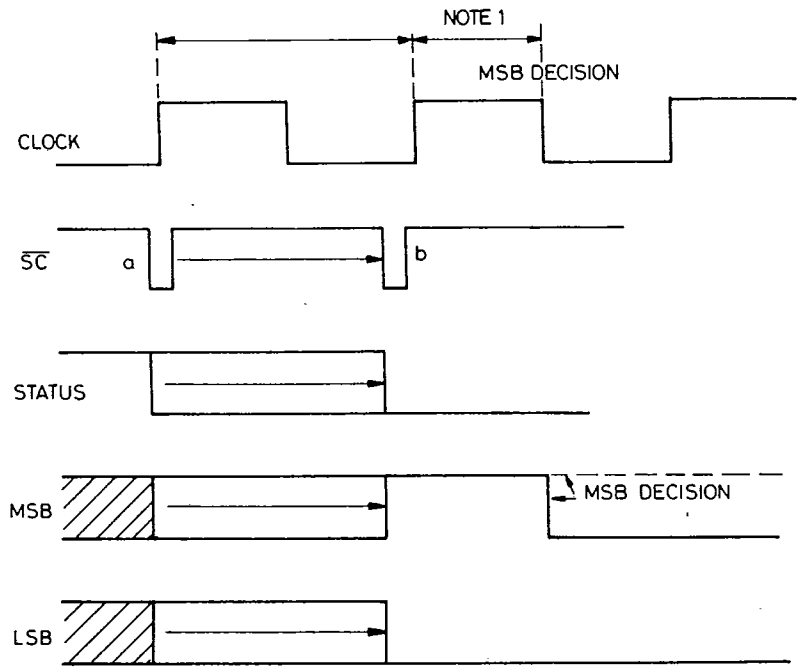
The ZN501 will accept a low-going $\overline{\text{START CONVERT}}$ pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 10.5 and 11.5 clock pulses later depending on the relative timing of the CLOCK and $\overline{\text{START CONVERT}}$ signals.

The converter is cleared by a low-going $\overline{\text{START CONVERT}}$ pulse, which sets the most significant bit and resets all the other bits and STATUS. Whilst the $\overline{\text{START CONVERT}}$ input is low the MSB output of the D-A converter is continuously compared with the analogue input, but otherwise the converter is inhibited. After the $\overline{\text{START CONVERT}}$ input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The $\overline{\text{SC}}$ pulse can be as short as 100ns; however the MSB must be allowed to settle for at least (625ns) before the MSB decision is made. To ensure that this criterion is met even with short $\overline{\text{SC}}$ pulses the converter waits, after the $\overline{\text{SC}}$ input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or (625ns) at maximum clock frequency. The clock high period and the $\overline{\text{SC}}$ pulse width must comply with this settling time i.e. clock high period + $\overline{\text{SC}}$ pulse width $\geqslant$625ns.

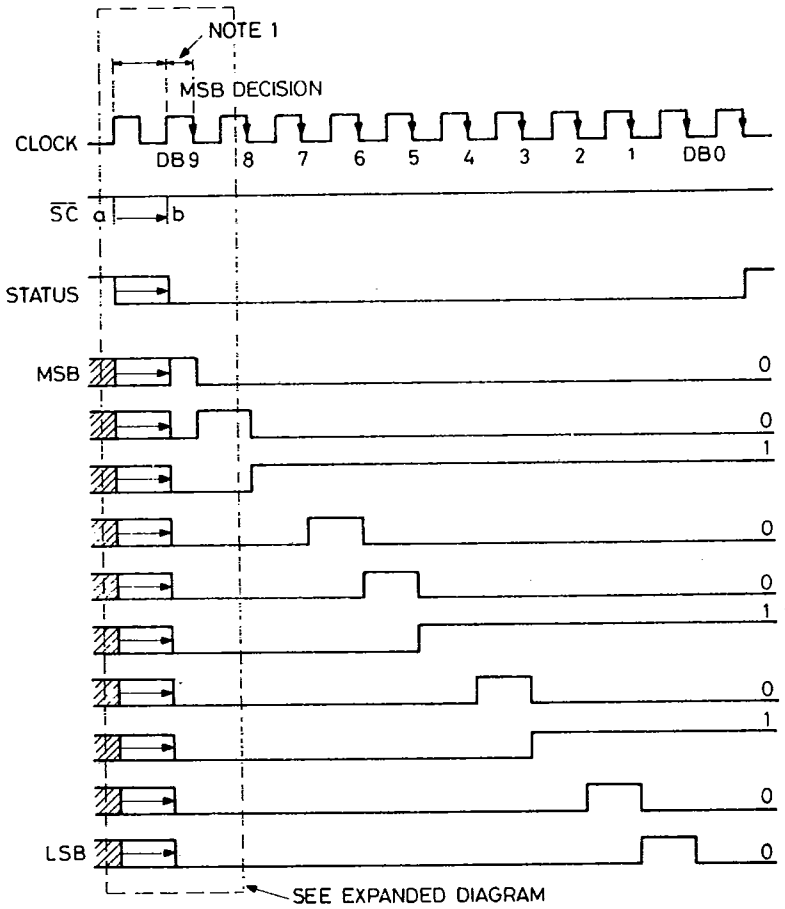
During a conversion the $\overline{\text{SC}}$ input is not locked out and if it is pulsed low at any time the conversion will restart.

At the end of a conversion STATUS waits 1 clock cycle before going high, so indicating that data is valid. The data outputs can be thus enabled anytime during a conversion and valid data will be available on the rising edge of the STATUS signal.



(Expanded inset)

Fig. 3 Expanded timing diagram



NOTE 1 GUARANTEED PERIOD OF ½ CLOCK CYCLE MIN
1½ CLOCK CYCLES MAX.
ALLOWS MSB TO SETTLE BEFORE MSB DECISION

Fig. 4 Timing diagram

CONTINUOUS CONVERSION

The converter can be made to cycle by inverting the STATUS output and feeding back to the $\overline{SC}$ input. To ensure that the converter starts reliably after power up an initial start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied.

The propagation delay of the NOR gate determines the period over which STATUS remains high, during which time the data can be stored into latches. The time available for storing the data can be increased by inserting delays into the inverter path.

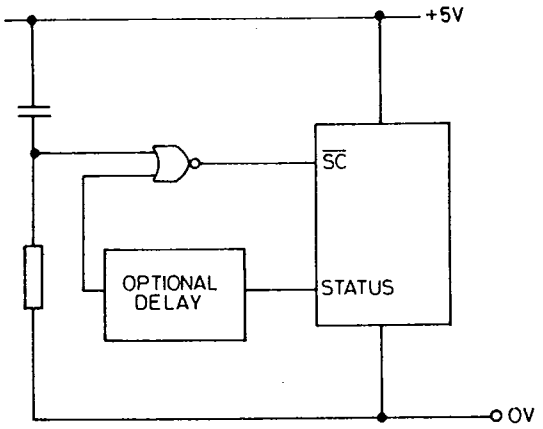


Fig. 5 Circuit for continuous conversion

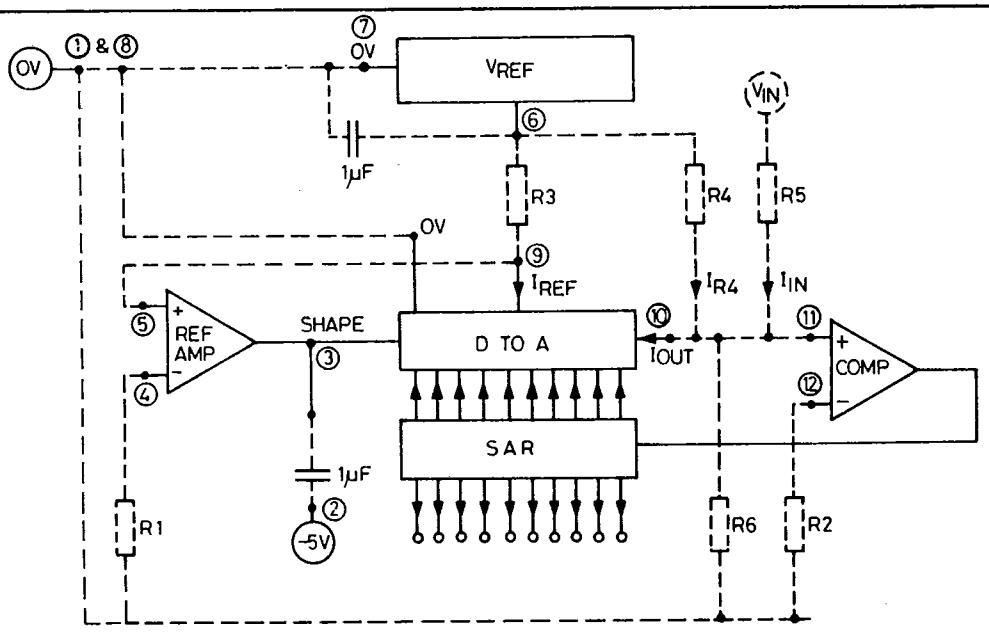


Fig. 6 External component connections

CALCULATION OF EXTERNAL RESISTORS

If $V_{in\ max}$ is the voltage for the logic output to be all 1's.

$V_{in\ min}$ is the voltage for the logic output to be all 0's.

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$$I_{out} = I_{R4} + I_{in}$$

$$I_{out} = \frac{V_{ref}}{R4} + \frac{V_{in}}{R5}$$

$I_{out} = 0$ (When $V_{in} = V_{in\ min}$)

$$\frac{V_{in\ min}}{R5} = -\frac{V_{ref}}{R4}$$

$$R4 = -\frac{V_{ref}\ R5}{V_{in\ min}}$$

I_{out}(f.s.) = 2mA: (When $V_{in} = V_{in\ max}$)

$$\frac{V_{in\ max}}{R5} + \frac{V_{ref}}{R4} = I_{out}(f.s.)$$

$$-\frac{V_{in\ min}}{R5} + \frac{V_{in\ max}}{R5} = I_{out}(f.s.)$$

$$R5 = \frac{V_{in\ max} - V_{in\ min}}{I_{out}(f.s.)}$$

It is important for gain stability that I_{out}(f.s.) of 2mA be kept constant, and this is done by the reference amplifier loop.

The current sources in the D-A itself cannot be checked directly so a number of reference current sources are distributed across the chip to monitor conditions all along the array.

So I_{ref} = 0.5mA

$$R3 = \frac{V_{ref}}{0.5mA}$$

I_{out}(f.s.) is four times I_{ref}.

R3 can affect gain stability and thus requires to be of high quality.
(Also slight variation in its value can act as a gain control).

R4 and R5 can affect offset stability and thus requires to be of high quality.
(Also slight variations in the value of R4 can act as an offset control).

R1 and R2 supply the bias currents of the reference amplifier and comparator.

So R1 = R3

and R2 = parallel combination of R4, R5 and R6

R6 should be chosen such that the parallel combination of R4, R5 and R6 is about 1.25KΩ as this determines the D-A time constant and hence conversion time.

(THE FOLLOWING IS A TABLE OF VALUES TO GIVE EXAMPLES OF THE ABOVE EQUATIONS):

$V_{in\ max}$	$V_{in\ min}$	V_{ref}	R1 (1)	R2 (1)	R3	R4	R5	R6 (1)
+2.5	2.5	2.5	5K	1.25K	5K	2.5K	2.5K	∞
+2.5	2.5	5*	10K	1.25K	10K	5.0K	2.5K	5.0K
+2.5	0	2.5	5K	1.25K	5K	∞	1.25K	∞
+5.0	0	2.5	5K	1.25K	5K	∞	2.5K	2.5K
+4.0	2.0	2.5	5K	1.25K	5K	3.75K	3.0K	5.0K
+4.0	2.0	12*	24K	1.25K	24K	3.75K	3.0K	5.0K
+10	10	2.5	5K	1.25K	5K	2.5K	10K	3.33K
+10	0	2.5	5K	1.25K	5K	∞	5K	1.66K

Note 1 Nearest prefered value may be used for R1, R2 and R6
*Note 2 External reference.

For unipolar operation where R4 approaches (∞) and a zero adjustment is required, the following offset circuit is suggested in place of R4.

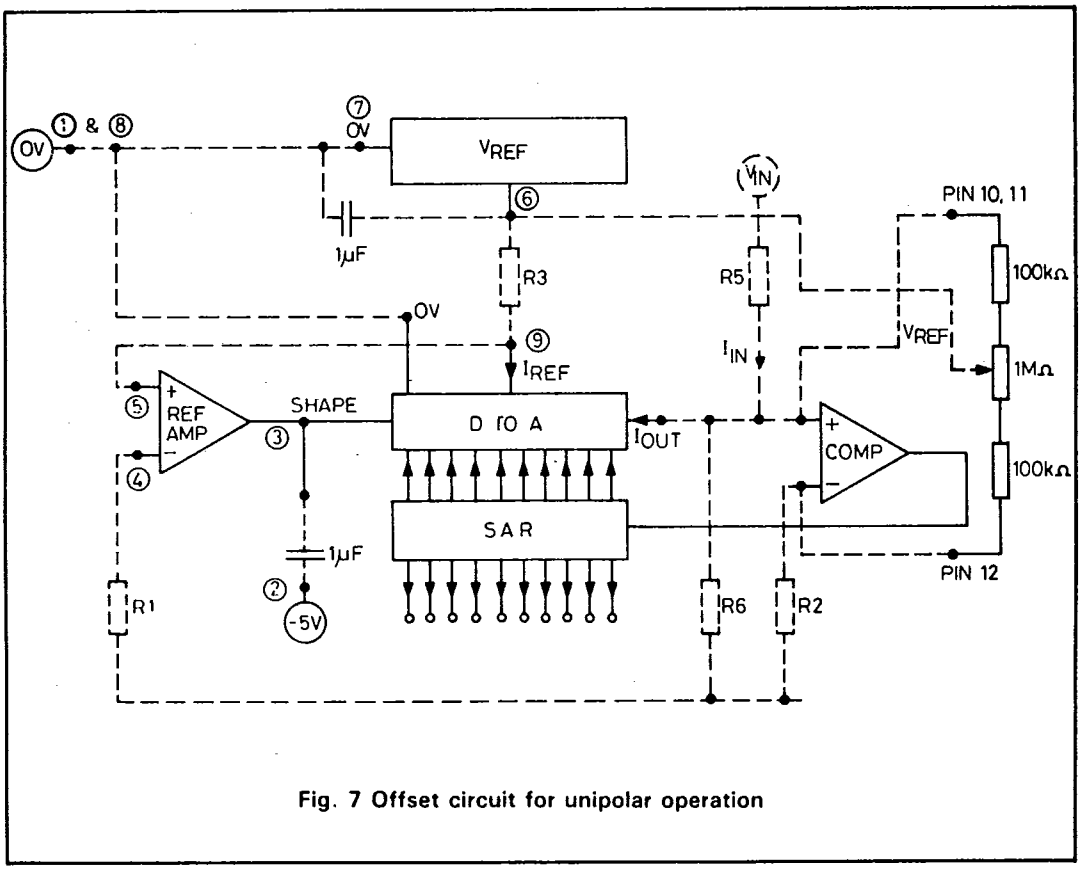


Fig. 7 Offset circuit for unipolar operation

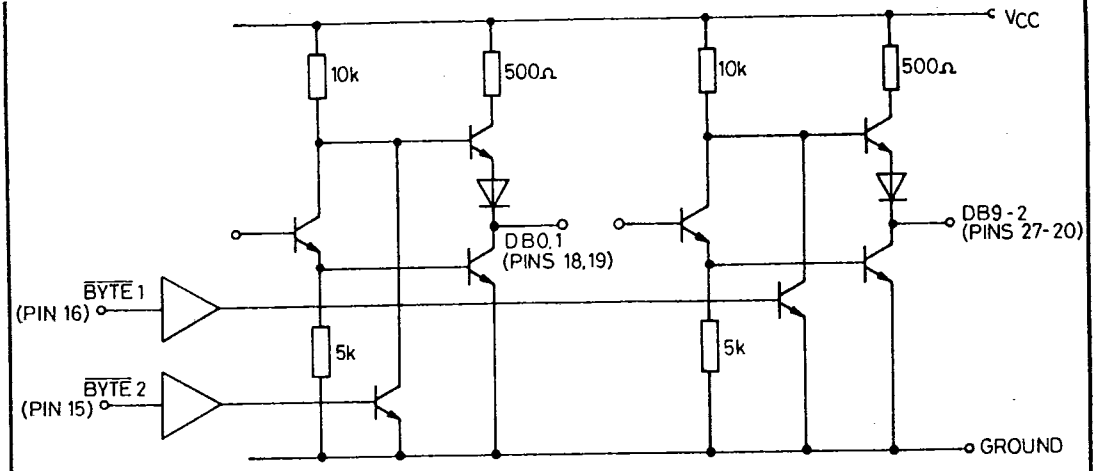
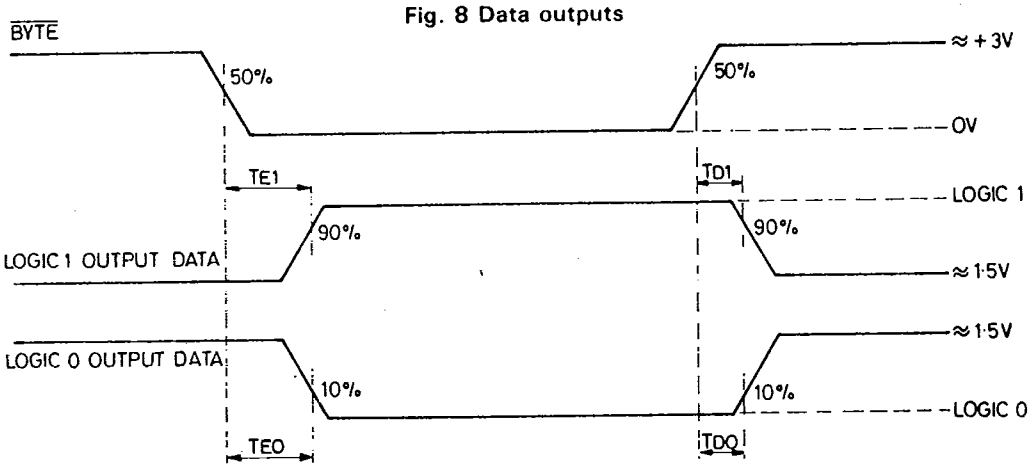


Fig. 8 Data outputs



TE = BYTE ENABLE DELAY TIME (CL = 50pF)
TD = BYTE DISABLE DELAY TIME (CL = 10pF)

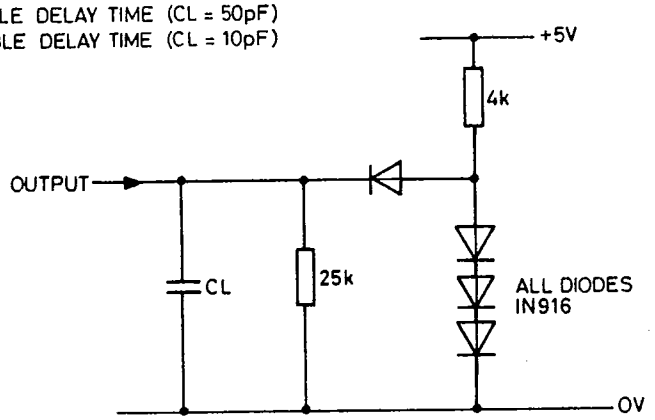


Fig. 9 Output enable/disable delays

DATA OUTPUTS

The ZN501 has true three-state output buffers on chip, hence eliminating the need for external buffers and latch circuitry.

The two $\overline{\text{BYTE}}$ select pins $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2, control outputs DB9 to DB2, and outputs DB1 to DB0 respectively.

$\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 will normally be held high during a conversion to keep the three-state buffers in their high impedance state, and when data is ready, which will be signalled by a high going STATUS pulse, it can easily be read out by taking $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 low.

(A test circuit and timing diagram for the output enable/disable delays are given).

The STATUS output shown utilises a 5K internal pullup resistor for CMOS/TTL compatibility.

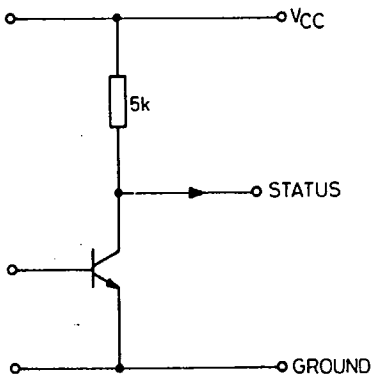


Fig. 10 Status output

DATA BUS CONNECTIONS

The ZN501 can be connected directly to an 8-bit microprocessor bus, where the two LSB's would normally be hardwired to the desired upper bits, usually the 2 MSB's. Hence the data would be transferred in two words with control of them, from $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2.

For use with a 16-bit microprocessor, $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 would be tied together and all 10 bits would be enabled simultaneously. The 10-bit word could then be placed at either the higher or lower end of the 16-bit bus.

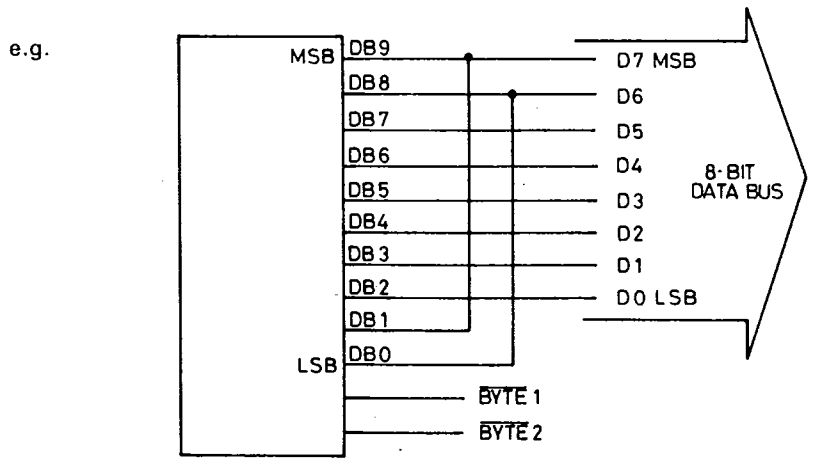


Fig. 11 Data bus connections

$\overline{\text{BYTE}}$ 1	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
	D7	D6	D5	D4	D3	D2	D1	D0
$\overline{\text{BYTE}}$ 2	DB1	DB0	X	X	X	X	X	X

DATA TRANSFERRED IN TWO WORDS

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UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{\text{START CONVERT}}$ pulse at intervals long enough to allow a complete conversion and monitor the digital outputs.

OFFSET SETTING

(ii) Apply ½LSB to V_{in} and adjust the offset CIRCUIT until DBO (LSB) just flickers between 0 and 1 with all the other bits at 0.
i.e. for transition 0000000000 to 0000000001.

GAIN SETTING

(iii) Apply full-scale minus 1.½LSB to V_{in} and adjust gain until DBO (LSB) just flickers between 0 and 1 with all other bits at 1.
i.e. for transition 1111111111 to 1111111110.

Note: R3 GAIN ADJUSTMENT.

UNIPOLAR SETTING-UP POINTS

Input range +FS	½LSB	F.S. – 1.½LSB
+2.5V	1.22mV	2.4963V
+5.0V	2.441mV	4.9926V

$1LSB = \frac{FS}{1024}$

UNIPOLAR LOGIC CODING

Analogue input (Nominal code centre value)	Digital output code MSB LSB
FS - 1LSB	1111111111
FS - 2LSB	1111111110
¾.FS	1100000000
½.FS + LSB	1000000001
½.FS	1000000000
½.FS - 1LSB	0111111111
¼.FS	0100000000
1LSB	0000000001
0	0000000000

BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{\text{START CONVERT}}$ pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

OFFSET SETTING

(ii) Apply −(FS - ½.LSB) to V_{in} and adjust offset control until DBO (LSB) output just flickers between 0 and 1 with all other bits at 0.
i.e. for transistions 0000000000 to 0000000001.

Note: R4 OFFSET ADJUSTMENT.

GAIN SETTING

(iii) Apply +(FS - 1½.LSB) to V_{in} and adjust gain until DBO (LSB) just flickers between 0 and 1 with all other bits at 0.
i.e. for transition 1111111111 to 1111111110.

Note: R3 GAIN ADJUSTMENT.

BIPOLAR SETTING-UP POINTS

Input range ±FS	−(FS − ½.LSB)	+(F.S. − 1.½.LSB)
±2.5V	−2.4976V	+2.4927V
±5.0V	−4.9951V	+4.9854V

$$1LSB = \frac{2FS}{1024}$$

BIPOLAR LOGIC CODING

Analogue input (Nominal code centre value)	Digital output code MSB LSB
+(FS - 1LSB)	1111111111
+(FS - 2LSB)	1111111110
+(½.FS)	1100000000
+(1LSB)	1000000001
0	1000000000
-(1LSB)	0111111111
-(½.FS)	0100000000
-(FS - 1LSB)	0000000001
-FS	0000000000