



# M48T58 M48T58Y

## 5.0V, 64 Kbit (8 Kb x 8) TIMEKEEPER<sup>®</sup> SRAM

### FEATURES SUMMARY

- INTEGRATED, ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- BYTEWIDE<sup>™</sup> RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES, and SECONDS
- FREQUENCY TEST OUTPUT FOR REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES ( $V_{PFD}$  = Power-fail Deselect Voltage):
  - M48T58:  $V_{CC} = 4.75$  to  $5.5V$   
 $4.5V \leq V_{PFD} \leq 4.75V$
  - M48T58Y:  $V_{CC} = 4.5$  to  $5.5V$   
 $4.2V \leq V_{PFD} \leq 4.5V$
- SELF-CONTAINED BATTERY and CRYSTAL IN THE CAPHAT<sup>™</sup> DIP PACKAGE
- PACKAGING INCLUDES a 28-LEAD SOIC and SNAPHAT<sup>®</sup> TOP (to be Ordered Separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT HOUSING CONTAINING THE BATTERY and CRYSTAL
- PIN and FUNCTION COMPATIBLE WITH JEDEC STANDARD 8 Kb x 8 SRAMs

Figure 1. 28-pin PCDIP, CAPHAT<sup>™</sup> Package

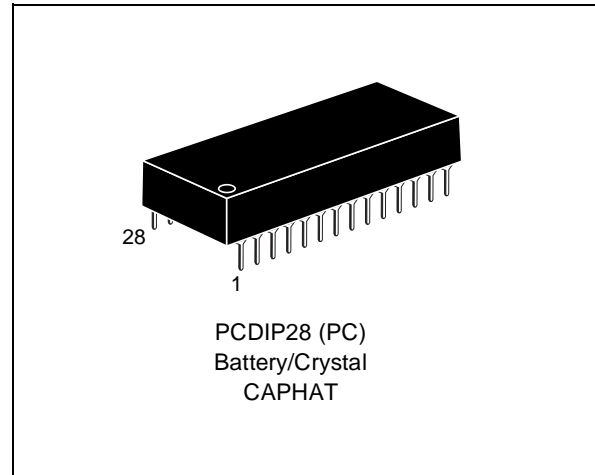
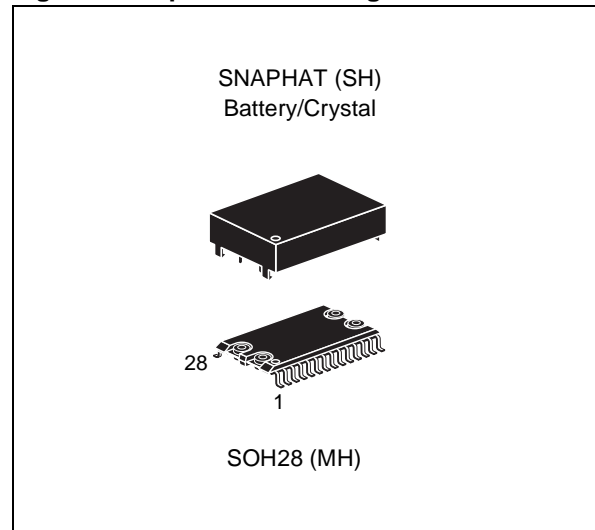


Figure 2. 28-pin SOIC Package



**TABLE OF CONTENTS**

**SUMMARY DESCRIPTION** ..... **4**

- Logic Diagram (Figure 3.) ..... 4
- Signal Names (Table 1.) ..... 4
- DIP Connections (Figure 4.) ..... 5
- SOIC Connections (Figure 5.) ..... 5
- Block Diagram (Figure 6.) ..... 5

**MAXIMUM RATING** ..... **6**

- Absolute Maximum Ratings (Table 2.) ..... 6

**DC AND AC PARAMETERS** ..... **7**

- Operating and AC Measurement Conditions (Table 3.) ..... 7
- AC Measurement Load Circuit (Figure 7.) ..... 7
- Capacitance (Table 4.) ..... 7
- DC Characteristics (Table 5.) ..... 8

**OPERATION MODES** ..... **9**

- Operating Modes (Table 6.) ..... 9
- READ Mode ..... 10
- READ Mode AC Waveforms (Figure 8.) ..... 10
- READ Mode AC Characteristics (Table 7.) ..... 11
- WRITE Mode ..... 12
- WRITE Enable Controlled, WRITE AC Waveform (Figure 9.) ..... 12
- Chip Enable Controlled, WRITE AC Waveforms (Figure 10.) ..... 13
- WRITE Mode AC Characteristics (Table 8.) ..... 14
- Data Retention Mode ..... 15
- Power Down/Up Mode AC Waveforms (Figure 11.) ..... 15
- Power Down/Up AC Characteristics (Table 9.) ..... 16
- Power Down/Up Trip Points DC Characteristics (Table 10.) ..... 16

|   |           |
|---|-----------|
| <b>CLOCK OPERATIONS</b> .....                             | <b>17</b> |
| Reading the Clock .....                                   | 17        |
| Register Map (Table 11.) .....                            | 17        |
| Setting the Clock .....                                   | 17        |
| Stopping and Starting the Oscillator .....                | 17        |
| Calibrating the Clock .....                               | 18        |
| Battery Low Flag .....                                    | 19        |
| Century Bit .....   | 19        |
| Crystal Accuracy Across Temperature (Figure 12.) .....    | 19        |
| Clock Calibration (Figure 13.) .....                      | 20        |
| V <sub>CC</sub> Noise And Negative Going Transients ..... | 20        |
| Supply Voltage Protection (Figure 14.) .....              | 20        |
| <b>PART NUMBERING</b> .....                               | <b>21</b> |
| SNAPHAT Battery Table (Table 13.) .....                   | 21        |
| <b>PACKAGE MECHANICAL INFORMATION</b> .....               | <b>22</b> |
| <b>REVISION HISTORY</b> .....                             | <b>26</b> |

## M48T58, M48T58Y

### SUMMARY DESCRIPTION

The M48T58/Y TIMEKEEPER<sup>®</sup> RAM is a 8Kb x 8 non-volatile static RAM and real time clock. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

The M48T58/Y is a non-volatile pin and function equivalent to any JEDEC standard 8Kb x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITES that can be performed.

The 28-pin, 600mil DIP CAPHAT<sup>™</sup> houses the M48T58/Y silicon with a quartz crystal and a long life lithium button cell in a single package.

The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT<sup>®</sup> housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion. The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form.

For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is "M4T28-BR12SH" (see Table 13, page 21).

Figure 3. Logic Diagram

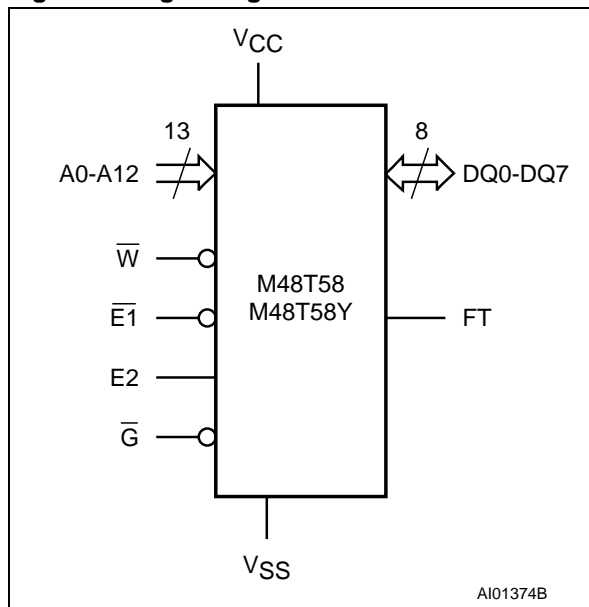


Table 1. Signal Names

|                 |                                    |
|-----------------|------------------------------------|
| A0-A12          | Address Inputs                     |
| DQ0-DQ7         | Data Inputs / Outputs              |
| FT              | Frequency Test Output (Open Drain) |
| $\overline{E1}$ | Chip Enable 1                      |
| E2              | Chip Enable 2                      |
| $\overline{G}$  | Output Enable                      |
| $\overline{W}$  | WRITE Enable                       |
| Vcc             | Supply Voltage                     |
| Vss             | Ground                             |

Figure 4. DIP Connections

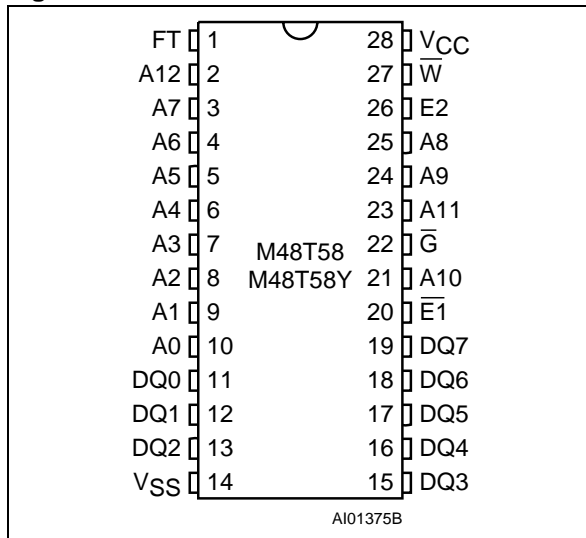


Figure 5. SOIC Connections

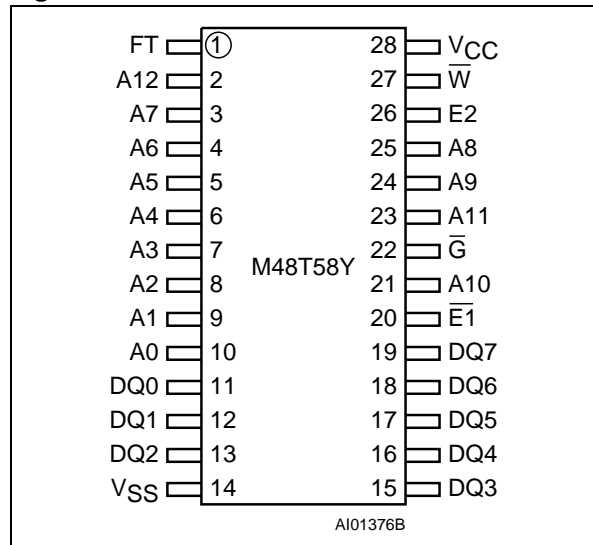
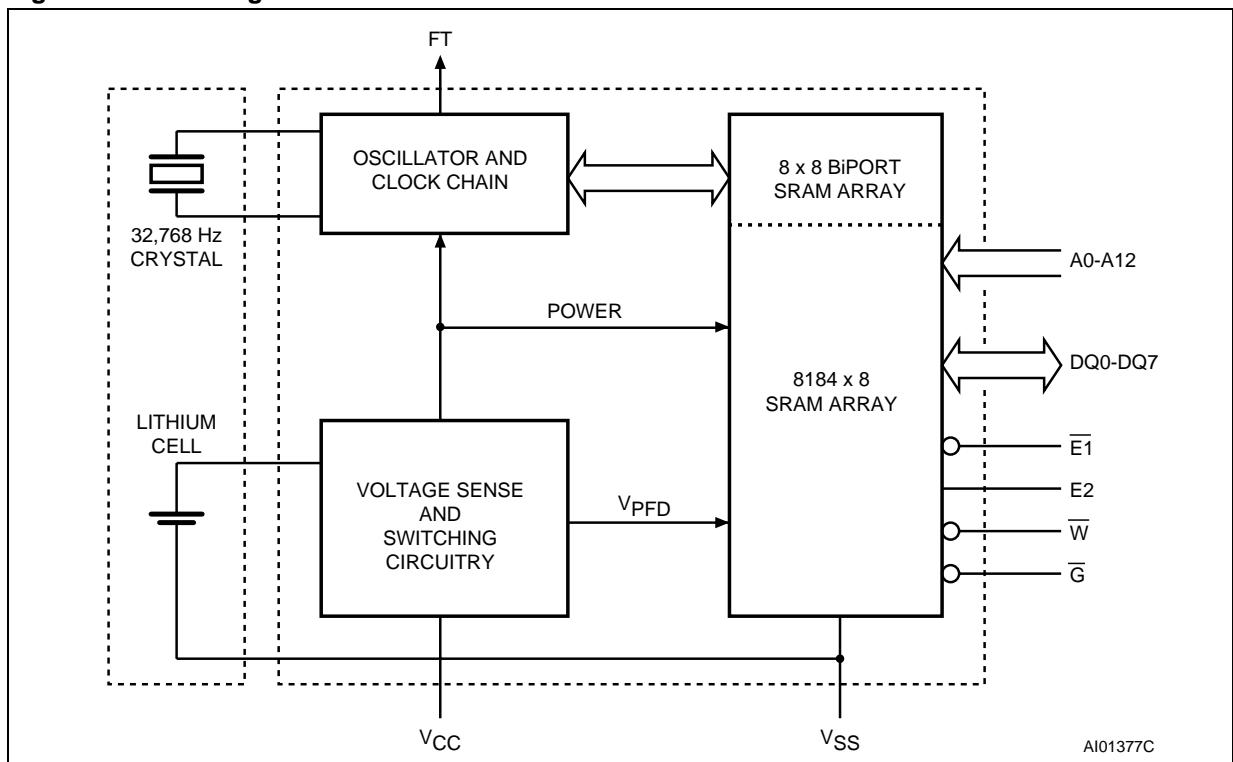


Figure 6. Block Diagram



**MAXIMUM RATING**

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is

not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute Maximum Ratings**

| Symbol                            | Parameter   | Value     | Unit |
|-----------------------------------|---|-----------|------|
| T <sub>A</sub>                    | Ambient Operating Temperature                             | 0 to 70   | °C   |
| T <sub>STG</sub>                  | Storage Temperature (V <sub>CC</sub> Off, Oscillator Off) | –40 to 85 | °C   |
| T <sub>SLD</sub> <sup>(1,2)</sup> | Lead Solder Temperature for 10 seconds                    | 260       | °C   |
| V <sub>IO</sub>                   | Input or Output Voltages                                  | –0.3 to 7 | V    |
| V <sub>CC</sub>                   | Supply Voltage  | –0.3 to 7 | V    |
| I <sub>O</sub>                    | Output Current  | 20        | mA   |
| P <sub>D</sub>                    | Power Dissipation   | 1         | W    |

Note: 1. For DIP package: Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).  
2. For SO package: Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 to 120 seconds).

**CAUTION:** Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.

**CAUTION:** Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

## DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

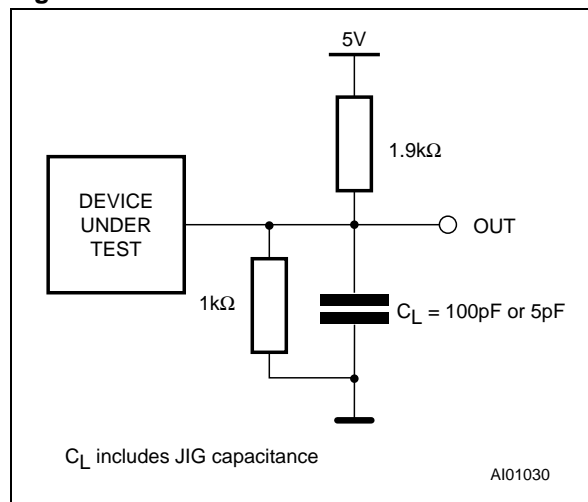
ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 3. Operating and AC Measurement Conditions**

| Parameter                               | M48T58      | M48T58Y    | Unit |
|---|-------------|------------|------|
| Supply Voltage ( $V_{CC}$ )             | 4.75 to 5.5 | 4.5 to 5.5 | V    |
| Ambient Operating Temperature ( $T_A$ ) | 0 to 70     | 0 to 70    | °C   |
| Load Capacitance ( $C_L$ )              | 100         | 100        | pF   |
| Input Rise and Fall Times               | $\leq 5$    | $\leq 5$   | ns   |
| Input Pulse Voltages                    | 0 to 3      | 0 to 3     | V    |
| Input and Output Timing Ref. Voltages   | 1.5         | 1.5        | V    |

Note: Output Hi-Z is defined as the point where data is no longer driven.

**Figure 7. AC Measurement Load Circuit**



**Table 4. Capacitance**

| Symbol          | Parameter <sup>(1,2)</sup> | Min | Max | Unit |
|-----------------|----------------------------|-----|-----|------|
| $C_{IN}$        | Input Capacitance          |     | 10  | pF   |
| $C_{OUT}^{(3)}$ | Output Capacitance         |     | 10  | pF   |

Note: 1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.

2. At 25°C,  $f = 1\text{MHz}$ .

3. Outputs deselected.

## M48T58, M48T58Y

**Table 5. DC Characteristics**

| Symbol         | Parameter                              | Test Condition <sup>(1)</sup>                           | M48T58 |                | M48T58Y |                | Unit    |
|----------------|--|---|--------|----------------|---------|----------------|---------|
|                |  |   | Min    | Max            | Min     | Max            |         |
| $I_{LI}$       | Input Leakage Current                  | $0V \leq V_{IN} \leq V_{CC}$                            |        | $\pm 1$        |         | $\pm 1$        | $\mu A$ |
| $I_{LO}^{(2)}$ | Output Leakage Current                 | $0V \leq V_{OUT} \leq V_{CC}$                           |        | $\pm 1$        |         | $\pm 1$        | $\mu A$ |
| $I_{CC}$       | Supply Current                         | Outputs open  |        | 50             |         | 50             | mA      |
| $I_{CC1}$      | Supply Current (Standby)<br>TTL        | $\overline{E1} = V_{IH}$<br>$E2 = V_{IO}$               |        | 3              |         | 3              | mA      |
| $I_{CC2}$      | Supply Current (Standby)<br>CMOS       | $\overline{E1} = V_{CC} - 0.2V$<br>$E2 = V_{SS} + 0.2V$ |        | 3              |         | 3              | mA      |
| $V_{IL}^{(3)}$ | Input Low Voltage                      |   | -0.3   | 0.8            | -0.3    | 0.8            | V       |
| $V_{IH}$       | Input High Voltage                     |   | 2.2    | $V_{CC} + 0.3$ | 2.2     | $V_{CC} + 0.3$ | V       |
| $V_{OL}$       | Output Low Voltage                     | $I_{OL} = 2.1mA$  |        | 0.4            |         | 0.4            |         |
|                | Output Low Voltage (FT) <sup>(4)</sup> | $I_{OL} = 10mA$   |        | 0.4            |         | 0.4            | V       |
| $V_{OH}$       | Output High Voltage                    | $I_{OH} = -1mA$   | 2.4    |                | 2.4     |                | V       |

Note: 1. Valid for Ambient Operating Temperature:  $T_A = 0$  to  $70^\circ C$ ;  $V_{CC} = 4.75$  to  $5.5V$  or  $4.5$  to  $5.5V$  (except where noted).

2. Outputs deselected.

3. Negative spikes of  $-1V$  allowed for up to  $10ns$  once per Cycle.

4. The FT pin is Open Drain.



## OPERATION MODES

As Figure 6, page 5 shows, the static memory array and the quartz controlled clock oscillator of the M48T58/Y are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the century, year, month, date, day, hour, minute, and second in 24 hour BCD format (except for the century). Corrections for 28, 29 (leap year - valid until 2100), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations

consisting of BiPORT™ READ/write memory cells. The M48T58/Y includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T58/Y also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When  $V_{CC}$  is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low  $V_{CC}$ . As  $V_{CC}$  falls below the Battery Back-up Switchover Voltage ( $V_{SO}$ ), the control circuitry connects the battery which maintains data and clock operation until valid power returns.

**Table 6. Operating Modes**

| Mode     | $V_{CC}$                                   | $\overline{E1}$ | E2       | $\overline{G}$ | $\overline{W}$ | DQ0-DQ7          | Power                |
|----------|--|-----------------|----------|----------------|----------------|------------------|----------------------|
| Deselect | 4.75 to 5.5V<br>or<br>4.5 to 5.5V          | $V_{IH}$        | X        | X              | X              | High Z           | Standby              |
| Deselect |  | X               | $V_{IL}$ | X              | X              | High Z           | Standby              |
| WRITE    |  | $V_{IL}$        | $V_{IH}$ | X              | $V_{IL}$       | D <sub>IN</sub>  | Active               |
| READ     |  | $V_{IL}$        | $V_{IH}$ | $V_{IL}$       | $V_{IH}$       | D <sub>OUT</sub> | Active               |
| READ     |  | $V_{IL}$        | $V_{IH}$ | $V_{IH}$       | $V_{IH}$       | High Z           | Active               |
| Deselect | $V_{SO}$ to $V_{PFD}$ (min) <sup>(1)</sup> | X               | X        | X              | X              | High Z           | CMOS Standby         |
| Deselect | $\leq V_{SO}$ <sup>(1)</sup>               | X               | X        | X              | X              | High Z           | Battery Back-up Mode |

Note: X =  $V_{IH}$  or  $V_{IL}$ ;  $V_{SO}$  = Battery Back-up Switchover Voltage.

1. See Table 10, page 16 for details.

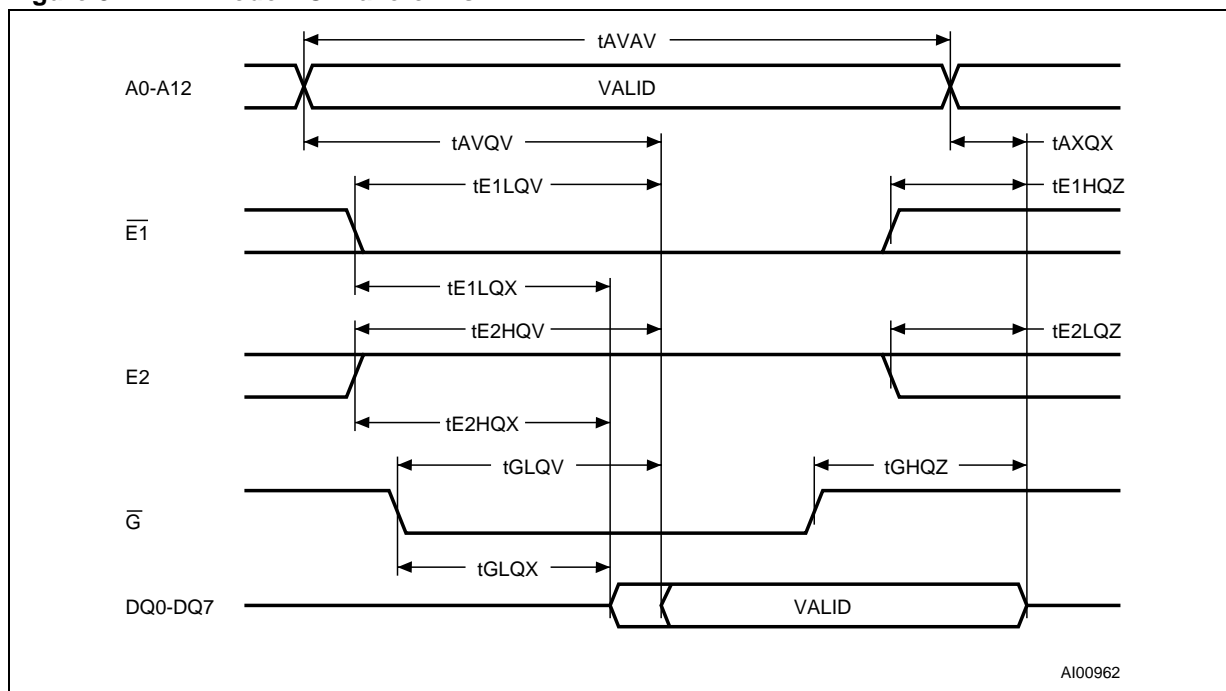
**READ Mode**

The M48T58/Y is in the READ Mode whenever  $\overline{W}$  (WRITE Enable) is high, E1 (Chip Enable 1) is low, and E2 (Chip Enable 2) is high. The unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time ( $t_{AVQV}$ ) after the last address input signal is stable, providing that the  $\overline{E1}$ , E2, and  $\overline{G}$  access times are also satisfied. If the  $\overline{E1}$ , E2 and  $\overline{G}$  access times are not met, valid data will be available after the latter of the Chip En-

able Access times ( $t_{E1LQV}$  or  $t_{E2HQV}$ ) or Output Enable Access time ( $t_{GLQV}$ ).

The state of the eight three-state Data I/O signals is controlled by E1, E2 and G. If the outputs are activated before  $t_{AVQV}$ , the data lines will be driven to an indeterminate state until  $t_{AVQV}$ . If the Address Inputs are changed while  $\overline{E1}$ , E2 and  $\overline{G}$  remain active, output data will remain valid for Output Data Hold time ( $t_{AXQX}$ ) but will go indeterminate until the next Address Access.

**Figure 8. READ Mode AC Waveforms**



Note: WRITE Enable ( $\overline{W}$ ) = High.

Table 7. READ Mode AC Characteristics

| Symbol                            | Parameter <sup>(1)</sup>                | M48T58/Y |     | Unit |
|-----------------------------------|---|----------|-----|------|
|                                   |   | Min      | Max |      |
| t <sub>AVAV</sub>                 | READ Cycle Time                         | 70       |     | ns   |
| t <sub>AVQV</sub>                 | Address Valid to Output Valid           |          | 70  | ns   |
| t <sub>E1LQV</sub>                | Chip Enable 1 Low to Output Valid       |          | 70  | ns   |
| t <sub>E2HQV</sub>                | Chip Enable 2 High to Output Valid      |          | 70  | ns   |
| t <sub>GLQV</sub>                 | Output Enable Low to Output Valid       |          | 35  | ns   |
| t <sub>E1LQX</sub> <sup>(2)</sup> | Chip Enable 1 Low to Output Transition  | 5        |     | ns   |
| t <sub>E2HQX</sub> <sup>(2)</sup> | Chip Enable 2 High to Output Transition | 5        |     | ns   |
| t <sub>GLQX</sub> <sup>(2)</sup>  | Output Enable Low to Output Transition  | 5        |     | ns   |
| t <sub>E1HQZ</sub> <sup>(2)</sup> | Chip Enable 1 High to Output Hi-Z       |          | 25  | ns   |
| t <sub>E2LQZ</sub> <sup>(2)</sup> | Chip Enable 2 Low to Output Hi-Z        |          | 25  | ns   |
| t <sub>GHQZ</sub> <sup>(2)</sup>  | Output Enable High to Output Hi-Z       |          | 25  | ns   |
| t <sub>AXQX</sub>                 | Address Transition to Output Transition | 10       |     | ns   |

Note: 1. Valid for Ambient Operating Temperature: T<sub>A</sub> = 0 to 70°C; V<sub>CC</sub> = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).

2. C<sub>L</sub> = 5pF.

**WRITE Mode**

The M48T58/Y is in the WRITE Mode whenever  $\overline{W}$  and E1 are low and E2 is high. The start of a WRITE is referenced from the latter occurring falling edge of  $\overline{W}$  or  $\overline{E1}$ , or the rising edge of E2. A WRITE is terminated by the earlier rising edge of  $\overline{W}$  or  $\overline{E1}$ , or the falling edge of E2. The addresses must be held valid throughout the cycle. E1 or  $\overline{W}$  must return high or E2 low for a minimum of  $t_{E1HAX}$  or  $t_{E2LAX}$  from Chip Enable or  $t_{WHAX}$  from WRITE

Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid  $t_{DVWH}$  prior to the end of WRITE and remain valid for  $t_{WHDX}$  afterward.  $\overline{G}$  should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on  $\overline{E1}$  and  $\overline{G}$  and a high on  $\overline{E2}$ , a low on  $\overline{W}$  will disable the outputs  $t_{WLQZ}$  after  $\overline{W}$  falls.

**Figure 9. WRITE Enable Controlled, WRITE AC Waveform**

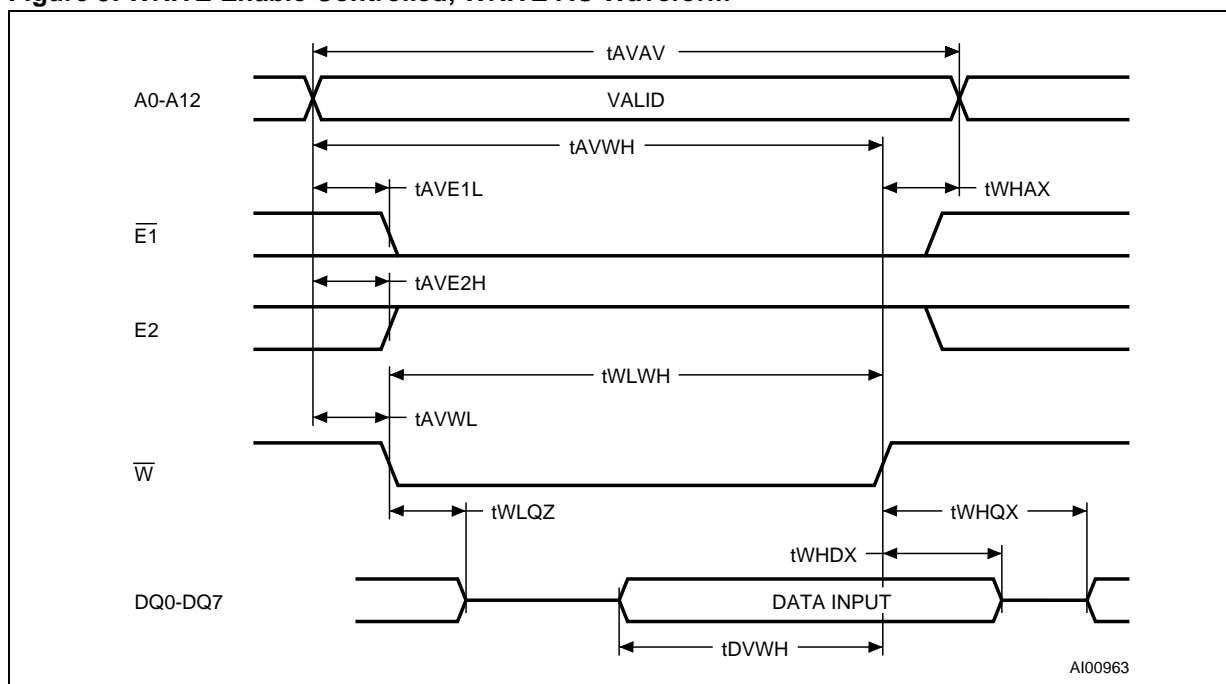
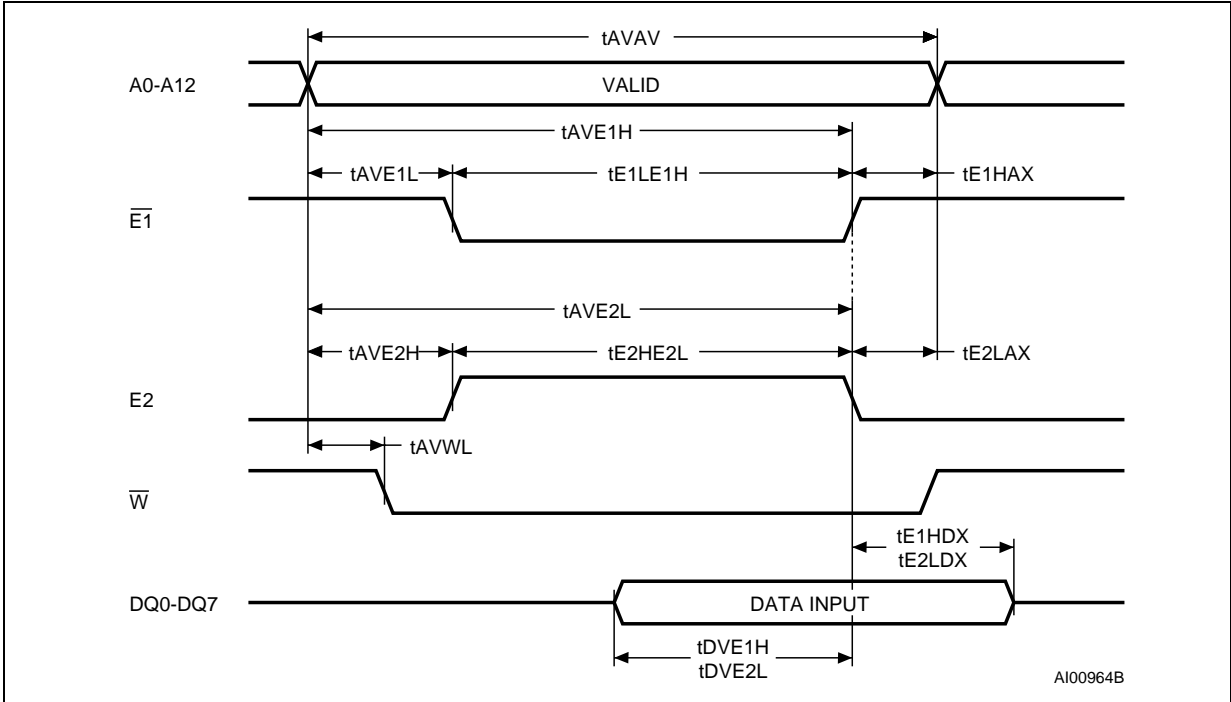


Figure 10. Chip Enable Controlled, WRITE AC Waveforms



## M48T58, M48T58Y

**Table 8. WRITE Mode AC Characteristics**

| Symbol                             | Parameter <sup>(1)</sup>                 | M48T58/Y |     | Unit |
|------------------------------------|--|----------|-----|------|
|                                    |  | Min      | Max |      |
| t <sub>AVAV</sub>                  | WRITE Cycle Time                         | 70       |     | ns   |
| t <sub>AVWL</sub>                  | Address Valid to WRITE Enable Low        | 0        |     | ns   |
| t <sub>AVE1L</sub>                 | Address Valid to Chip Enable 1 Low       | 0        |     | ns   |
| t <sub>AVE2H</sub>                 | Address Valid to Chip Enable 2 High      | 0        |     | ns   |
| t <sub>WLWH</sub>                  | WRITE Enable Pulse Width                 | 50       |     | ns   |
| t <sub>E1LE1H</sub>                | Chip Enable 1 Low to Chip Enable 1 High  | 55       |     | ns   |
| t <sub>E2HE2L</sub>                | Chip Enable 2 High to Chip Enable 2 Low  | 55       |     | ns   |
| t <sub>WHAX</sub>                  | WRITE Enable High to Address Transition  | 0        |     | ns   |
| t <sub>E1HAX</sub>                 | Chip Enable 1 High to Address Transition | 0        |     | ns   |
| t <sub>E2LAX</sub>                 | Chip Enable 2 Low to Address Transition  | 0        |     | ns   |
| t <sub>DVWH</sub>                  | Input Valid to WRITE Enable High         | 30       |     | ns   |
| t <sub>DVE1H</sub>                 | Input Valid to Chip Enable 1 High        | 30       |     | ns   |
| t <sub>DVE2L</sub>                 | Input Valid to Chip Enable 2 Low         | 30       |     | ns   |
| t <sub>WHDX</sub>                  | WRITE Enable High to Input Transition    | 5        |     | ns   |
| t <sub>E1HDX</sub>                 | Chip Enable 1 High to Input Transition   | 5        |     | ns   |
| t <sub>E2LDX</sub>                 | Chip Enable 2 Low to Input Transition    | 5        |     | ns   |
| t <sub>WLQZ</sub> <sup>(2,3)</sup> | Write Enable Low to Output Hi-Z          |          | 25  | ns   |
| t <sub>AVWH</sub>                  | Address Valid to WRITE Enable High       | 60       |     | ns   |
| t <sub>AVE1H</sub>                 | Address Valid to Chip Enable 1 High      | 60       |     | ns   |
| t <sub>AVE2L</sub>                 | Address Valid to Chip Enable 2 Low       | 60       |     | ns   |
| t <sub>WHQX</sub> <sup>(2,3)</sup> | WRITE Enable High to Output Transition   | 5        |     | ns   |

Note: 1. Valid for Ambient Operating Temperature: T<sub>A</sub> = 0 to 70°C; V<sub>CC</sub> = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).

2. C<sub>L</sub> = 5pF.

3. If  $\overline{E1}$  goes low or E2 high simultaneously with  $\overline{W}$  going low, the outputs remain in the high impedance state.

### Data Retention Mode

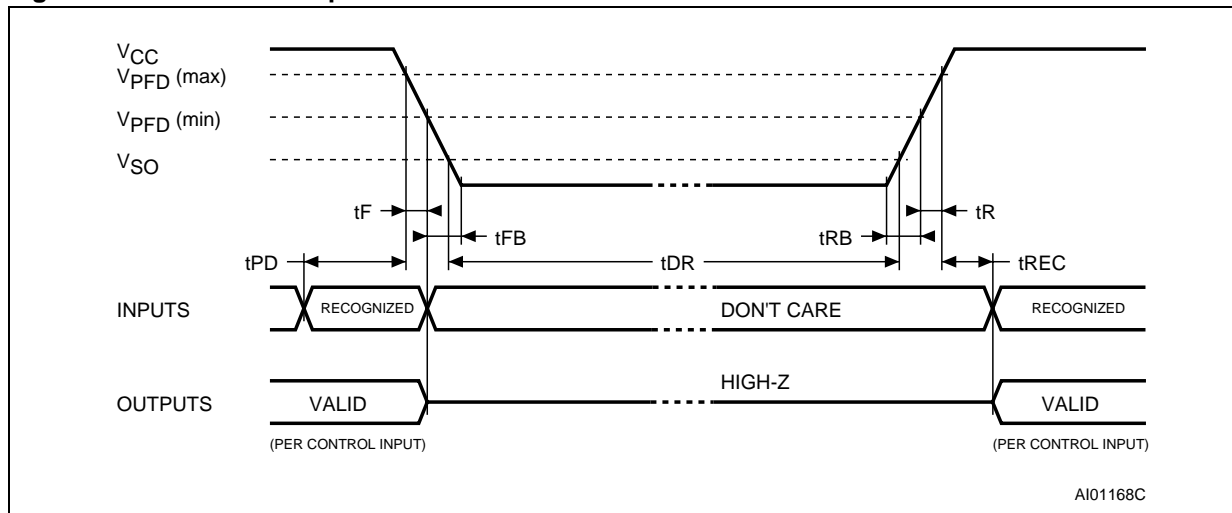
With valid  $V_{CC}$  applied, the M48T58/Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when  $V_{CC}$  falls within the  $V_{PFD}(\max)$ ,  $V_{PFD}(\min)$  window. All outputs become high impedance, and all inputs are treated as “don't care.”

**Note:** A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below  $V_{PFD}(\min)$ , the user can be assured the memory will be in a write protected state, provided the  $V_{CC}$  fall time is not less than  $t_F$ . The M48T58/Y may respond to transient noise spikes on  $V_{CC}$  that reach into the deselect window during the time the device is sampling  $V_{CC}$ . Therefore, decoupling of the power supply lines is recommended.

When  $V_{CC}$  drops below  $V_{SO}$ , the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T58/Y for an accumulated period of at least 7 years when  $V_{CC}$  is less than  $V_{SO}$ . As system power returns and  $V_{CC}$  rises above  $V_{SO}$ , the battery is disconnected, and the power supply is switched to external  $V_{CC}$ . Write protection continues until  $V_{CC}$  reaches  $V_{PFD}(\min)$  plus  $t_{REC}(\min)$ . E1 should be kept high or E2 low as  $V_{CC}$  rises past  $V_{PFD}(\min)$  to prevent inadvertent WRITE cycles prior to system stabilization. Normal RAM operation can resume  $t_{REC}$  after  $V_{CC}$  exceeds  $V_{PFD}(\max)$ .

For more information on Battery Storage Life refer to the Application Note AN1012.

**Figure 11. Power Down/Up Mode AC Waveforms**



## M48T58, M48T58Y

**Table 9. Power Down/Up AC Characteristics**

| Symbol                         | Parameter <sup>(1)</sup>  | Min     | Max | Unit |    |
|--------------------------------|---|---------|-----|------|----|
| t <sub>PD</sub>                | $\overline{E1}$ or $\overline{W}$ at V <sub>IH</sub> or E2 at V <sub>IL</sub> before Power Down | 0       |     | μs   |    |
| t <sub>F</sub> <sup>(2)</sup>  | V <sub>PFD</sub> (max) to V <sub>PFD</sub> (min) V <sub>CC</sub> Fall Time                      | 300     |     | μs   |    |
| t <sub>FB</sub> <sup>(3)</sup> | V <sub>PFD</sub> (min) to V <sub>SS</sub> V <sub>CC</sub> Fall Time                             | M48T58  | 10  |      | μs |
|                                |   | M48T58Y | 10  |      | μs |
| t <sub>R</sub>                 | V <sub>PFD</sub> (min) to V <sub>PFD</sub> (max) V <sub>CC</sub> Rise Time                      | 10      |     | μs   |    |
| t <sub>RB</sub>                | V <sub>SS</sub> to V <sub>PFD</sub> (min) V <sub>CC</sub> Rise Time                             | 1       |     | μs   |    |
| t <sub>REC</sub>               | V <sub>PFD</sub> (max) to Inputs Recognized   | 40      | 200 | ms   |    |

Note: 1. Valid for Ambient Operating Temperature: T<sub>A</sub> = 0 to 70°C; V<sub>CC</sub> = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).  
 2. V<sub>PFD</sub> (max) to V<sub>PFD</sub> (min) fall time of less than t<sub>F</sub> may result in deselection/write protection not occurring until 200μs after V<sub>CC</sub> passes V<sub>PFD</sub> (min).  
 3. V<sub>PFD</sub> (min) to V<sub>SS</sub> fall time of less than t<sub>FB</sub> may cause corruption of RAM data.

**Table 10. Power Down/Up Trip Points DC Characteristics**

| Symbol                         | Parameter <sup>(1,2)</sup>         | Min     | Typ | Max  | Unit  |   |
|--------------------------------|------------------------------------|---------|-----|------|-------|---|
| V <sub>PFD</sub>               | Power-fail Deselect Voltage        | M48T58  | 4.5 | 4.6  | 4.75  | V |
|                                |                                    | M48T58Y | 4.2 | 4.35 | 4.5   | V |
| V <sub>SO</sub>                | Battery Back-up Switchover Voltage |         | 3.0 |      | V     |   |
| t <sub>DR</sub> <sup>(3)</sup> | Expected Data Retention Time       | 7       |     |      | YEARS |   |

Note: 1. Valid for Ambient Operating Temperature: T<sub>A</sub> = 0 to 70°C; V<sub>CC</sub> = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).  
 2. All voltages referenced to V<sub>SS</sub>.  
 3. At 25°C.



## CLOCK OPERATIONS

### Reading the Clock

Updates to the TIMEKEEPER® registers (see Table 11) should be halted before clock data is read to prevent reading data in transition. The Bi-PORT™ TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ Bit, D6 in the Control Register 1FF8h. As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0.'

### Setting the Clock

Bit D7 of the Control register (1FF8h) is the WRITE Bit. Setting the WRITE Bit to a '1,' like the READ Bit, halts updates to the TIMEKEEPER® registers. The user can then load them with the

correct day, date, and time data in 24 hour BCD format (see Table 11, page 17). Resetting the WRITE Bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The bits marked as '0' in Table 11, page 17 must be written to '0' to allow for normal TIMEKEEPER and RAM operation. After the WRITE Bit is reset, the next clock update will occur within one second.

See the Application Note AN923 "TIMEKEEPER Rolling Into the 21st Century" for information on Century Rollover.

### Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP Bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T58/Y is shipped from STMicroelectronics with the STOP Bit set to a '1.' When reset to a '0,' the M48T58/Y oscillator starts within 1 second.

**Table 11. Register Map**

| Address | Data     |            |          |             |         |     |    |         | Function/Range<br>BCD Format |         |
|---------|----------|------------|----------|-------------|---------|-----|----|---------|------------------------------|---------|
|         | D7       | D6         | D5       | D4          | D3      | D2  | D1 | D0      |                              |         |
| 1FFFh   | 10 Years |            |          |             | Year    |     |    |         | Year                         | 00-99   |
| 1FFEh   | 0        | 0          | 0        | 10 M        | Month   |     |    |         | Month                        | 01-12   |
| 1FFDh   | BLE      | BL         | 10 Date  |             | Date    |     |    |         | Date                         | 01-31   |
| 1FFCh   | 0        | FT         | CEB      | CB          | 0       | Day |    |         | Century/Day                  | 0-1/1-7 |
| 1FFBh   | 0        | 0          | 10 Hours |             | Hours   |     |    |         | Hours                        | 00-23   |
| 1FFAh   | 0        | 10 Minutes |          |             | Minutes |     |    |         | Minutes                      | 00-59   |
| 1FF9h   | ST       | 10 Seconds |          |             | Seconds |     |    |         | Seconds                      | 00-59   |
| 1FF8h   | W        | R          | S        | Calibration |         |     |    | Control |                              |         |

Keys: S = SIGN Bit

FT = FREQUENCY TEST Bit

R = READ Bit

W = WRITE Bit

ST = STOP Bit

0 = Must be set to '0'

BLE = Battery Low Enable Bit

BL = Battery Low Bit (Read only)

CEB = Century Enable Bit

CB = Century Bit

Note: When CEB is set to '1,' CB will toggle from '0' to '1' or from '1' to '0' at the turn of the century (dependent upon the initial value set). When CEB is set to '0,' CB will not toggle. The WRITE Bit does not need to be set to write to CEB.

### Calibrating the Clock

The M48T58/Y is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about  $\pm 1.53$  minutes per month. With the calibration bits properly set, the accuracy of each M48T58/Y improves to better than  $+1/-2$  ppm at 25°C.

The oscillation rate of any crystal changes with temperature (see Figure 12, page 19). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome “trim” capacitors. The M48T58/Y design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 13, page 20. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration Byte occupies the five lower order bits (D4-D0) in the Control Register 1FF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is the Sign Bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is

+4.068 or  $-2.034$  ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration Byte would represent +10.7 or  $-5.35$  seconds per month which corresponds to a total range of +5.5 or  $-2.75$  minutes per month.

Two methods are available for ascertaining how much calibration a given M48T58/Y may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration Byte.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) Bit (D6 in the Day Register) is set to a '1,' and D7 of the Seconds Register is a '0' (Oscillator Running), The Frequency Test (Pin 1) will toggle at 512Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a  $-10$  (WR001010) to be loaded into the Calibration Byte for correction.

The Frequency Test pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10k $\Omega$  resistor is recommended in order to control the rise time.

For more information on calibration, see Application Note AN934, “TIMEKEEPER<sup>®</sup> Calibration.”

### Battery Low Flag

The M48T58/Y automatically performs periodic battery voltage monitoring upon power-up and at factory-programmed time intervals of 24 hours (at day rollover) as long as the device is powered and the oscillator is running. The Battery Low flag (BL), Bit D6 of the flags Register 1FFDh, will be asserted high if the internal or SNAPHAT<sup>®</sup> battery is found to be less than approximately 2.5V and the Battery Low Enable (BLE) Bit has been previously set to '1.' The BL flag will remain active until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery voltage is below 2.5V (approximately), which may be insufficient to maintain data integrity. Data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data has not been compromised due to the fact that a nominal  $V_{CC}$  is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, it is

recommended that the battery be replaced. The SNAPHAT top may be replaced while  $V_{CC}$  is applied to the device.

**Note:** This will cause the clock to lose time during the interval the SNAPHAT battery/crystal top is disconnected.

**Note:** Battery monitoring is a useful technique only when performed periodically. The M48T58/Y only monitors the battery when a nominal  $V_{CC}$  is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

### Century Bit

Bit D5 and D4 of Clock Register 1FFCh contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

**Note:** The WRITE Bit must be set in order to write to the CENTURY Bit.

Figure 12. Crystal Accuracy Across Temperature

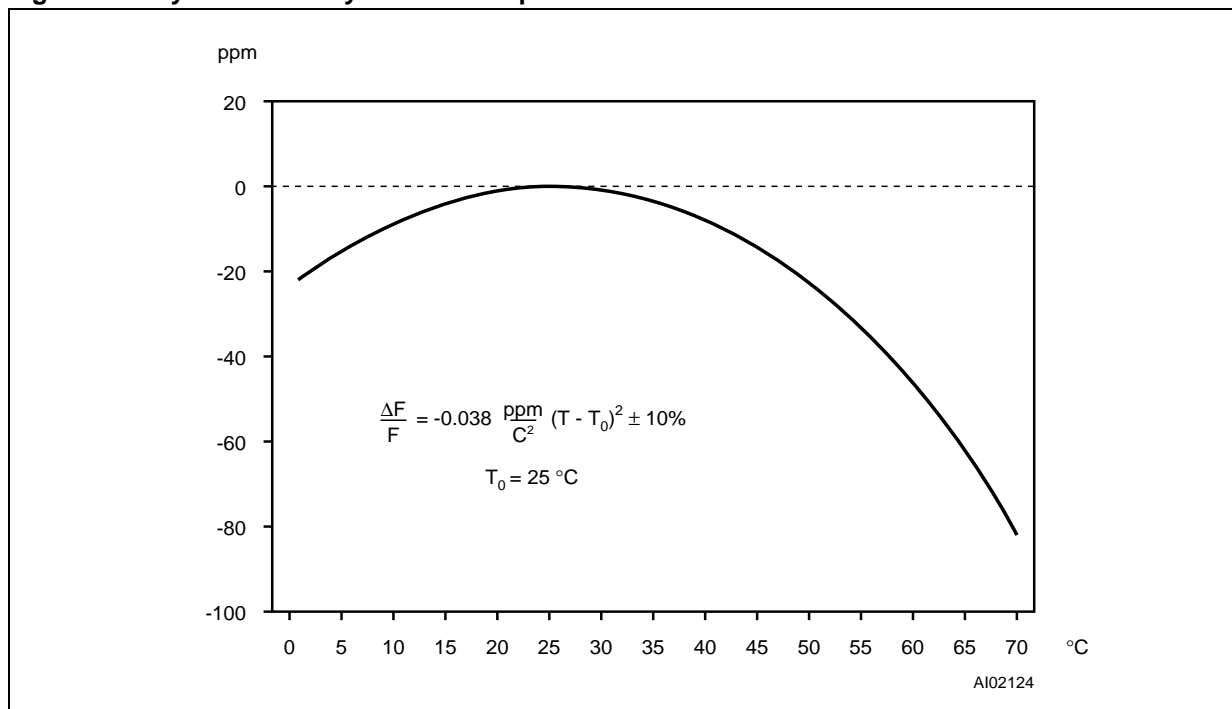
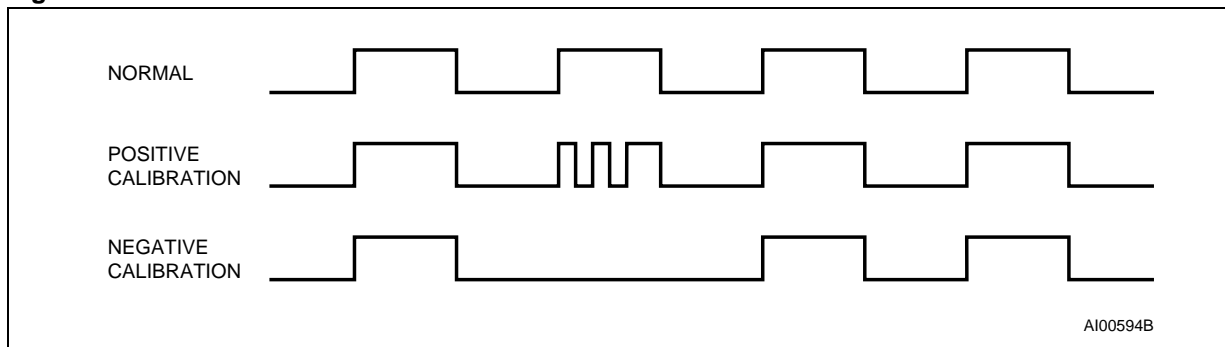


Figure 13. Clock Calibration

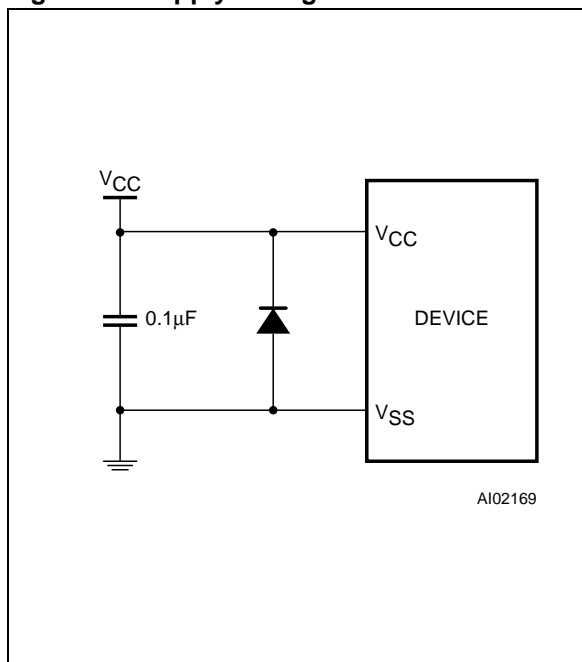


**V<sub>CC</sub> Noise And Negative Going Transients**

I<sub>CC</sub> transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V<sub>CC</sub> bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V<sub>CC</sub> bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A bypass capacitor value of 0.1μF (as shown in Figure 14) is recommended in order to provide the needed filtering.

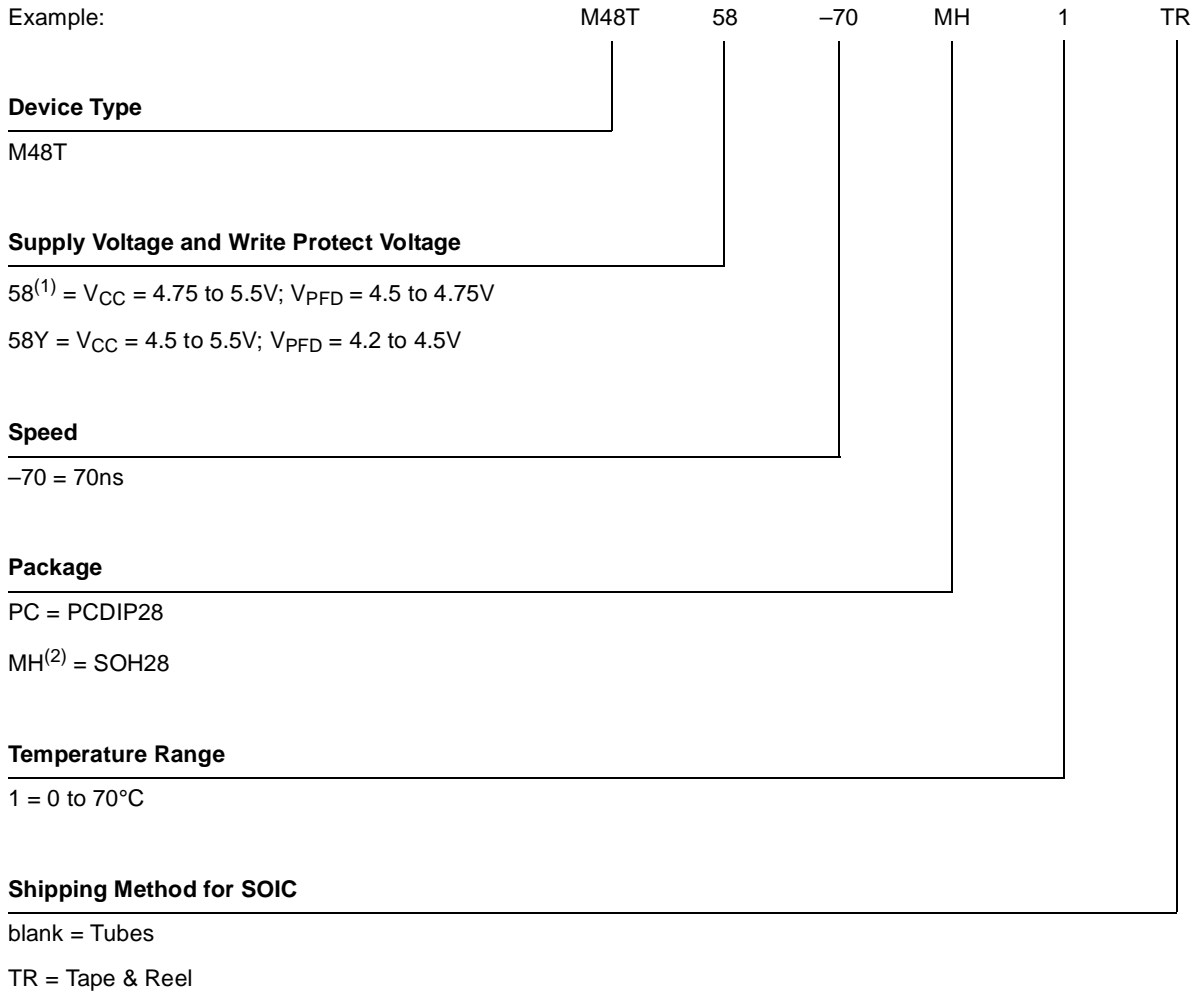
In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V<sub>CC</sub> that drive it to values below V<sub>SS</sub> by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from V<sub>CC</sub> to V<sub>SS</sub> (cathode connected to V<sub>CC</sub>, anode to V<sub>SS</sub>). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 14. Supply Voltage Protection



**PART NUMBERING**

**Table 12. Ordering Information Scheme**



Note: 1. The M48T58 part is offered with the PCDIP28 (e.g., CAPHAT™) package only.  
 2. The SOIC package (SOH28) requires the battery package (SNAPHAT®) which is ordered separately under the part number "M4TXX-BR12SH" in plastic tube or "M4TXX-BR12SHTR" in Tape & Reel form.

**Caution:** Do not place the SNAPHAT battery package "M4TXX-BR00SH" in conductive foam as it will drain the lithium button-cell battery.

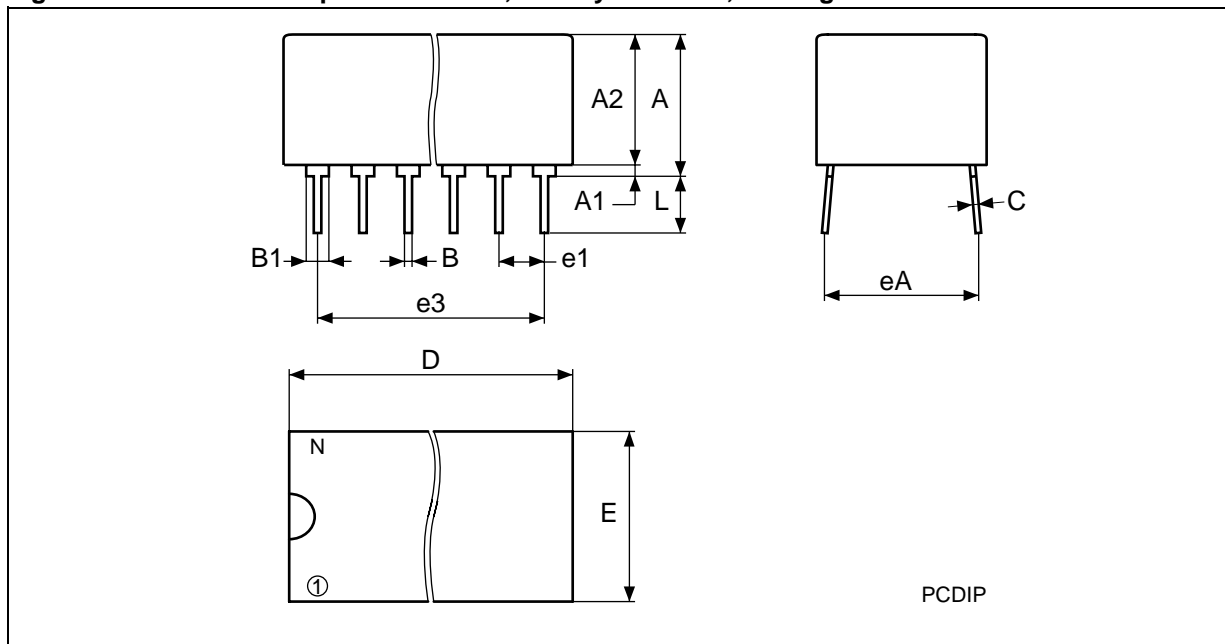
For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

**Table 13. SNAPHAT Battery Table**

| Part Number  | Description                      | Package |
|--------------|----------------------------------|---------|
| M4T28-BR12SH | Lithium Battery (48mAh) SNAPHAT  | SH      |
| M4T32-BR12SH | Lithium Battery (120mAh) SNAPHAT | SH      |

PACKAGE MECHANICAL INFORMATION

Figure 15. PCDIP28 – 28-pin Plastic DIP, battery CAPHAT, Package Outline

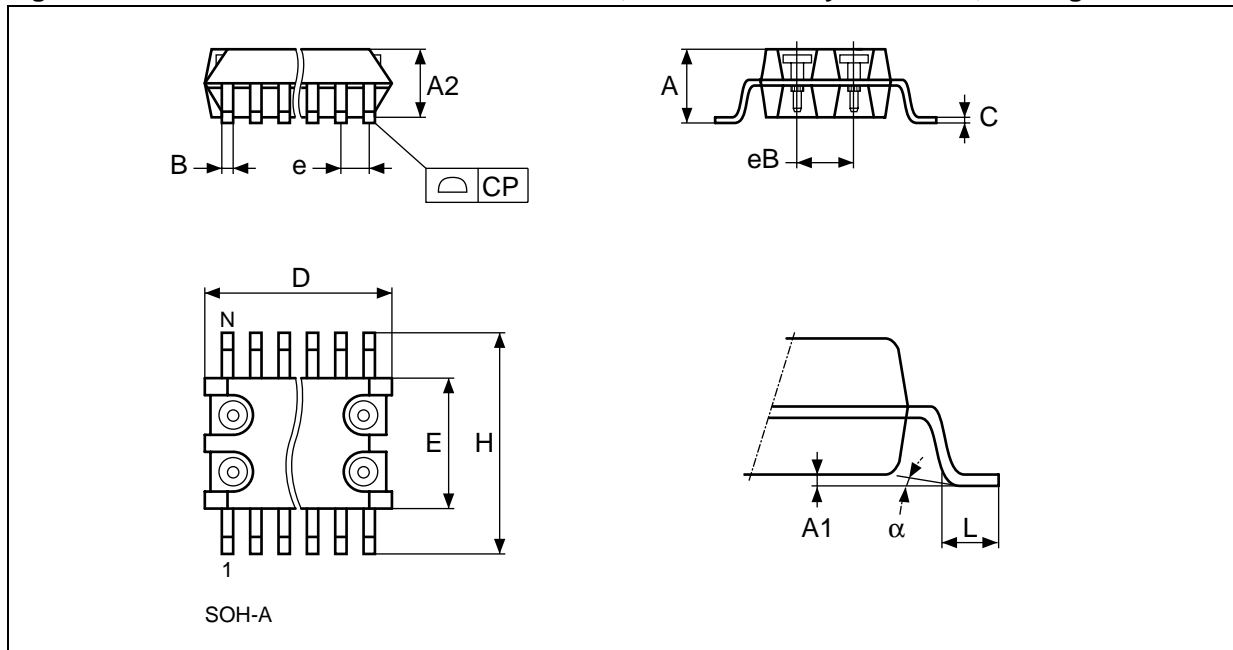


Note: Drawing is not to scale.

Table 14. PCDIP28 – 28-pin Plastic DIP, battery CAPHAT, Package Mechanical Data

| Symb | mm  |       |       | inches |       |       |
|------|-----|-------|-------|--------|-------|-------|
|      | Typ | Min   | Max   | Typ    | Min   | Max   |
| A    |     | 8.89  | 9.65  |        | 0.350 | 0.380 |
| A1   |     | 0.38  | 0.76  |        | 0.015 | 0.030 |
| A2   |     | 8.38  | 8.89  |        | 0.330 | 0.350 |
| B    |     | 0.38  | 0.53  |        | 0.015 | 0.021 |
| B1   |     | 1.14  | 1.78  |        | 0.045 | 0.070 |
| C    |     | 0.20  | 0.31  |        | 0.008 | 0.012 |
| D    |     | 39.37 | 39.88 |        | 1.550 | 1.570 |
| E    |     | 17.83 | 18.34 |        | 0.702 | 0.722 |
| e1   |     | 2.29  | 2.79  |        | 0.090 | 0.110 |
| e3   |     | 29.72 | 36.32 |        | 1.170 | 1.430 |
| eA   |     | 15.24 | 16.00 |        | 0.600 | 0.630 |
| L    |     | 3.05  | 3.81  |        | 0.120 | 0.150 |
| N    |     | 28    |       |        | 28    |       |

Figure 16. SOH28 – 28-lead Plastic Small Outline, 4-socket battery SNAPHAT, Package Outline

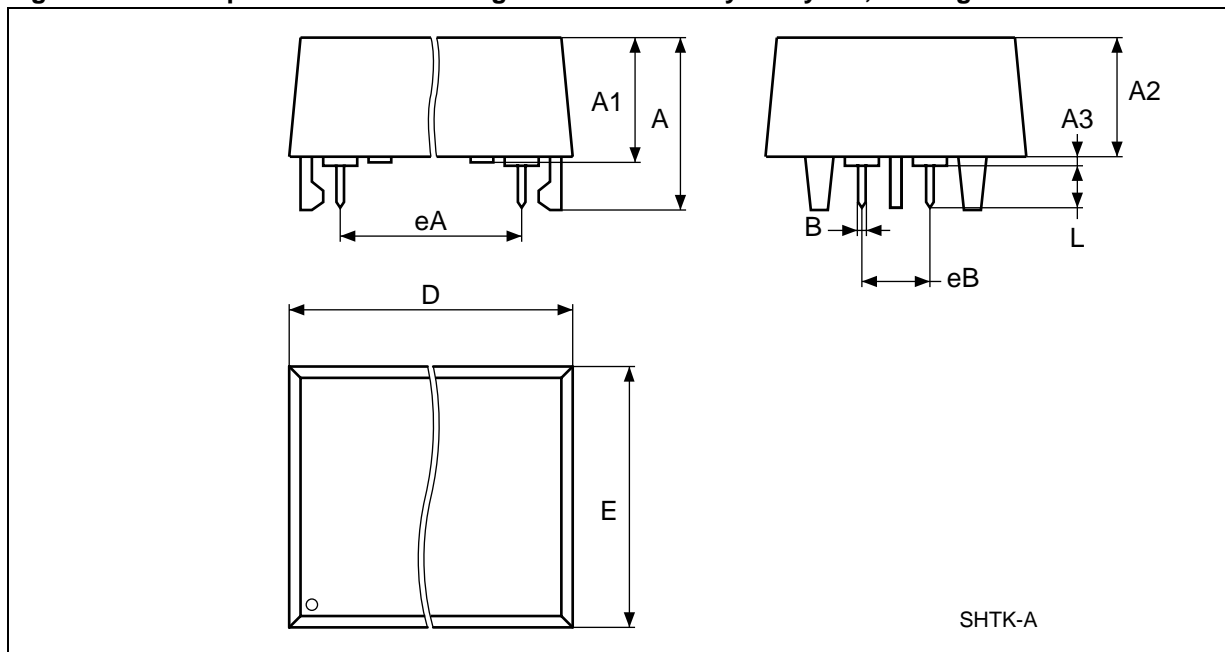


Note: Drawing is not to scale.

Table 15. SOH28 – 28-lead Plastic Small Outline, 4-socket battery SNAPHAT, Package Mechanical Data

| Symb     | mm   |       |       | inches |       |       |
|----------|------|-------|-------|--------|-------|-------|
|          | Typ  | Min   | Max   | Typ    | Min   | Max   |
| A        |      |       | 3.05  |        |       | 0.120 |
| A1       |      | 0.05  | 0.36  |        | 0.002 | 0.014 |
| A2       |      | 2.34  | 2.69  |        | 0.092 | 0.106 |
| B        |      | 0.36  | 0.51  |        | 0.014 | 0.020 |
| C        |      | 0.15  | 0.32  |        | 0.006 | 0.012 |
| D        |      | 17.71 | 18.49 |        | 0.697 | 0.728 |
| E        |      | 8.23  | 8.89  |        | 0.324 | 0.350 |
| e        | 1.27 | –     | –     | 0.050  | –     | –     |
| eB       |      | 3.20  | 3.61  |        | 0.126 | 0.142 |
| H        |      | 11.51 | 12.70 |        | 0.453 | 0.500 |
| L        |      | 0.41  | 1.27  |        | 0.016 | 0.050 |
| $\alpha$ |      | 0°    | 8°    |        | 0°    | 8°    |
| N        |      | 28    |       |        | 28    |       |
| CP       |      |       | 0.10  |        |       | 0.004 |

Figure 17. SH – 4-pin SNAPHAT Housing for 48mAh Battery & Crystal, Package Outline



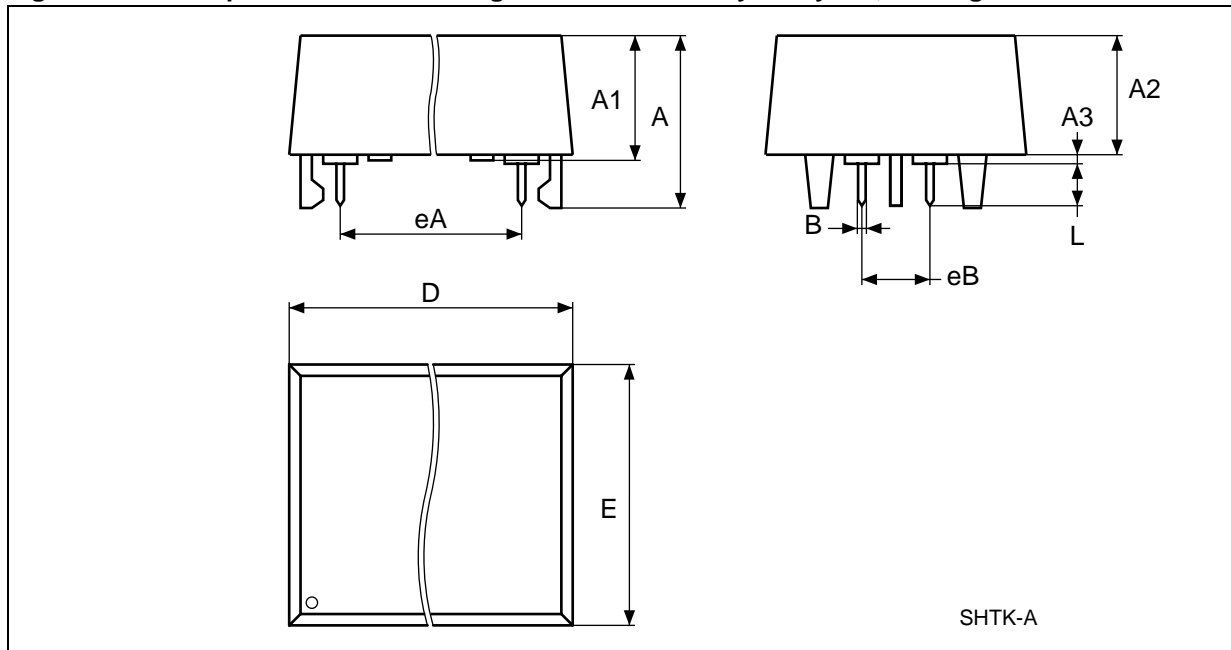
Note: Drawing is not to scale.

Table 16. SH – 4-pin SNAPHAT Housing for 48mAh Battery & Crystal, Package Mechanical Data

| Symb | mm  |       |       | inches |       |       |
|------|-----|-------|-------|--------|-------|-------|
|      | Typ | Min   | Max   | Typ    | Min   | Max   |
| A    |     |       | 9.78  |        |       | 0.385 |
| A1   |     | 6.73  | 7.24  |        | 0.265 | 0.285 |
| A2   |     | 6.48  | 6.99  |        | 0.255 | 0.275 |
| A3   |     |       | 0.38  |        |       | 0.015 |
| B    |     | 0.46  | 0.56  |        | 0.018 | 0.022 |
| D    |     | 21.21 | 21.84 |        | 0.835 | 0.860 |
| E    |     | 14.22 | 14.99 |        | 0.560 | 0.590 |
| eA   |     | 15.55 | 15.95 |        | 0.612 | 0.628 |
| eB   |     | 3.20  | 3.61  |        | 0.126 | 0.142 |
| L    |     | 2.03  | 2.29  |        | 0.080 | 0.090 |



Figure 18. SH – 4-pin SNAPHAT Housing for 120mAh Battery &amp; Crystal, Package Outline



Note: Drawing is not to scale.

Table 17. SH – 4-pin SNAPHAT Housing for 120mAh Battery &amp; Crystal, Package Mechanical Data

| Symb | mm  |       |       | inches |       |       |
|------|-----|-------|-------|--------|-------|-------|
|      | Typ | Min   | Max   | Typ    | Min   | Max   |
| A    |     |       | 10.54 |        |       | 0.415 |
| A1   |     | 8.00  | 8.51  |        | 0.315 | 0.335 |
| A2   |     | 7.24  | 8.00  |        | 0.285 | 0.315 |
| A3   |     |       | 0.38  |        |       | 0.015 |
| B    |     | 0.46  | 0.56  |        | 0.018 | 0.022 |
| D    |     | 21.21 | 21.84 |        | 0.835 | 0.860 |
| E    |     | 17.27 | 18.03 |        | 0.680 | 0.710 |
| eB   |     | 3.20  | 3.61  |        | 0.126 | 0.142 |
| L    |     | 2.03  | 2.29  |        | 0.080 | 0.090 |

**REVISION HISTORY**

**Table 18. Document Revision History**

| <b>Date</b> | <b>Revision Details</b>  |
|-------------|--|
| July 1999   | First Issue  |
| 07/27/00    | Century Bit and Battery Low Flag Paragraphs added<br>Power Down/Up AC Characteristics Table and Waveforms changed (Table 9, Figure 11) |
| 06/04/01    | Reformatted; temperature information added (Tables 5, 7, 8, 9, 10)   |
| 07/31/01    | Formatting changes from recent document review findings  |
| 05/20/02    | Modify reflow time and temperature footnotes (Table 2)   |

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics  
All other names are the property of their respective owners.

© 2002 STMicroelectronics - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES  
Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia -  
Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

[www.st.com](http://www.st.com)