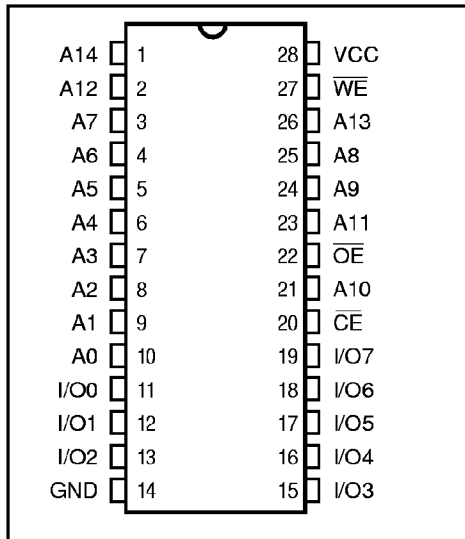


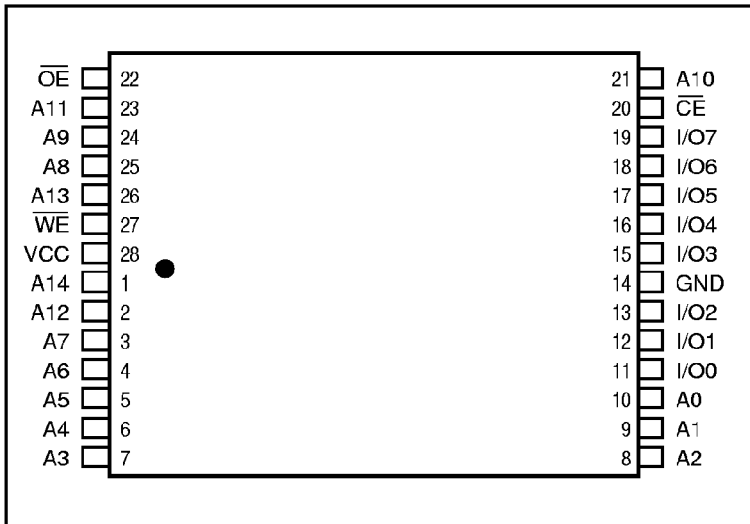
## PIN CONFIGURATION

### 28-Pin SOJ



## PIN CONFIGURATION

### 28-Pin TSOP (Type I)



## PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	Isb1, Isb2
Output Disabled	H	L	H	High-Z	Icc
Read	H	L	L	DOUT	Icc
Write	L	L	X	DIN	Icc

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
VCC	Power Supply Voltage Relative to GND	-0.5 to +4.6	V
VTERM	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
TBIAS	Temperature Under Bias	Com. -10 to +85 Ind. -45 to +90	°C
TSTG	Storage Temperature	-65 to +150	°C
P <sub>D</sub>	Power Dissipation	1	W
I <sub>OUT</sub>	DC Output Current	±20	mA

### Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE**

Range	Ambient Temperature	Speed	V <sub>CC</sub>
Commercial	0°C to +70°C	8, 10, 12	3.3V, +10%, -5%
		15, 20	3.3V ± 10%
Industrial	-40°C to +85°C	All	3.3V + 10%, -5%

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA	2.4	—	V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA	—	0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V	
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	Com.	-1	1	μA
			Ind.	-5	5	
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Outputs Disabled	Com.	-1	1	μA
			Ind.	-5	5	

**Notes:**

- V<sub>IL</sub> (min.) = -0.3V (DC); V<sub>IL</sub> (min.) = -2.0V (pulse width ≤ 2.0 ns).  
V<sub>IH</sub> (max.) = V<sub>CC</sub> + 0.5V (DC); V<sub>IH</sub> (max.) = V<sub>CC</sub> + 2.0V (pulse width ≤ 2.0 ns).
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Sym.	Parameter	Test Conditions		-8 ns <sup>(2)</sup>		-10 ns <sup>(2)</sup>		-12 ns		-15 ns		-20 ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	120	—	110	—	100	—	90	—	80	mA
			Ind.	—	—	—	120	—	110	—	100	—	90	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IK</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CE} \geq V_{IH}$ , f = 0	Com.	—	30	—	25	—	25	—	25	—	25	mA
			Ind.	—	—	—	30	—	30	—	30	—	30	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., $\overline{CE} \leq V_{CC} - 0.2V$ , V <sub>IK</sub> > V <sub>CC</sub> - 0.2V, or V <sub>IK</sub> ≤ 0.2V, f = 0	Com.	—	2	—	2	—	2	—	2	—	2	mA
			Ind.	—	—	—	5	—	5	—	5	—	5	

**Notes:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Shaded area = **PREPRODUCTION AVAILABILITY**.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5	pF

**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 3.3V.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

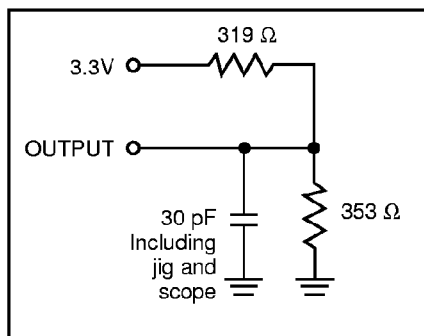
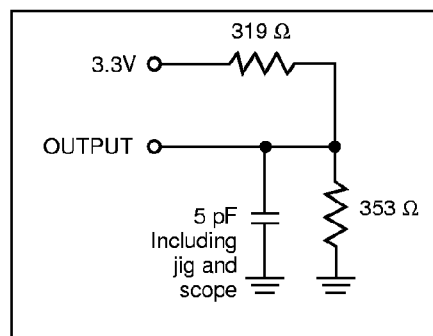
Symbol	Parameter	-8 ns <sup>(2)</sup>		-10 ns <sup>(2)</sup>		-12 ns		-15 ns		-20 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
t <sub>AA</sub>	Address Access Time	—	8	—	10	—	12	—	15	—	20	ns
t <sub>OH(A)</sub>	Output Hold Time	2	—	2	—	2	—	2	—	2	—	ns
t <sub>ACE</sub>	$\overline{CE}$ Access Time	—	8	—	10	—	12	—	15	—	20	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	4	—	5	—	6	—	7	—	8	ns
t <sub>LZOE<sup>(3)</sup></sub>	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	0	—	ns
t <sub>HZOE<sup>(3)</sup></sub>	$\overline{OE}$ to High-Z Output	—	4	—	5	—	5	—	6	—	6	ns
t <sub>LZCE<sup>(3)</sup></sub>	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	3	—	3	—	ns
t <sub>HZCE<sup>(3)</sup></sub>	$\overline{CE}$ to High-Z Output	—	4	—	5	—	6	—	7	—	7	ns
t <sub>PU<sup>(4)</sup></sub>	$\overline{CE}$ to Power-Up	0	—	0	—	0	—	0	—	0	—	ns
t <sub>PD<sup>(4)</sup></sub>	$\overline{CE}$ to Power-Down	—	8	—	10	—	12	—	15	—	20	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Shaded area = **PREPRODUCTION AVAILABILITY.**
3. Tested with the load in Figure 2. Transition is measured  $\pm 200$  mV from steady-state voltage. Not 100% tested.
4. Not 100% tested.

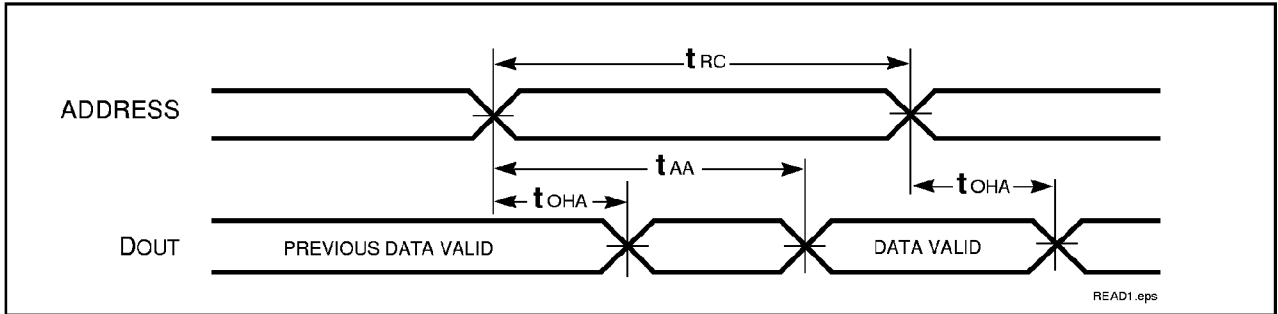
**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

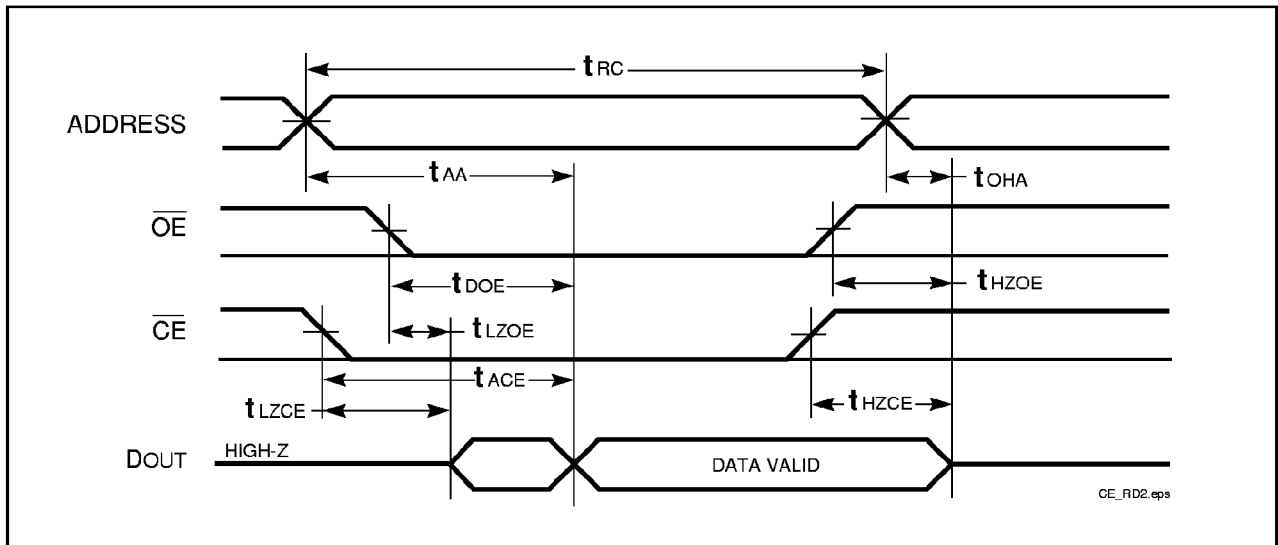
**AC TEST LOADS**

**Figure 1.**

**Figure 2.**

AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup>



READ CYCLE NO. 2<sup>(1,3)</sup>



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)**

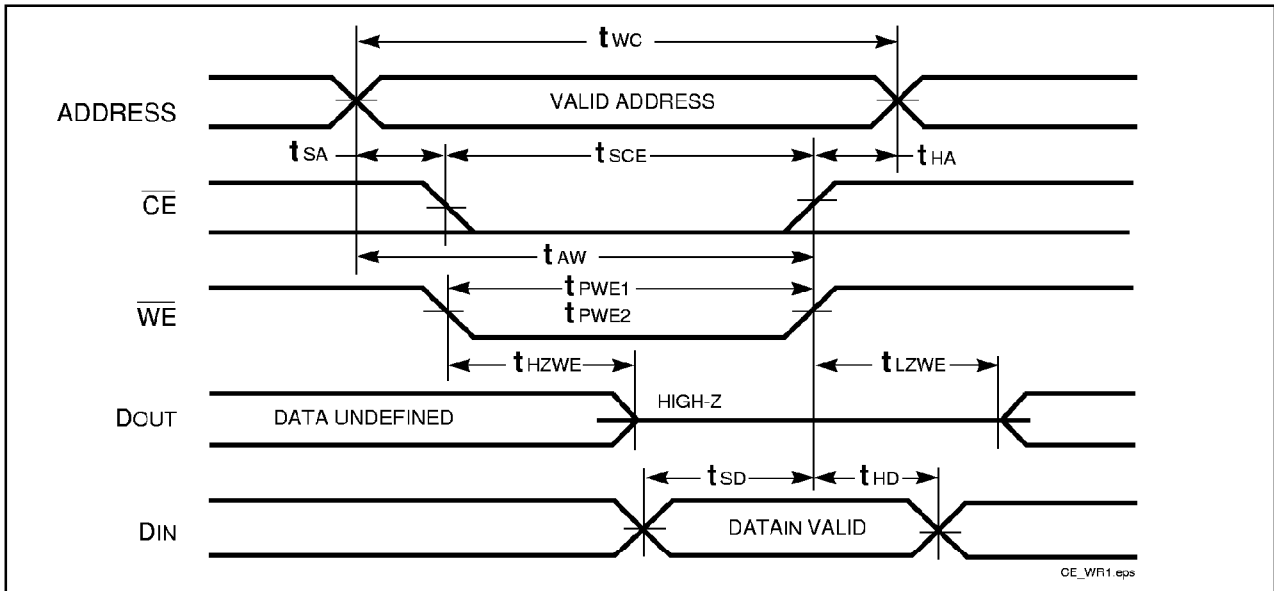
Symbol	Parameter	-8 ns <sup>(3)</sup>		-10 ns <sup>(3)</sup>		-12 ns		-15 ns		-20 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>wc</sub>	Write Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
t <sub>sce</sub>	$\overline{CE}$ to Write End	6.5	—	8	—	8	—	10	—	12	—	ns
t <sub>aw</sub>	Address Setup Time to Write End	6.5	—	8	—	8	—	10	—	12	—	ns
t <sub>ha</sub>	Address Hold from Write End	0	—	0	—	0	—	0	—	0	—	ns
t <sub>sa</sub>	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t <sub>pwe1</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ HIGH)	8	—	10	—	12	—	15	—	20	—	ns
t <sub>pwe2</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ LOW)	6.5	—	7	—	8	—	10	—	12	—	ns
t <sub>sd</sub>	Data Setup to Write End	5	—	5	—	6	—	7	—	10	—	ns
t <sub>hd</sub>	Data Hold from Write End	0	—	0	—	0	—	0	—	0	—	ns
t <sub>hzwe<sup>(4)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	4	—	6	—	7	—	7	ns
t <sub>lzwe<sup>(4)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	0	—	0	—	ns

**Notes:**

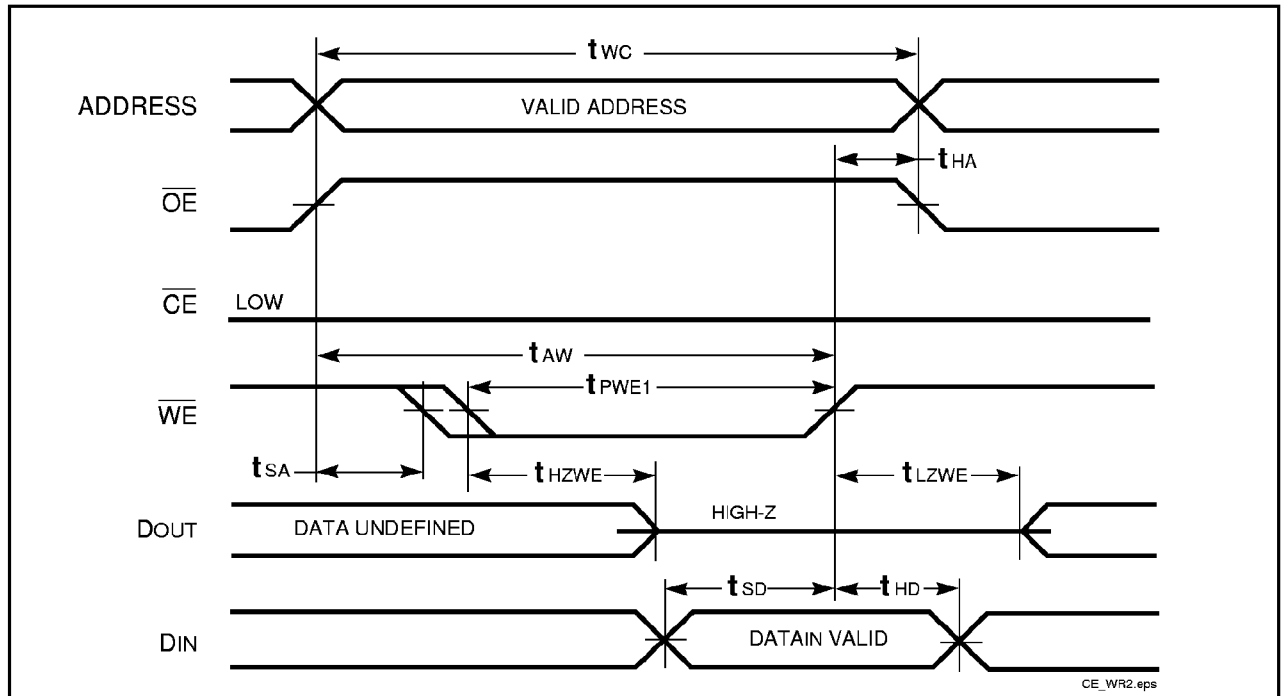
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Shaded area = **PREPRODUCTION AVAILABILITY**.
4. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS**

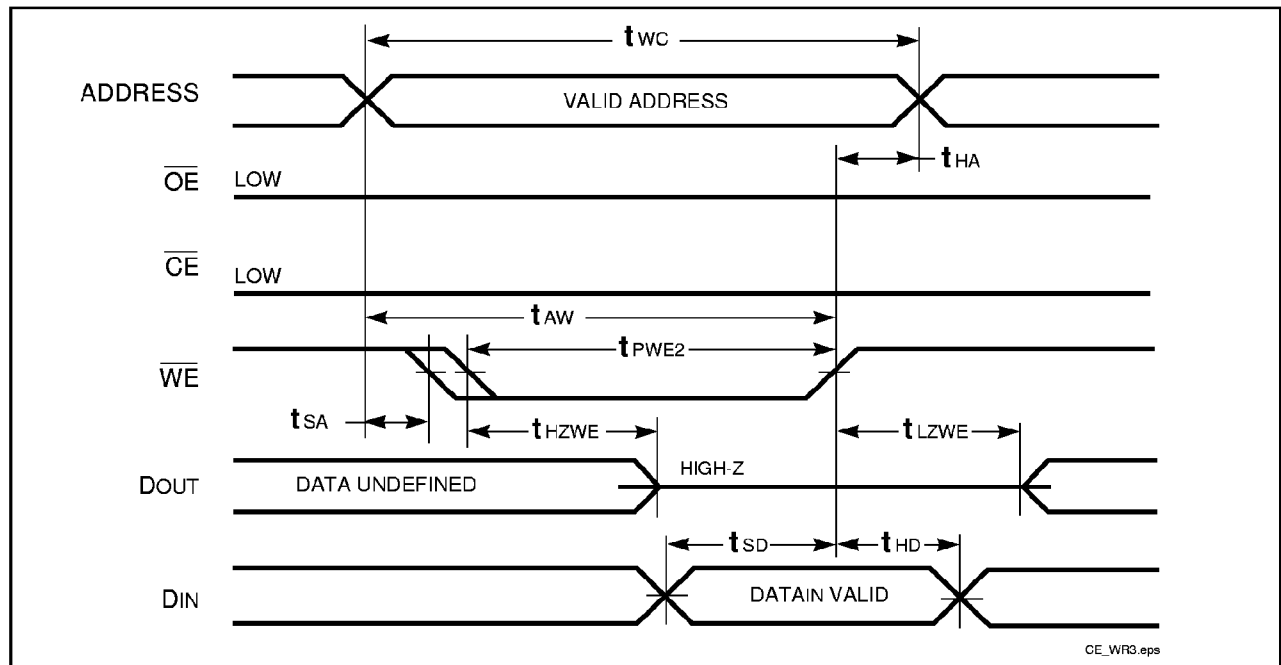
**WRITE CYCLE NO. 1 ( $\overline{CE}$  Controlled,  $\overline{OE}$  is HIGH or LOW) <sup>(1)</sup>**



**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled,  $\overline{OE}$  is HIGH During Write Cycle) <sup>(1,2)</sup>



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled,  $\overline{OE}$  is LOW During Write Cycle) <sup>(1)</sup>



**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .