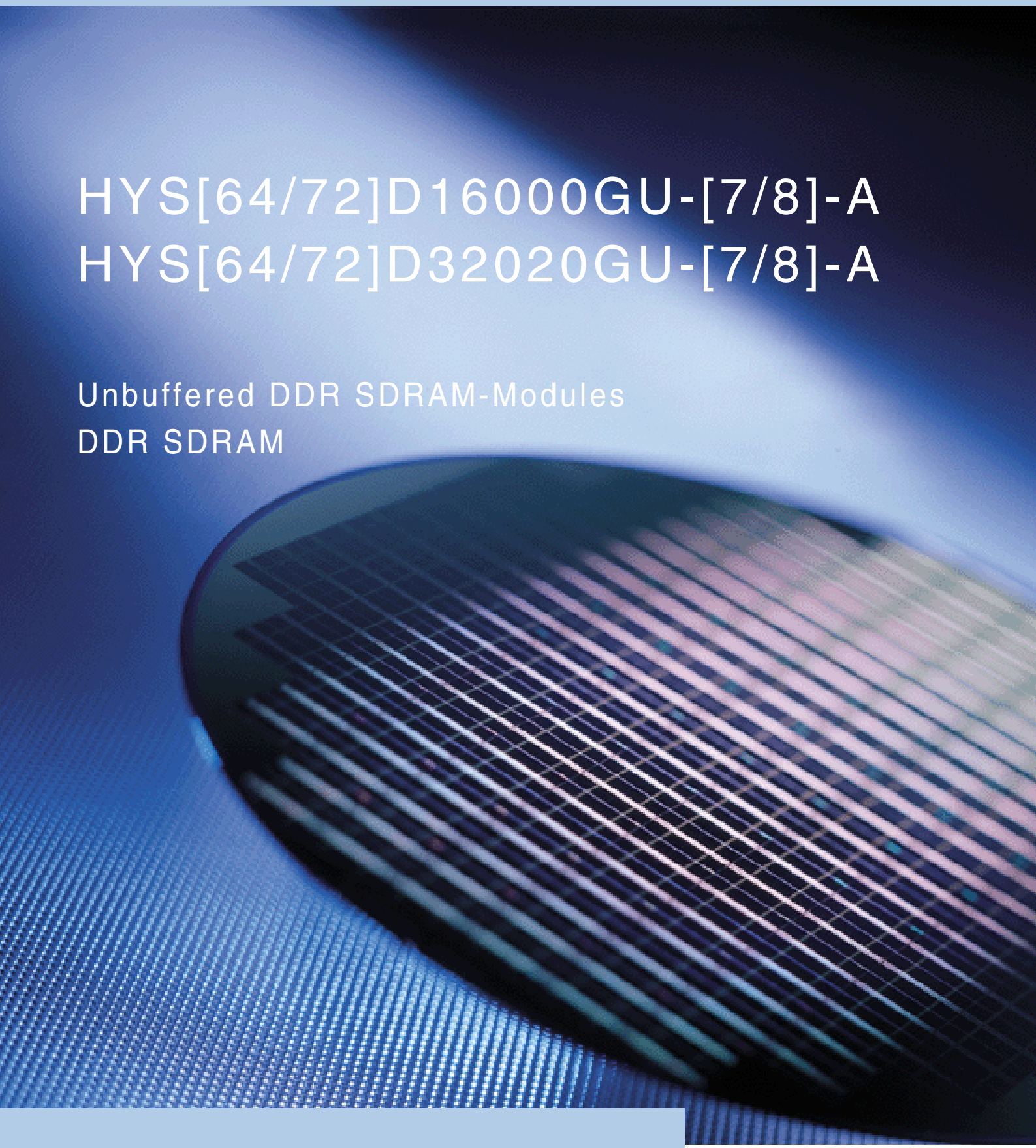
Data Sheet, Rev. 1.03, Jan. 2004

HYS[64/72]D16000GU-[7/8]-A
HYS[64/72]D32020GU-[7/8]-A

Unbuffered DDR SDRAM-Modules
DDR SDRAM



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HYS[64/72]D32020GU-[7/8]-A

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DDR SDRAM

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Page	Subjects (major changes since last revision)
all	Editorial changes

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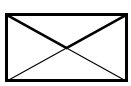

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1 Overview

1.1 Features

- 184-pin Unbuffered 8-Byte Dual-In-Line DDR SDRAM non-parity and ECC-Modules for PC and Server main memory applications
- One rank 16M x 64, 16M x 72 and two rank 32M x 64, 32M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) Single + 2.5 V (± 0.2 V) power supply
- Built with 128 Mb DDR SDRAMs organised as 16Mb x 8 in 66-Lead TSOPII package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- JEDEC standard MO-206 form factor:
  133.35 mm × 31.75 mm × 4.00 mm max.
- JEDEC standard reference layout
- Gold plated contacts

Table 1 Performance -8/-7

Part Number Speed Code			–7	–8	Unit
Speed Grade	Component		DDR266A	DDR200	—
	Module		PC2100-2033	PC1600-2022	—
max. Clock Frequency	@CL2.5	$f_{CK2.5}$	143	125	MHz
	@CL2	f_{CK2}	133	100	MHz

1.2 Description

The HYS64/72D16000GU and HYS64/72D32020GU are industry standard 184-pin 8-byte Dual in-line Memory Modules (DIMMs) organized as 16M x 64 and 32M × 64 for non-parity and 16M x 72 and 32M x 72 for ECC main memory applications. The memory array is designed with 128Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Table 2 Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC2100 (CL=2):			
HYS64D16000GU-7-A	PC2100-20330-A1	one rank 128 MB DIMM	128 MBit (x8)
HYS72D16000GU-7-A	PC2100-20330-A1	one rank 128 MB ECC-DIMM	128 MBit (x8)
HYS64D32020GU-7-A	PC2100-20330-B1	two ranks 256 MB DIMM	128 MBit (x8)
HYS72D32020GU-7-A	PC2100-20330-B1	two ranks 256 MB ECC-DIMM	128 MBit (x8)
PC1600 (CL=2):			
HYS64D16000GU-8-A	PC1600-20220-A1	one rank 128 MB DIMM	128 MBit (x8)
HYS72D16000GU-8-A	PC1600-20220-A1	one rank 128 MB ECC-DIMM	128 MBit (x8)
HYS64D32020GU-8-A	PC1600-20220-B1	two ranks 256 MB DIMM	128 MBit (x8)
HYS72D32020GU-8-A	PC1600-20220-B1	two ranks 256 MB ECC-DIMM	128 MBit (x8)

Note: All part numbers end with a place code, designating the silicon-die revision. Reference information available on request. Example: HYS 72D32020GU-8-A, indicating Rev.A dies are used for the SDRAM components. The Compliance Code is printed on the module labels and describes the speed sort fe. “PC2100”, the latencies (f.e. “20330” means CAS latency = 2, trcd latency = 3 and trp latency =3) and the Raw Card used for this module.

2 Pin Configuration

Table 3 Pin Definitions and Functions

Symbol	Type[1)]	Function
A0 - A12	I	Address Inputs
BA0, BA1	I	Bank Selects
DQ0 - DQ63	I/O	Data Input/Output
CB0 - CB7	I/O	Check Bits (×72 organization only)
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I	Command Inputs
CKE0 - CKE1	I	Clock Enable
DQS0 - DQS8	I/O	SDRAM low data strobes
CK0 - CK2,	I	SDRAM clock (positive lines)
$\overline{CK0}$ - $\overline{CK2}$	I	SDRAM clock (negative lines)
DM0 - DM8 DQS9 - DQS17	I I/O	SDRAM low data mask/ high data strobes
$\overline{S0}$, $\overline{S1}$	I	Chip Selects for Rank0 and Rank1
V_{DD}	PWR	Power (+2.5 V)
V_{SS}	GND	Ground
V_{DDQ}	PWR	I/O Driver power supply
V_{DDID}	PWR	VDD Indentification flag
V_{REF}	AI	I/O reference supply
V_{DDSPD}	PWR	Serial EEPROM power supply
SCL	I	Serial bus clock
SDA	I/O	Serial bus data line
SA0 - SA2	I	slave address select
NC	NC	Not Connected

1) I: Input; O: Output; I/O: bidirectional In-/Output; AI: Analog Input; PWR: Power Supply; GND: Signal Ground; NC: Not Connected

Note: S1 and CKE1 are used on two rank modules only

Table 4 Pin Configuration

Frontside				Backside			
PIN#	**Symbol**	**PIN#**	**Symbol**	**PIN#**	**Symbol**	**PIN#**	**Symbol**
1	V_{REF}	48	A0	93	V_{SS}	140	NC / DM8/DQS17
2	DQ0	49	NC / CB2	94	DQ4	141	A10
3	V_{SS}	50	V_{SS}	95	DQ5	142	NC / CB6
4	DQ1	51	NC / CB3	96	V_{DDQD}	143	V_{DDQD}
5	DQS0	52	BA1	97	DM0/DQS9	144	NC / CB7
6	DQ2	**Key**		98	DQ6	**Key**	
7	V_{DD}			99	DQ7		
8	DQ3	53	DQ32	100	V_{SS}	145	V_{SS}
9	NC	54	V_{DDQ}	101	NC	146	DQ36
10	NC	55	DQ33	102	NC	147	DQ37
11	V_{SS}	56	DQS4	103	NC	148	V_{DD}
12	DQ8	57	DQ34	104	V_{DDQ}	149	DM4/DQS13
13	DQ9	58	V_{SS}	105	DQ12	150	DQ38
14	DQS1	59	BA0	106	DQ13	151	DQ39
15	V_{DDQ}	60	DQ35	107	DM1/DQS10	152	V_{SS}
16	CK1	61	DQ40	108	V_{DD}	153	DQ44
17	CK1	62	V_{DDQ}	109	DQ14	154	$\overline{RAS}$
18	V_{SS}	63	$\overline{WE}$	110	DQ15	155	DQ45
19	DQ10	64	DQ41	111	CKE1	156	V_{DDQ}
20	DQ11	65	$\overline{CAS}$	112	V_{DDQ}	157	$\overline{S0}$
21	CKE0	66	V_{SS}	113	NC (BA2)	158	$\overline{S1}$
22	V_{DDQ}	67	DQS5	114	DQ20	159	DM5/DQS14
23	DQ16	68	DQ42	115	NC / A12	160	V_{SS}
24	DQ17	69	DQ43	116	V_{SS}	161	DQ46
25	DQS2	70	V_{DD}	117	DQ21	162	DQ47
26	V_{SS}	71	NC	118	A11	163	NC
27	A9	72	DQ48	119	DM2/DQS11	164	V_{DDQ}
28	DQ18	73	DQ49	120	V_{DD}	165	DQ52
29	A7	74	V_{SS}	121	DQ22	166	DQ53
30	V_{DDQ}	75	CK2	122	A8	167	NC (A13)
31	DQ19	76	CK2	123	DQ23	168	V_{DD}
32	A5	77	V_{DDQ}	124	V_{SS}	169	DM6/DQS15
33	DQ24	78	DQS6	125	A6	170	DQ54
34	V_{SS}	79	DQ50	126	DQ28	171	DQ55
35	DQ25	80	DQ51	127	DQ29	172	V_{DDQ}
36	DQS3	81	V_{SS}	128	V_{DDQ}	173	NC
37	A4	82	V_{DDID}	129	DM3/DQS12	174	DQ60
38	V_{DD}	83	DQ56	130	A3	175	DQ61
39	DQ26	84	DQ57	131	DQ30	176	V_{SS}

Table 4 Pin Configuration (cont'd)

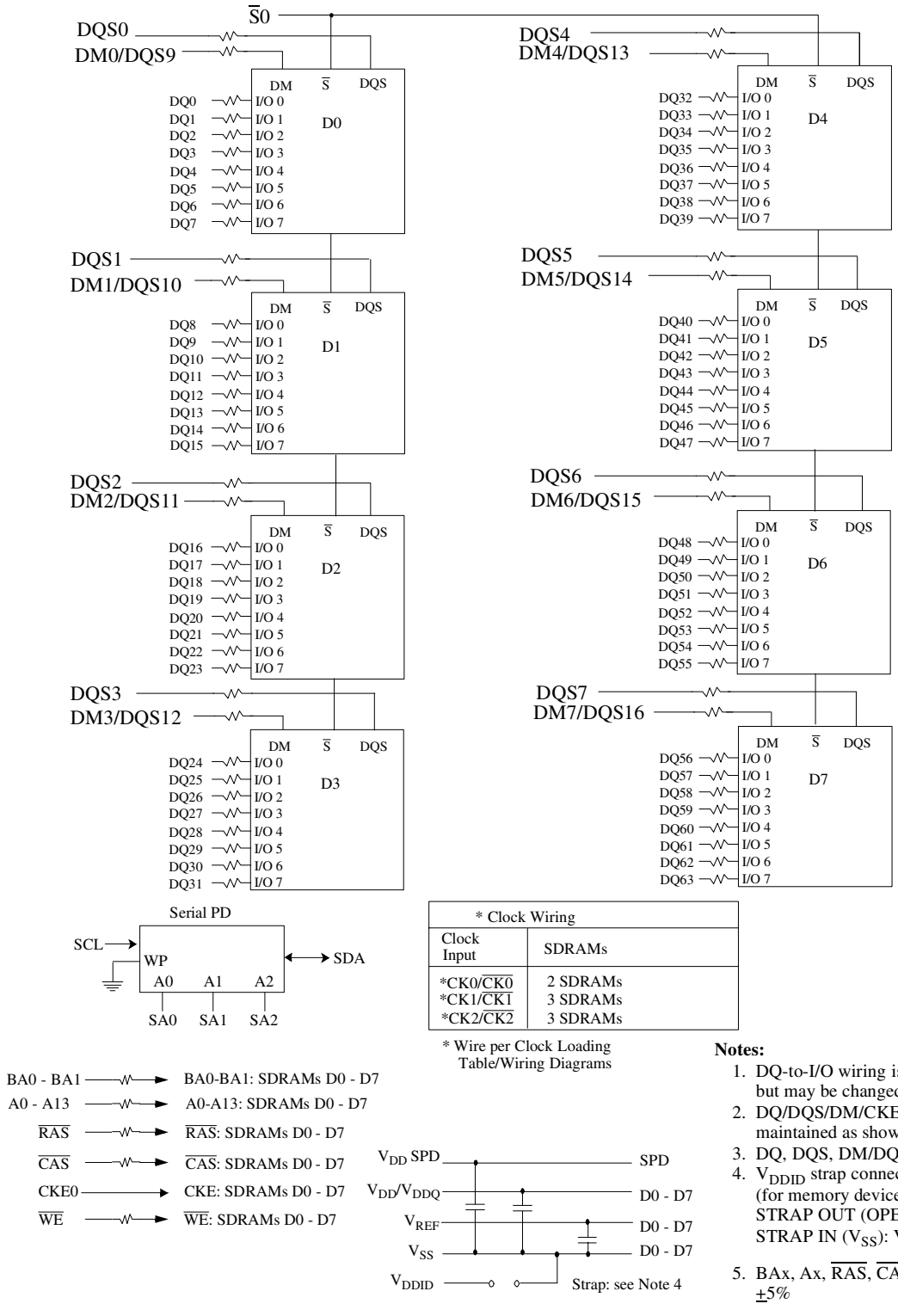
Frontside				Backside			
PIN#	**Symbol**	**PIN#**	**Symbol**	**PIN#**	**Symbol**	**PIN#**	**Symbol**
40	DQ27	85	V_{DD}	132	V_{SS}	177	DM7/DQS16
41	A2	86	DQS7	133	DQ31	178	DQ62
42	V_{SS}	87	DQ58	134	NC / CB4	179	DQ63
43	A1	88	DQ59	135	NC / CB5	180	V_{DDQ}
44	NC / CB0	89	V_{SS}	136	V_{DDQ}	181	SA0
45	NC / CB1	90	NC	137	CK0	182	SA1
46	V_{DD}	91	SDA	138	$\overline{CK0}$	183	SA2
47	NC / DQS8	92	SCL	139	V_{SS}	184	V_{DDSPD}

Note: Pins 44, 45, 47, 49, 51, 134, 135, 140 and 144 are NC ("not connected") on ×64 organised non-ECC modules.

Table 5 Address Format

Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
128 MB	16M × 64	1	16M × 8	8	12/2/10	4K	64 ms	15.6 µs
128 MB	16M × 72	1	16M × 8	9	12/2/10	4K	64 ms	15.6 µs
256 MB	32M × 64	2	16M × 8	16	12/2/10	4K	64 ms	15.6 µs
256 MB	32M × 72	2	16M × 8	18	12/2/10	4K	64 ms	15.6 µs

Note: Pins 44, 45, 47, 49, 51, 134, 135, 140 and 144 are NC ("no-connects") on x64 organised non-ECC modules. A12 is used for 256 Mbit based modules only.



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%
4. V_{DDID} strap connections
   (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 5.1 ohms ±5%

Figure 1 Block Diagram: One Rank 16M × 64 DDR SDRAM DIMM Module HYS64D16000GU using ×8 organized SDRAMs

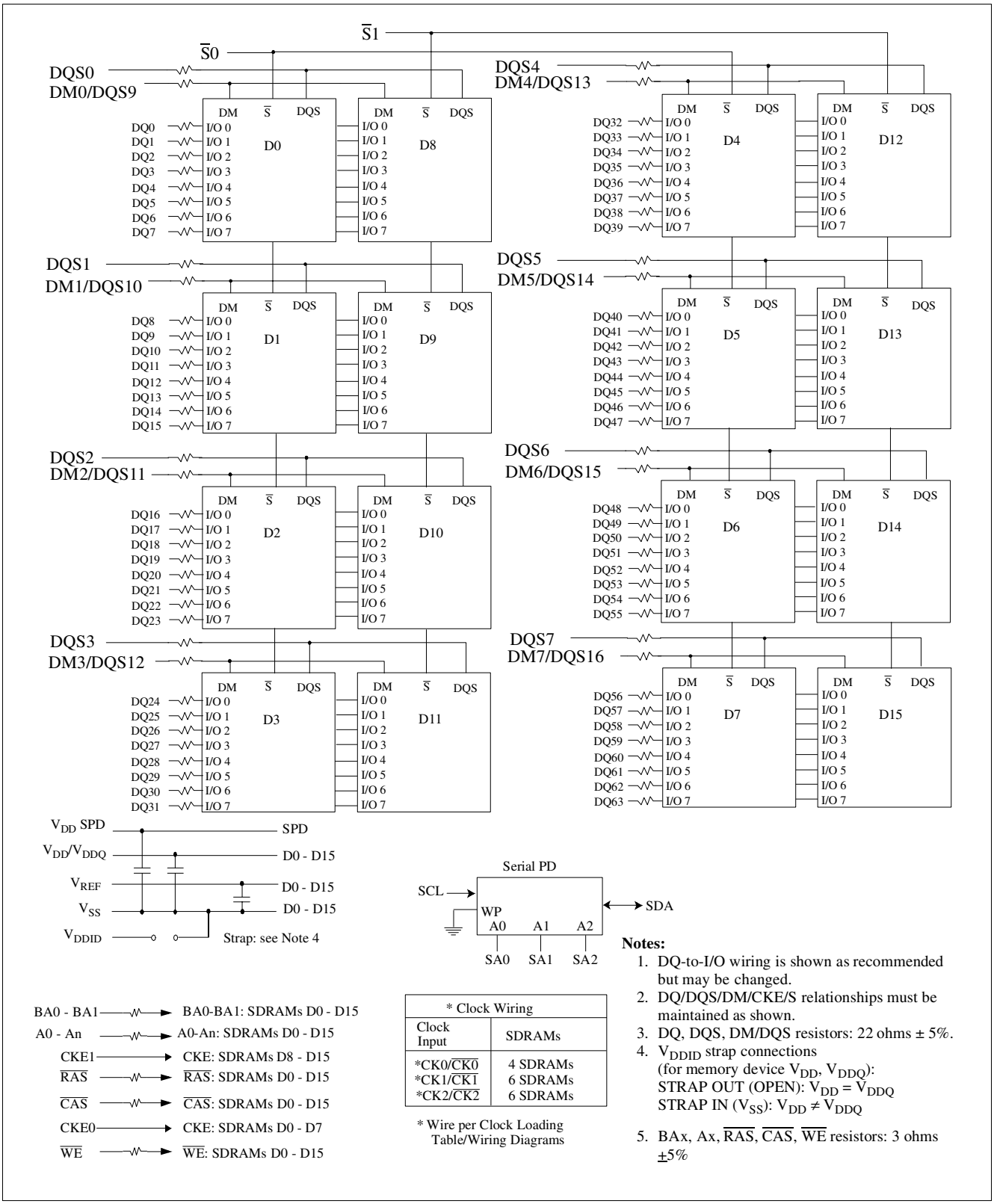
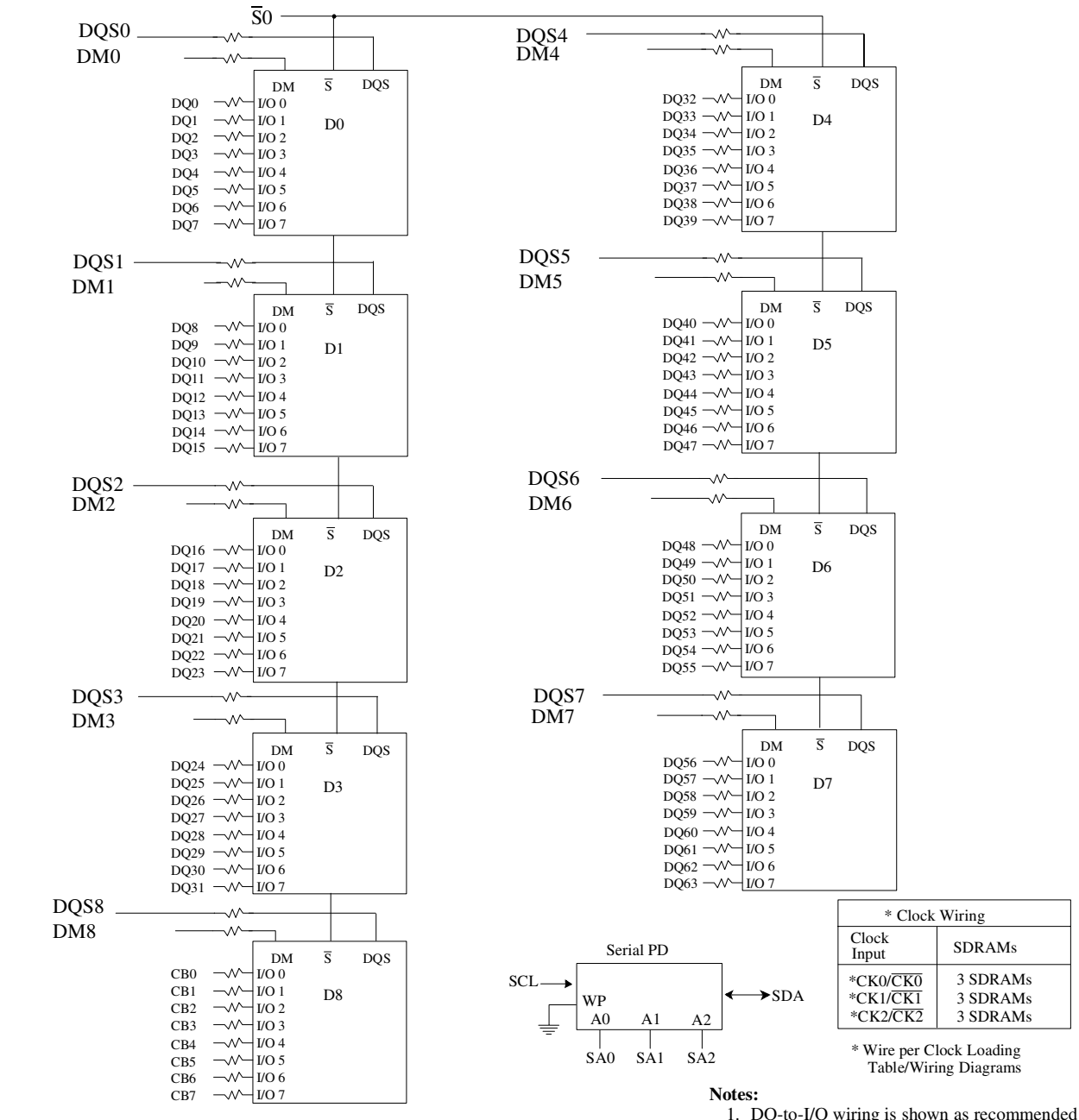


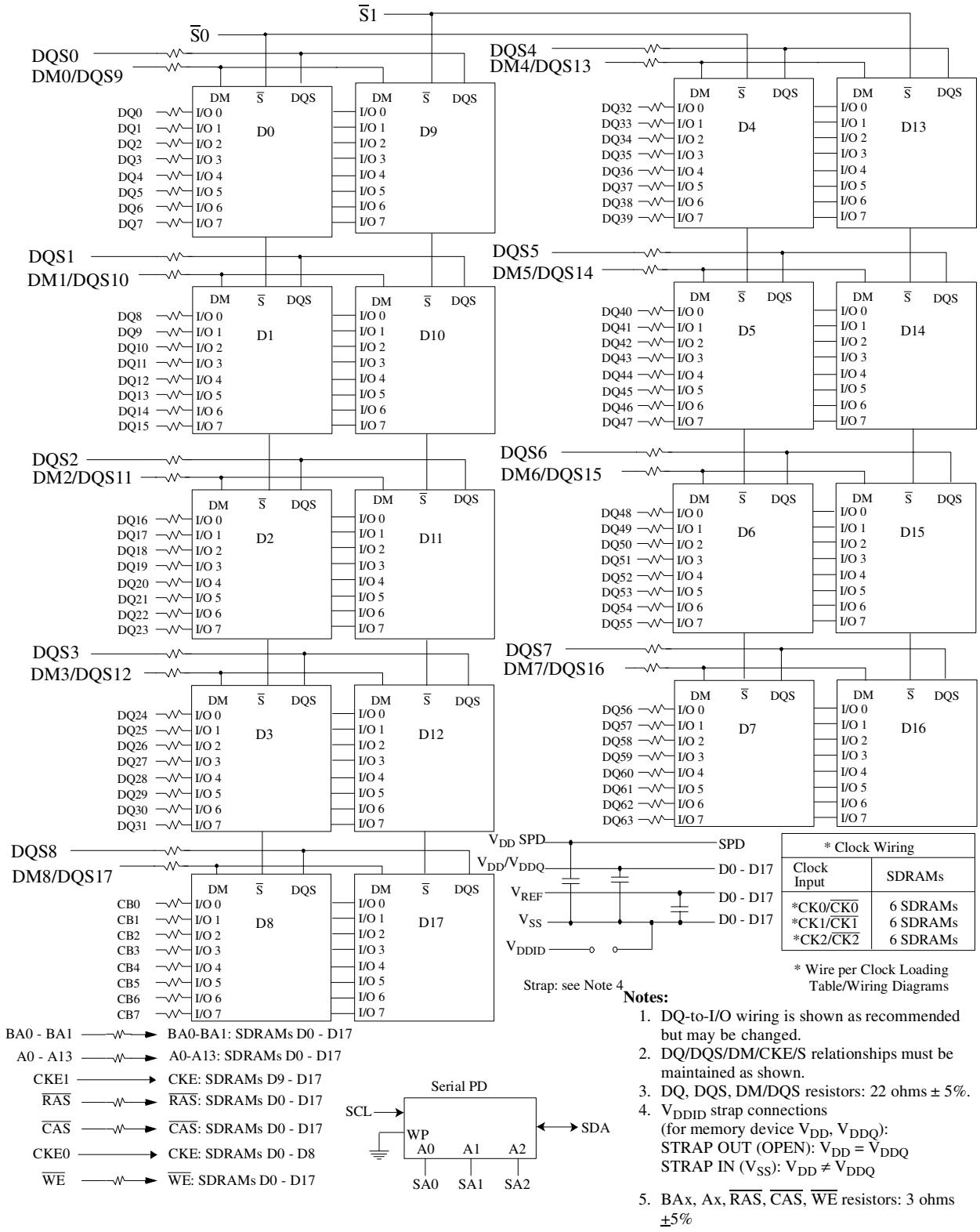
Figure 2 Block Diagram: Two Rank 32M × 64 DDR SDRAM DIMM Modules HYS64D32020GU using ×8 Organized SDRAMs



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 5.1 ohm ±5%

Figure 3 Block Diagram: One Rank 16M × 72 DDR SDRAM DIMM Module HYS72D16000GU using ×8 organized SDRAMs



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$
5. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 3 ohms ±5%

Figure 4 Block Diagram: Two Rank 32M × 72 DDR SDRAM DIMM Modules HYS72D32020GU using ×8 Organized SDRAMs

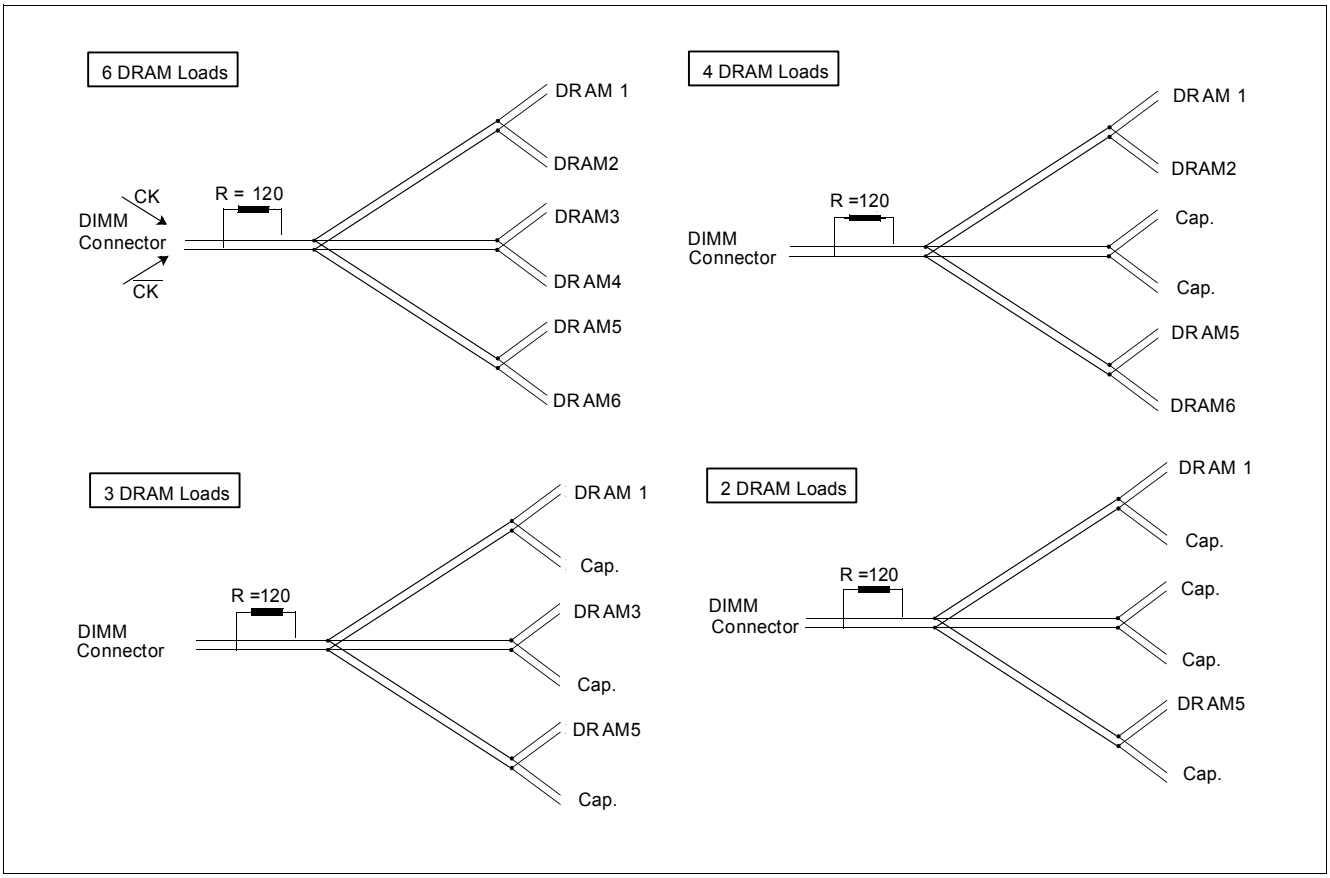


Figure 5 Clock Net Wiring

3 Electrical Characteristics

3.1 Operating Conditions

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	P_D	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

Attention: Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

Table 7 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	[2]
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	[3]
I/O Termination Voltage (System)	V_{TT}	$V_{REF} - 0.04$		$V_{REF} + 0.04$	V	[4]
Input High (Logic1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$		$V_{DDQ} + 0.3$	V	[7]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3		$V_{REF} - 0.15$	V	[7]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3		$V_{DDQ} + 0.3$	V	[7]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		$V_{DDQ} + 0.6$	V	[7][5]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[6]
Input Leakage Current	I_I	–2		2	µA	Any input 0 V $\leq V_{IN} \leq V_{DD}$; All other pins not under test = 0 V [7][8]
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; 0 V $\leq V_{OUT} \leq V_{DDQ}$ [7]
Output High Current, Normal Strength Driver	I_{OH}	—		–16.2	mA	V_{OUT} = 1.95 V [7]
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V [7]

1) 0 °C $\leq T_A \leq$ 70 °C

2) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

3) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.

5) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

6) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

7) Inputs are not recognized as valid until V_{REF} stabilizes.

8) Values are shown per component

3.2 Current Specification and Conditions

Table 8 I_{DD} Conditions

Parameter	Symbol
Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet.	I_{DD1}
Precharge Power-Down Standby Current all banks idle; power-down mode; CKE ≤ $V_{IL,MAX}$	I_{DD2P}
Precharge Floating Standby Current $\overline{CS}$ ≥ $V_{IH,,MIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$; address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ $V_{IH,MIN}$; V_{IN} = V_{REF} for DQ, DQS and DM; address and other control inputs stable at ≥ $V_{IH,MIN}$ or ≤ $V_{IL,MAX}$.	I_{DD2Q}
Active Power-Down Standby Current one bank active; power-down mode; CKE ≤ V_{ILMAX}; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD3P}
Active Standby Current one bank active; $\overline{CS}$ ≥ $V_{IH,MIN}$; CKE ≥ $V_{IH,MIN}$; t_{RC} = $t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; I_{OUT} = 0 mA	I_{DD4R}
Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	I_{DD4W}
Auto-Refresh Current t_{RC} = t_{RFCMIN}, burst refresh	I_{DD5}
Self-Refresh Current CKE ≤ 0.2 V; external clock on	I_{DD6}
Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet.	I_{DD7}

Table 9 I_{DD} Specification and Conditions -8/-7

Part Number & Organization	HYS64D16000GU-8-A	HYS64D16000GU-7-A	HYS72D16000GU-8-A	HYS72D16000GU-8-A	HYS64D32020GU-8-A	HYS64D32020GU-7-A	HYS72D32020GU-8-A	HYS72D32020GU-7-A	Unit	Note [1)2)]
	128MB		128MB		256MB		256MB			
	×64		×72		×64		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	-8	-7	-8	-7	-8	-7	-8	-7		
Symbol	**max**		**max**		**max**		**max**			
I_{DD0}	680	720	765	810	960	1080	1080	1215	mA	3)
I_{DD1}	800	880	900	990	1080	1240	1215	1395	mA	3)4)
I_{DD2P}	36	40	40.5	45	72	80	81	90	mA	5)
I_{DD2F}	280	360	315	405	560	720	630	810	mA	5)
I_{DD2Q}	280	360	315	405	560	720	630	810	mA	5)
I_{DD3P}	120	120	135	135	240	240	270	270	mA	5)
I_{DD3N}	280	360	315	405	560	720	630	810	mA	5)
I_{DD4R}	720	880	810	990	1000	1240	1125	1395	mA	3)4)
I_{DD4W}	760	880	855	990	1040	1240	1170	1395	mA	3)
I_{DD5}	1440	1520	1620	1710	1720	1880	1935	2115	mA	3)
I_{DD6}	20	20	22.5	22.5	40	40	45	45	mA	5)
I_{DD7}	2160	2240	2430	2520	2440	2600	2745	2925	mA	3)4)

1) Module I_{DD} values are calculated on the basis of component I_{DD} and can be measured differently according to DQ loading capacity.

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the I_{DDx} values of the component data sheet as follows:
m × I_{DDx}[component] + **n** × I_{DD3N}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included in the calculations (see note 1)

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

3.3 AC Characteristics

Table 10 AC Timing - Absolute Specifications –8/–7

Parameter	Symbol	–8		–7		Unit	Note/ Test Condition [1]
		DDR200		DDR266A			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	$t_{CK2.5}$	8	12	7	12	ns	CL = 2.5 2)3)4)5)
	t_{CK2}	10	12	7.5	12	ns	CL = 2.0 2)3)4)5)
	$t_{CK1.5}$	10	12	—	—	ns	CL = 1.5 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.6	—	0.5	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.6	—	0.5	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.5	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	t_{DIPW}	2.0	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.6	—	+0.5	ns	2)3)4)5)
Data hold skew factor	t_{QHS}	—	1.0	—	0.75	ns	2)3)4)5)
DQ/DQS output hold time	t_{QH}	t_{HP} – t_{QHS}	—	t_{HP} – t_{QHS}	—	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Address and control input setup time	t_{IS}	1.1	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.1	—	1.0	—	ns	slow slew rate 3)4)5)6)10)

Table 10 AC Timing - Absolute Specifications –8/–7

Parameter	Symbol	–8		–7		Unit	Note/ Test Condition [1]
		DDR200		DDR266A			
		Min.	Max.	Min.	Max.		
Address and control input hold time	t_{IH}	1.1	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.1	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	CL > 1.5 2)3)4)5)
	$t_{RPRE1.5}$	0.9	1.1	NA		t_{CK}	CL = 1.5 2)3)4)5)11)
Read preamble setup time	t_{RPRES}	1.5	—	NA		ns	2)3)4)5)12)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active to Precharge command	t_{RAS}	50	120E+3	45	120E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	70	—	65	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	80	—	75	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	20	—	20	—	ns	2)3)4)5)
Precharge command period	t_{RP}	20	—	20	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	20	—	20	—	ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	15	—	15	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{wr}/t_{CK}) + (t_{rp}/t_{CK})$				t_{CK}	2)3)4)5)13)
Internal write to read command delay	t_{WTR}	1	—	1	—	t_{CK}	CL > 1.5 2)3)4)5)
	$t_{WTR1.5}$	2	—	—	—	t_{CK}	CL = 1.5 2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	80	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)14)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V

2) Input slew rate ≥ 1 V/ns for DDR266, and = 1 V/ns for DDR200

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) CAS Latency 1.5 operation is supported on DDR200 devices only

12) t_{RPRES} is defined for CL = 1.5 operation only

13) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

14) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

4 SPD Contents

Table 11 SPD Codes for PC1600 Modules -8

Byte#	Description		128MB x64 1rank –8	128MB x72 1rank –8	128MB x64 2ranks –8	128MB x64 2ranks –8
			hex.	hex.	hex.	hex.
0	Number of SPD Bytes	128	80	80	80	80
1	Total Bytes in Serial PD	256	08	08	08	08
2	Memory Type	DDR-SDRAM	07	07	07	07
3	Number of Row Addresses	12	0C	0C	0C	0C
4	Number of Column Addresses	10	0A	0A	0A	0A
5	Number of DIMM Banks	1/2	01	01	02	02
6	Module Data Width	×64/×72	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	SSTL_2.5	04	04	04	04
9	SDRAM Cycle Time at CL = 2.5	8 ns	80	80	80	80
10	Access Time from Clock at CL = 2.5	0.8 ns	80	80	80	80
11	DIMM config	non-ECC/ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh 15.6 ms	80	80	80	80
13	SDRAM Width, Primary	×8	08	08	08	08
14	Error Checking SDRAM Data Witdh	na/×8	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E	0E
17	Number of SDRAM Banks	4	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 2.5	0C	0C	0C	0C
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 1	02	02	02	02
21	SDRAM DIMM Module Attributes	unbuffered	20	20	20	20
22	SDRAM Device Attributes: General	–	C0	C0	C0	C0
23	Min. Clock Cycle Time at CAS Latency = 2	10 ns	A0	A0	A0	A0
24	Access Time from Clock for CL = 2	0.8 ns	80	80	80	80
25	Minimum Clock Cycle Time for CL = 1.5	not supported	00	00	00	00

Table 11 SPD Codes for PC1600 Modules -8 (cont'd)

Byte#	Description		128MB x64 1rank –8	128MB x72 1rank –8	128MB x64 2ranks –8	128MB x64 2ranks –8
			hex.	hex.	hex.	hex.
26	Access Time from Clock at CL = 1.5	not supported	00	00	00	00
27	Minimum Row Precharge Time	20 ns	50	50	50	50
28	Minimum Row Act. to Row Act. Delay t_{RRD}	15 ns	3C	3C	3C	3C
29	Minimum RAS to CAS Delay t_{RCD}	20 ns	50	50	50	50
30	Minimum RAS Pulse Width t_{RAS}	50 ns	32	32	32	32
31	Module Bank Density (per Bank)	128 MByte	20	20	20	20
32	Addr. and Command Setup Time	1.1 ns	B0	B0	B0	B0
33	Addr. and Command Hold Time	1.1 ns	B0	B0	B0	B0
34	Data Input Setup Time	0.6 ns	60	60	60	60
35	Data Input Hold Time	0.6 ns	60	60	60	60
36 to 40	Superset Information	–				
41	Minimum Core Cycle Time t_{RC}	70 ns	46	46	46	46
42	Min. Auto Refresh Cmd Cycle Time t_{FRC}	80 ns	50	50	50	50
43	Maximum Clock Cycle Time t_{CK}	12 ns	30	30	30	30
44	Max. DQS-DQ Skew tDQSQ	0.6 ns	3C	3C	3C	3C
45	X-Factor tQHS	1.0 ns	A0	A0	A0	A0
46 to 61	Superset Information	–	00	00	00	00
62	SPD Revision	Revision 0.0	00	00	00	00
63	Checksum for Bytes 0 - 62	–	84	96	85	97
64	Manufactures JEDEC ID Codes	–				
65 to 71	Manufactures	–	Infineon	Infineon	Infineon	Infineon
72	Module Assembly Location	–	–	–	–	–
73 to 90	Module Part Number	–	–	–	–	–
91 to 92	Module Revision Code	–	–	–	–	–
93 to 94	Module Manufacturing Date	–	–	–	–	–
95 to 98	Module Serial Number	–	–	–	–	–
99 to 127	–	–	–	–	–	–
128 to 255	open for Customer use	–	–	–	–	–

Table 12 SPD Codes for PC2100 Modules -7

Byte#	Description		128MB x64 1rank –7	128MB x72 1rank –7	128MB x64 2ranks –7	128MB x64 2ranks –7
			hex.	hex.	hex.	hex.
0	Number of SPD Bytes	128	80	80	80	80
1	Total Bytes in Serial PD	256	08	08	08	08
2	Memory Type	DDR-SDRAM	07	07	07	07
3	Number of Row Addresses	12	0C	0C	0C	0C
4	Number of Column Addresses	10	0A	0A	0A	0A
5	Number of DIMM Banks	1/2	01	01	02	02
6	Module Data Width	×64/×72	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	SSTL_2.5	04	04	04	04
9	SDRAM Cycle Time at CL = 2.5	7 ns	70	70	70	70
10	Access Time from Clock at CL = 2.5	0.75 ns	75	75	75	75
11	DIMM config	non-ECC/ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh 15.6 ms	80	80	80	80
13	SDRAM Width, Primary	×8	08	08	08	08
14	Error Checking SDRAM Data Witdh	na/×8	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E	0E
17	Number of SDRAM Banks	4	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 2.5	0C	0C	0C	0C
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 1	02	02	02	02
21	SDRAM DIMM Module Attributes	unbuffered	20	20	20	20
22	SDRAM Device Attributes: General	–	C0	C0	C0	C0
23	Min. Clock Cycle Time at CAS Latency = 2	7.5 ns	75	75	75	75
24	Access Time from Clock for CL = 2	0.75 ns	75	75	75	75
25	Minimum Clock Cycle Time for CL = 1.5	not supported	00	00	00	00
26	Access Time from Clock at CL = 1.5	not supported	00	00	00	00

Table 12 SPD Codes for PC2100 Modules -7 (cont'd)

Byte#	Description		128MB x64 1rank –7	128MB x72 1rank –7	128MB x64 2ranks –7	128MB x64 2ranks –7
			hex.	hex.	hex.	hex.
27	Minimum Row Precharge Time	20 ns	50	50	50	50
28	Minimum Row Act. to Row Act. Delay t_{RRD}	15 ns	3C	3C	3C	3C
29	Minimum RAS to CAS Delay t_{RCD}	20 ns	50	50	50	50
30	Minimum RAS Pulse Width t_{RAS}	45 ns	2D	2D	2D	2D
31	Module Bank Density (per Bank)	128 MByte	20	20	20	20
32	Addr. and Command Setup Time	0.9 ns	90	90	90	90
33	Addr. and Command Hold Time	0.9 ns	90	90	90	90
34	Data Input Setup Time	0.5 ns	50	50	50	50
35	Data Input Hold Time	0.5 ns	50	50	50	50
36 to 40	Superset Information	–				
41	Minimum Core Cycle Time t_{RC}	65 ns	41	41	41	41
42	Min. Auto Refresh Cmd Cycle Time t_{FRC}	75 ns	4B	4B	4B	4B
43	Maximum Clock Cycle Time t_{CK}	12 ns	30	30	30	30
44	Max. DQS-DQ Skew tDQSQ	0.5 ns	32	32	32	32
45	X-Factor tQHS	0.75 ns	75	75	75	75
46 to 61	Superset Information	–	00	00	00	00
62	SPD Revision	Revision 0.0	00	00	00	00
63	Checksum for Bytes 0 - 62	–	8F	8F	8F	8F
64	Manufactures JEDEC ID Codes	–	C1	C1	C1	C1
65 to 71	Manufactures	–	Infineon	Infineon	Infineon	Infineon
72	Module Assembly Location	–	–	–	–	–
73 to 90	Module Part Number	–	–	–	–	–
91 to 92	Module Revision Code	–	–	–	–	–
93 to 94	Module Manufacturing Date	–	–	–	–	–
95 to 98	Module Serial Number	–	–	–	–	–
99 to 127	–	–	–	–	–	–
128 to 255	open for Customer use	–	–	–	–	–

5 Package Outlines

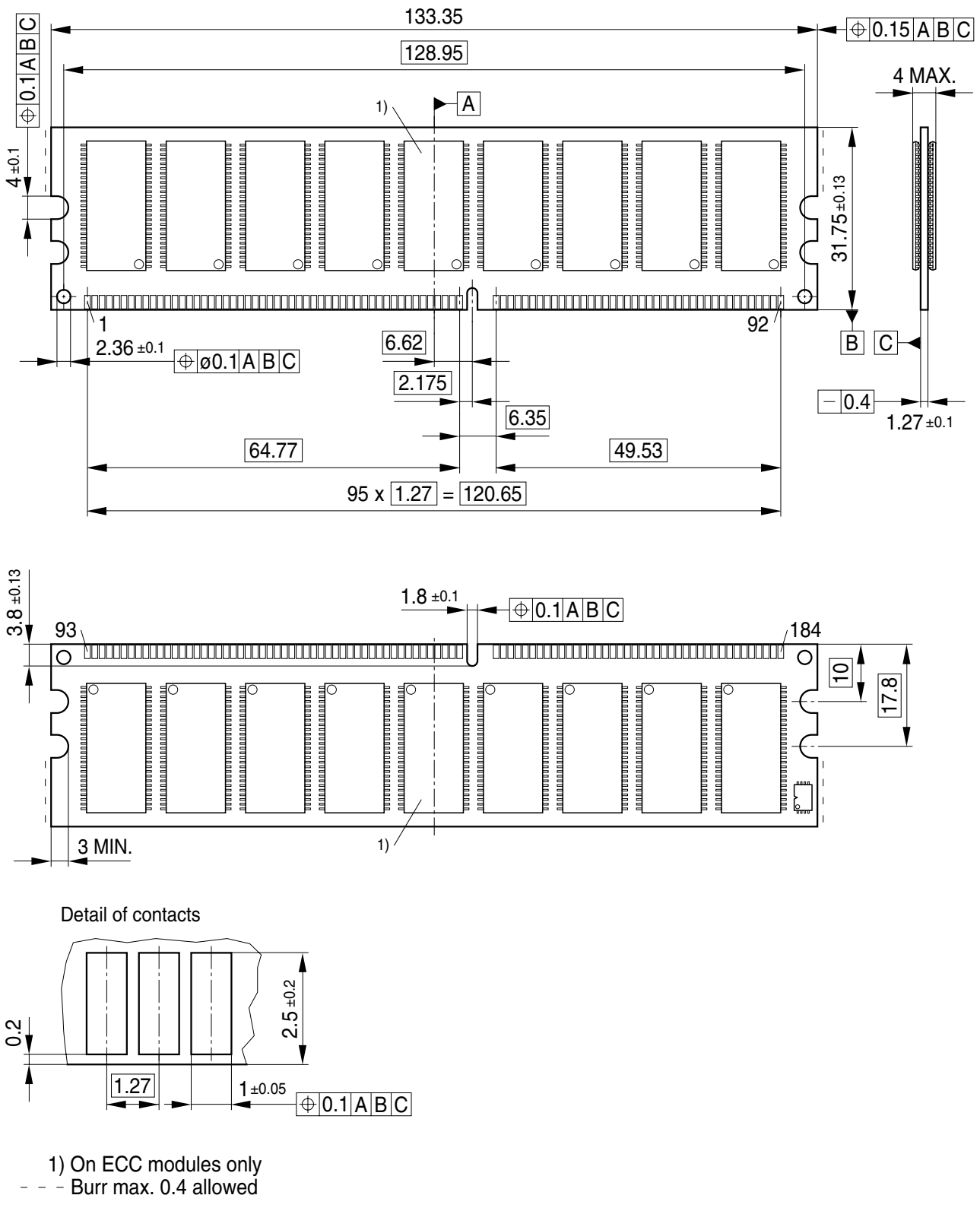


Figure 6 DDR-SDRAM DIMM Module Package

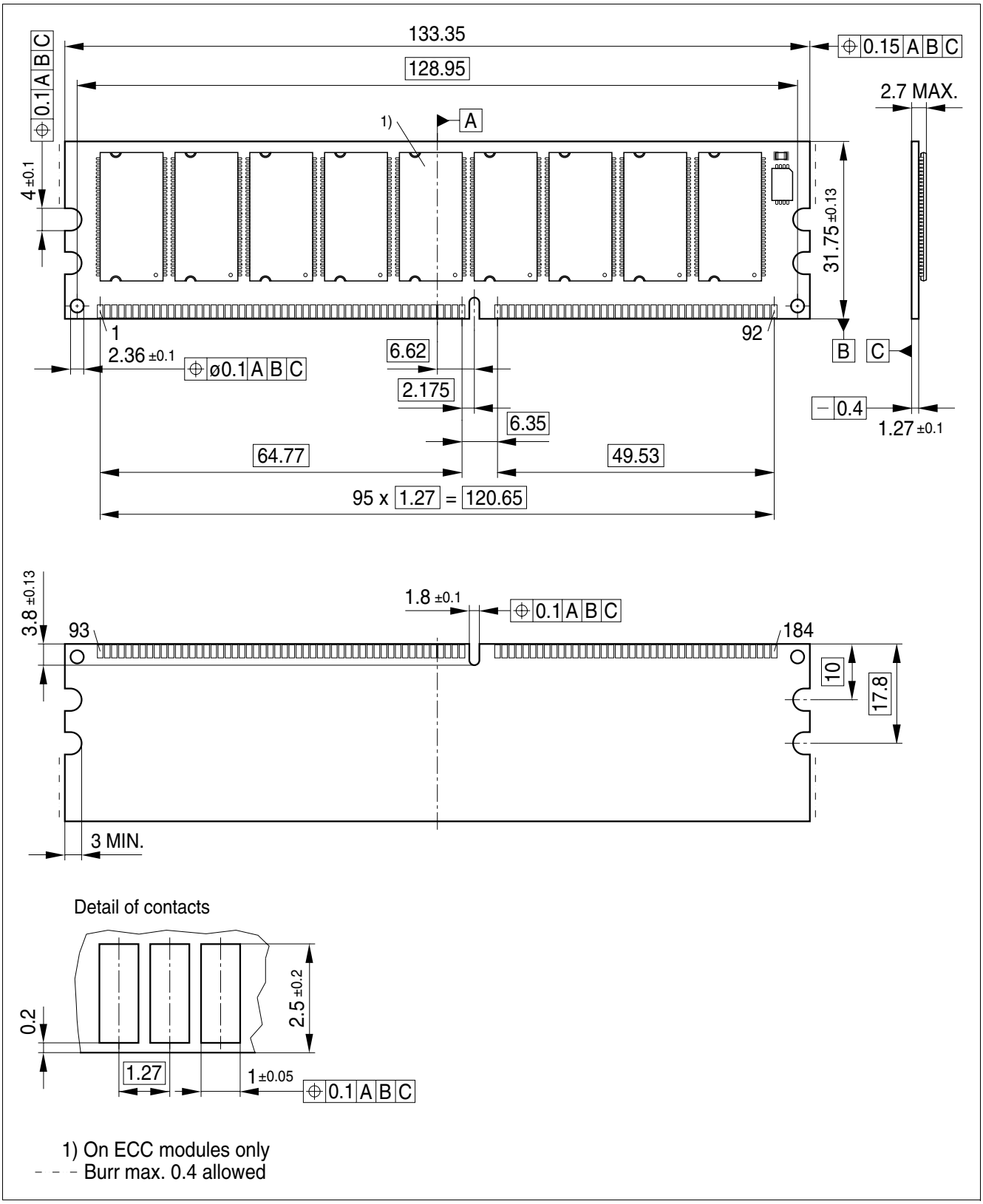


Figure 7 Package Outlines -Raw Card A1 (One Rank Modules)

DDR-SDRAM DIMM Module Package

two banks modules

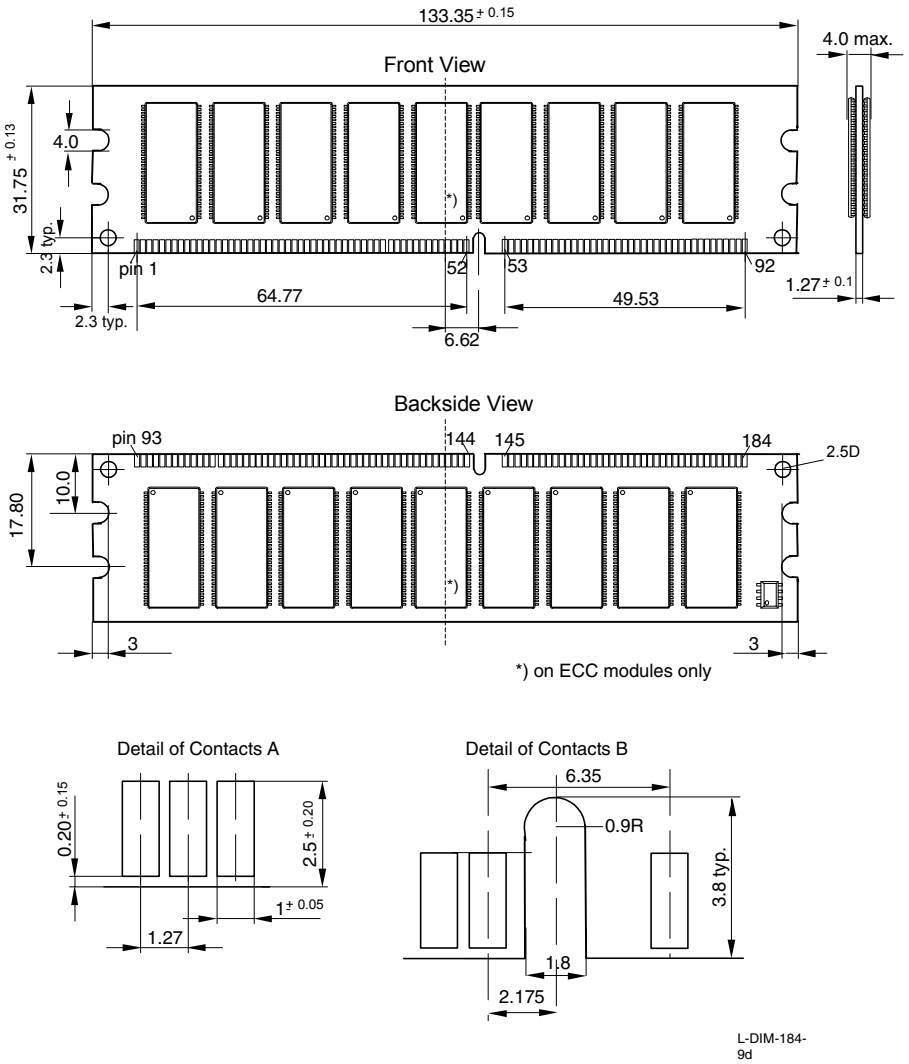


Figure 8 Package Outlines - Raw Card B1 (Two Rank Modules)

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