

# HM100490 Series — Preliminary

65536-Words × 1-Bit Fully Decoded Random Access Memory

## DESCRIPTION

The HM100490 is ECL 100K compatible, 65536-words by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

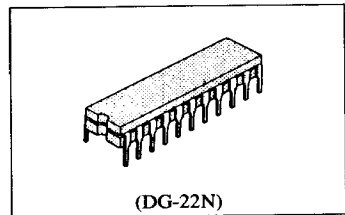
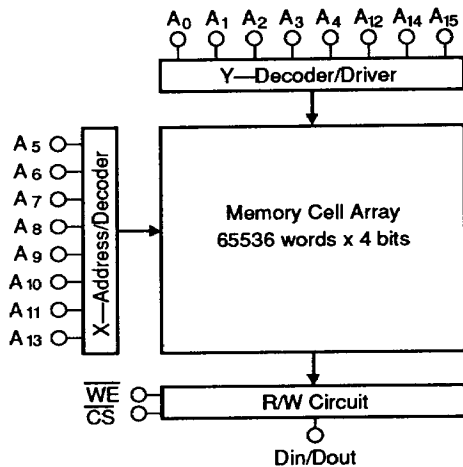
## FEATURES

- 65536 × 1 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time ..... 10/12ns (max.)
- Write Pulse Width ..... 6/8ns (min.)
- Low Power Dissipation ..... .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

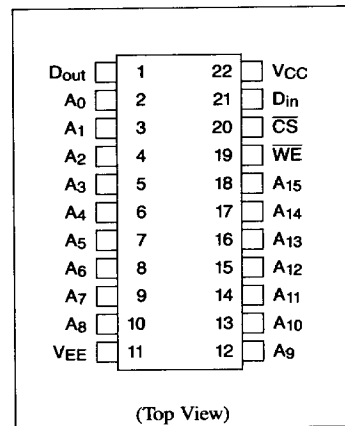
## ORDERING INFORMATION

Type No.	Access Time	Package
HM100490-10	10ns	300 mil 22 pin Cerdip
HM100490-12	12ns	(DG-22N)

## BLOCK DIAGRAM



## PIN ARRANGEMENT



## FUNCTION TABLE

Input			Output	Mode
CS	WE	D <sub>in</sub>		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D <sub>out</sub> *	Read

NOTES: X = Irrelevant;  
\* = Read out noninvert



Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ **ABSOLUTE MAXIMUM RATINGS** ( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Rating	Unit
Supply Voltage	$V_{EE}$ to $V_{CC}$	+0.5 to $\Theta 7.0$	V
Input Voltage	$V_{in}$	+0.5 to $\Theta 3.0$	V
Output Current	$I_{out}$	$\Theta 30$	mA
Storage Temperature	$T_{stg}$	$\Theta 65$ to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{under bias})$	$\Theta 55$ to +125	$^\circ\text{C}$

■ **ELECTRICAL CHARACTERISTICS**

• **DC Characteristics** ( $V_{EE} = -4.5\text{V}$ ,  $R_L = 50\Omega$  to  $-2.0\text{V}$ ,  $T_a = 0$  to  $+85^\circ\text{C}$ , air flow exceeding 2m/sec.)

Item	Symbol	Test Condition	Min.(B)	Typ.	Max.(A)	Unit	
Output Voltage	$V_{OH}$	$V_{in} = V_{IHA}$ or $V_{ILB}$	$\Theta 1025$	$\Theta 955$	$\Theta 880$	mV	
	$V_{OL}$		$\Theta 1810$	$\Theta 1715$	$\Theta 1620$	mV	
Output Threshold Voltage	$V_{OHC}$	$V_{in} = V_{IHB}$ or $V_{ILA}$	$\Theta 1035$	—	—	mV	
	$V_{OLC}$		—	—	$\Theta 1610$	mV	
Input Voltage	$V_{IH}$	Guaranteed Input Voltage High/Low for All Inputs	$\Theta 1165$	—	$\Theta 880$	mV	
	$V_{IL}$		$\Theta 1810$	—	$\Theta 1475$	mV	
Input Current	$I_{IH}$	$V_{in} = V_{IHA}$	—	—	220	$\mu\text{A}$	
	$I_{IL}$	$V_{in} = V_{ILB}$	$\overline{\text{CS}}$	0.5	—	170	$\mu\text{A}$
			Others	$\Theta 50$	—	—	
Supply Current	$I_{EE}$	All Inputs and Outputs Open	$\Theta 140$	—	—	mA	

• **AC Characteristics** ( $V_{EE} = -4.5\text{V} \pm 5\%$ ,  $T_a = 0$  to  $+85^\circ\text{C}$ , air flow exceeding 2m/sec.)

**1. Read Mode**

Item	Symbol	Test Condition	HM100490-10			HM100490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	$t_{ACS}$		—	—	6	—	—	8	ns
Chip Select Recovery Time	$t_{RCS}$		—	—	6	—	—	8	ns
Address Access Time	$t_{AA}$		—	—	10	—	—	12	ns

**2. Write Mode**

Item	Symbol	Test Condition	HM100490-10			HM100490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Pulse Width	$t_w$	$t_{WSA} = t_{wSA}$ min.	6	—	—	8	—	—	ns
Data Setup Time	$t_{WSD}$		2	—	—	2	—	—	ns
Data Hold Time	$t_{WHD}$		2	—	—	2	—	—	ns
Address Setup Time	$t_{WSA}$	$t_w = t_w$ min.	2	—	—	2	—	—	ns
Address Hold Time	$t_{WHA}$		2	—	—	2	—	—	ns
Chip Select Setup Time	$t_{WSCS}$		2	—	—	2	—	—	ns
Chip Select Hold Time	$t_{WHCS}$		2	—	—	2	—	—	ns
Write Disable Time	$t_{WS}$		—	—	6	—	—	8	ns
Write Recovery Time	$t_{WR}$		—	—	12	—	—	14	ns



**3. Rise/Fall Time**

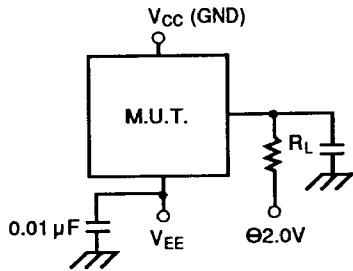
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	$t_r$		—	2	—	ns
Output Fall Time	$t_f$		—	2	—	ns

**4. Capacitance**

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	$C_{in}$		—	3	—	pF
Output Capacitance	$C_{out}$		—	5	—	pF

**■ TEST CIRCUIT AND WAVEFORMS**

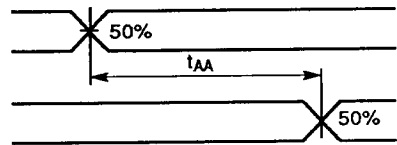
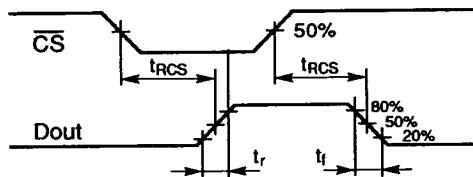
**1. Loading Condition**



**2. Input Pulse**



**3. Read Mode**



4. Write Mode

