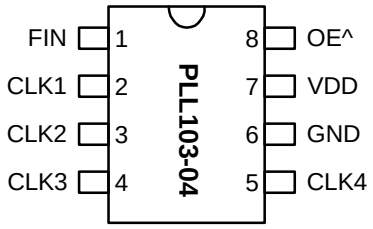
1-to-4 Clock Distribution Buffer

FEATURES

- 4 outputs identical to FIN.
- Low skew (< 250 ps between outputs).
- Input / Output frequency range 0 160 MHz
- 25mA drive capability at TTL levels.
- 70mA drive capability at CMOS levels.
- Output enable mode available to tri-state all outputs.
- 3.3V operation.
- Available in 8-Pin 150mil SOIC.

PIN CONFIGURATION



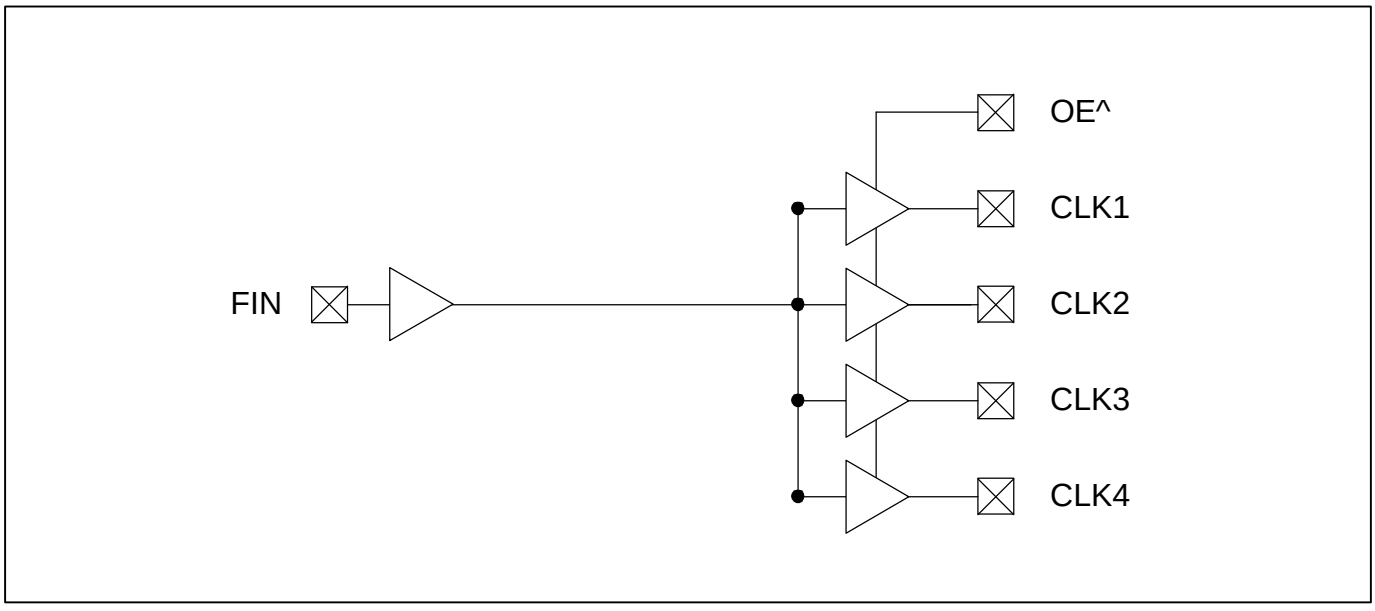
FIN = 0 ~ 160 Mhz

Note: ^: Internal pull-up (30kΩ)

DESCRIPTIONS

The PLL103-04 is a 1-to-4 Clock Distribution Buffer, reproducing the reference input frequency (FIN) at 4 different outputs. It is designed to minimize skew between outputs and provides TTL and CMOS compatible output levels. An output enable selector is available to tri-state all outputs.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
FIN	1	I	Input Clock Frequency (FIN range 0 ~ 160MHz).
CLK1	2	O	Buffered Clock Output.
CLK2	3	O	Buffered Clock Output.
CLK3	4	O	Buffered Clock Output.
CLK4	5	O	Buffered Clock Output.
GND	6	P	Ground.
VDD	7	P	3.3V Power Supply.
OE	8	I	Output Enable. Tri-states all outputs if low. Internal pull-up resistor of 30 kΩ

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{CC}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{CC}+0.5	V
Output Voltage Range	V_O	-0.5	V_{CC}+0.5	V
Soldering Temperature			260	°C
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature		0	70	°C
ESD Voltage			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. Electrical Characteristics

V_{DD} = 3.0~3.6V, unless otherwise stated

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN} = 0V		19	50.0	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.10	100.0	µA
Output Low Current	I_{OL}	V_{OL} = 1.5 V		50		mA
Output High Current	I_{OH}	V_{OH} = 1.5 V		50		mA
Power Down Supply Current	I_{DD}	REF = 0MHz		0.3	50.0	µA
Supply Current	I_{DD}	Unloaded outputs at 75MHz, SEL inputs at V_{DD} or GND		30.0	40.0	mA

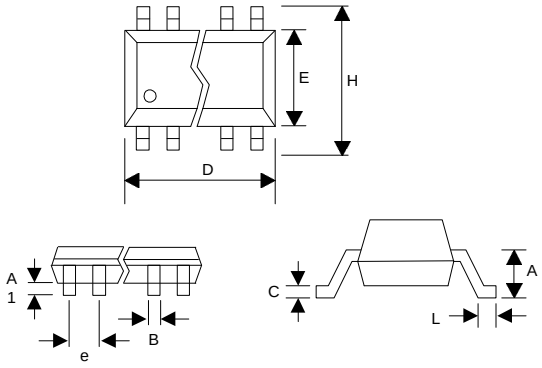
3. TIMING CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Rise Time	T_r	Measured at 0.8V ~ 2.0V @ 3.3V	0.8	0.95	1.1	ns
Fall Time	T_f	Measured at 2.0V ~ 0.8V @ 3.3V	0.78	0.85	0.9	ns
Propagation	T_{PROP}	V_T = 1.5 V	1	4	6	ns
Output Duty Cycle	D_T		45	50	55	%
Output-to-Output skew	T_{skew}	Rising edges at VDD/2			250	ps

PACKAGE INFORMATION

8 PIN Narrow SOIC (mm)

	SOIC	
Symbol	Min.	Max.
A	1.55	1.73
A1	0.15	0.18
B	0.35	0.49
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
H	5.84	6.20
L	0.41	0.89
e	1.27 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL103-04 S C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
S=SOIC