LH168R

384-output TFT-LCD Source Driver IC

DESCRIPTION

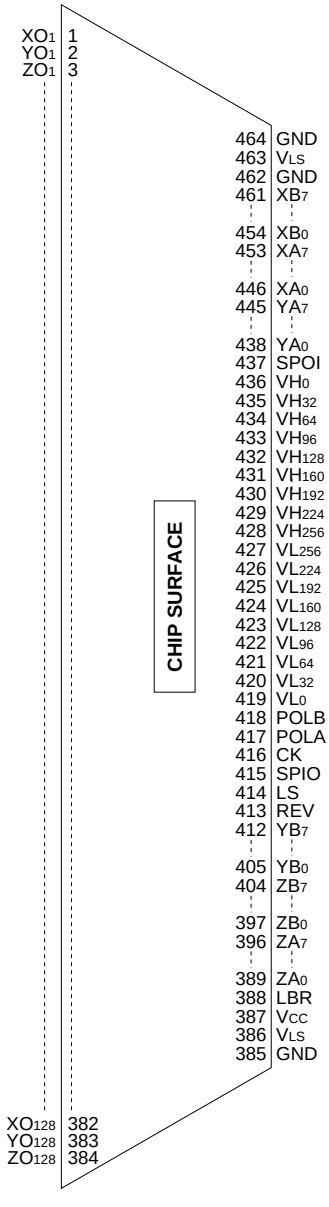
The LH168R is a 384-output TFT-LCD source driver IC which can simultaneously display 16.7 million colors in 256 gray scales.

FEATURES

- Number of LCD drive outputs : 384
- Built-in 8-bit digital input DAC
- Dot-inversion drive : Outputs the inverted gray scale voltages between LCD drive pins next to each other
- 2-port input for each circuit of data inputs R, G and B, and it is possible to sample and hold display data of two pixels at the same time
- Possible to display 16.7 million colors in 256 gray scales with reference voltage input of 18 gray scales : This reference voltage input corresponds to γ correction and intermediate reference voltage input can be abbreviated
- Cascade connection
- Sampling sequence :
  Output shift direction can be selected
  XO_1, YO_1, $ZO_1 \rightarrow XO_{128}$, YO_{128}, ZO_{128} or
  ZO_{128}, YO_{128}, $XO_{128} \rightarrow ZO_1$, YO_1, XO_1
- Shift clock frequency : 65 MHz (MAX.)
- Supply voltages
  – V_{CC} (for logic system) : +2.5 to +3.6 V
  – V_{LS} (for LCD drive) : +13 V (MAX.)
- Package : 464-pin TCP (Tape Carrier Package)

PIN CONNECTIONS

464-PIN TCP TOP VIEW

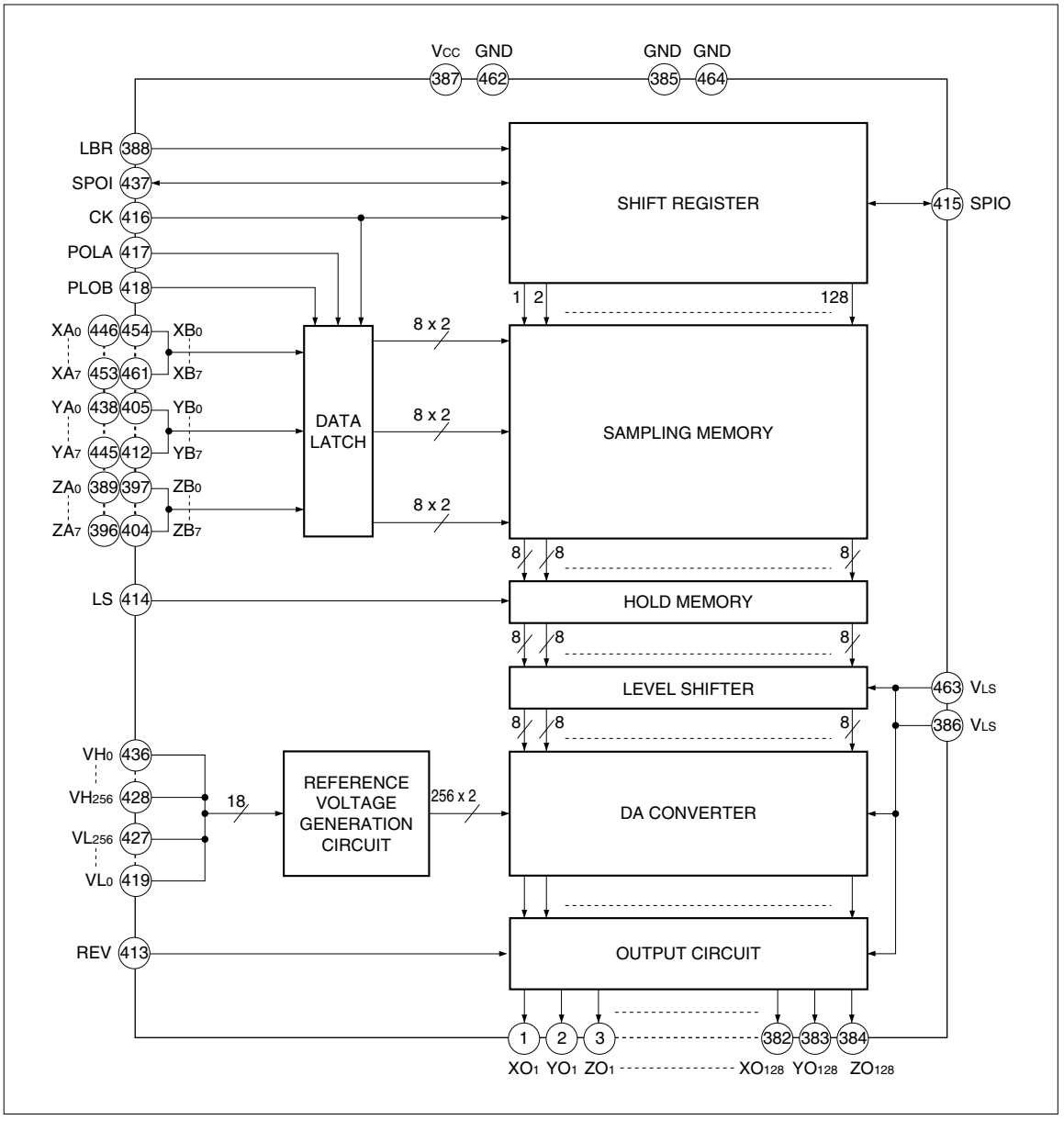


NOTE :
Doesn't prescribe TCP outline.

PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 384	XO_1-ZO_{128}	O	LCD drive output pins
385, 462, 464	GND	–	Ground pins
386	V_{LS}	–	Power supply pin for analog circuit
387	V_{CC}	–	Power supply pin for digital circuit
388	LBR	I	Shift direction selection input pin
389 to 396	ZA_0-ZA_7	I	Data input pins
397 to 404	ZB_0-ZB_7	I	Data input pins
405 to 412	YB_0-YB_7	I	Data input pins
413	REV	I	LCD drive output polarity exchange input pin
414	LS	I	Latch input pin
415	SPIO	I/O	Start pulse input/cascade output pin
416	CK	I	Shift clock input pin
417, 418	POLA, POLB	I	Input data polarity exchange input pins
419 to 427	VL_0-VL_{256}	I	Reference voltage input pins
428 to 436	VH_{256}-VH_0	I	Reference voltage input pins
437	SPOI	I/O	Start pulse input/cascade output pin
438 to 445	YA_0-YA_7	I	Data input pins
446 to 453	XA_0-XA_7	I	Data input pins
454 to 461	XB_0-XB_7	I	Data input pins
463	V_{LS}	–	Power supply pin for analog circuit

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Shift Register	Used as a bi-directional shift register which performs the shifting operation by CK and selects bits for data sampling.
Data Latch	Used to temporary latch the input data which is sent to the sampling memory.
Sampling Memory	Used to sample the data to be entered by time sharing.
Hold memory	Used for latch processing of data in the sampling memory by LS input.
Level Shifter	Used to shift the data in the hold memory to the power supply level of the analog circuit unit and sends the shifted data to DA converter.
Reference Voltage Generation Circuit	Used to generate a gamma-corrected 256 x 2-level voltage by the resistor dividing circuit.
DA Converter	Used to generate an analog signal according to the display data and sends the signal to the output circuit.
Output Circuit	Used as a voltage follower, configured with an operational amplifier and an output buffer, which outputs analog signals of 256 x 2 gray scales to LCD drive output pin.

INPUT/OUTPUT CIRCUITS

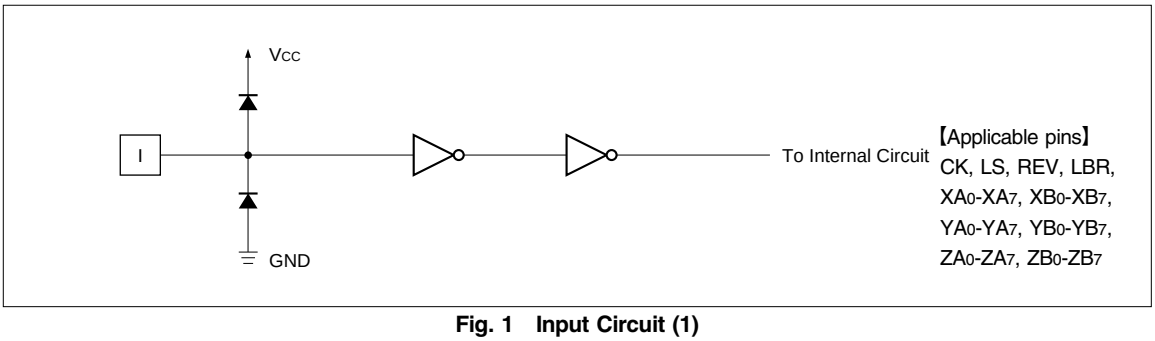


Fig. 1 Input Circuit (1)

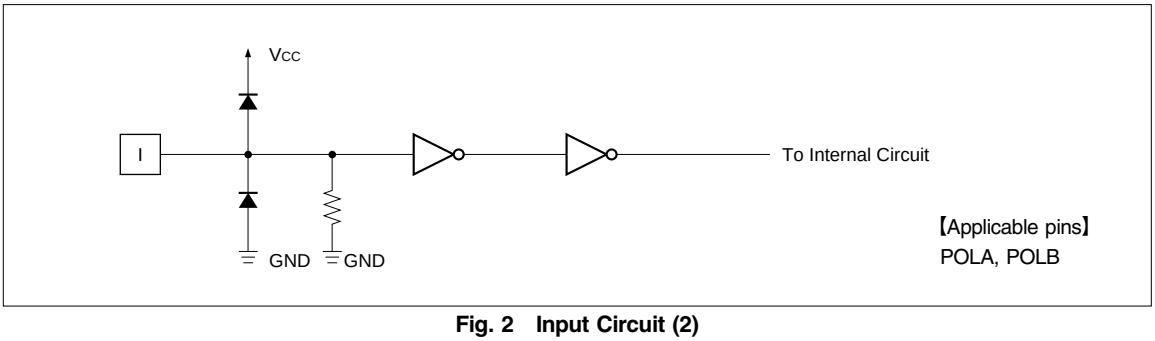


Fig. 2 Input Circuit (2)

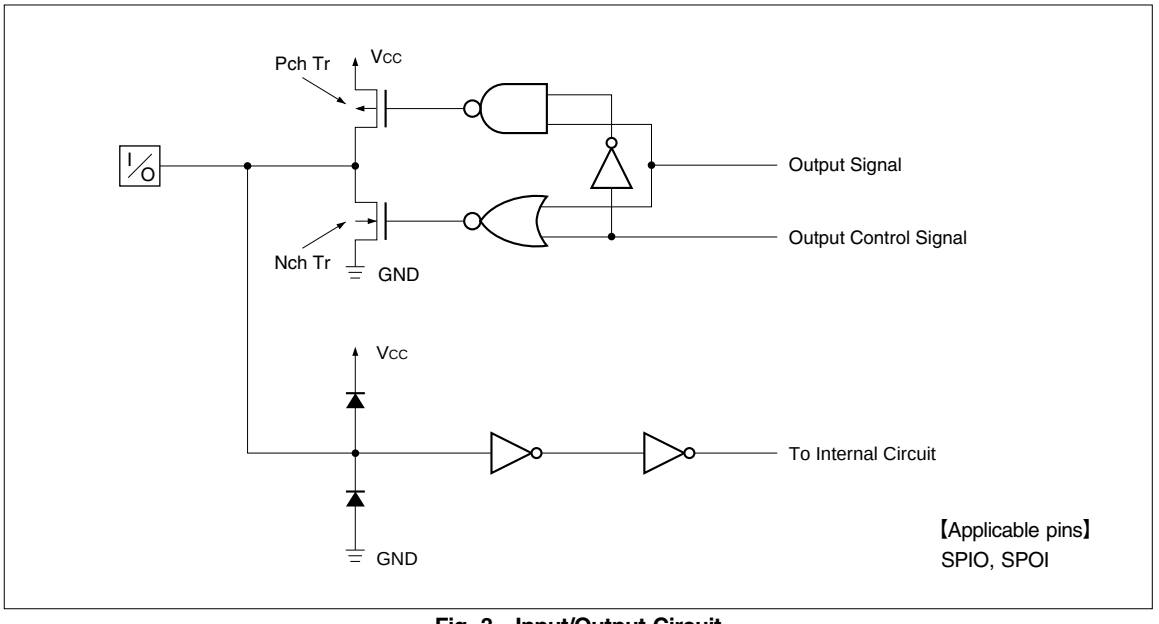


Fig. 3 Input/Output Circuit

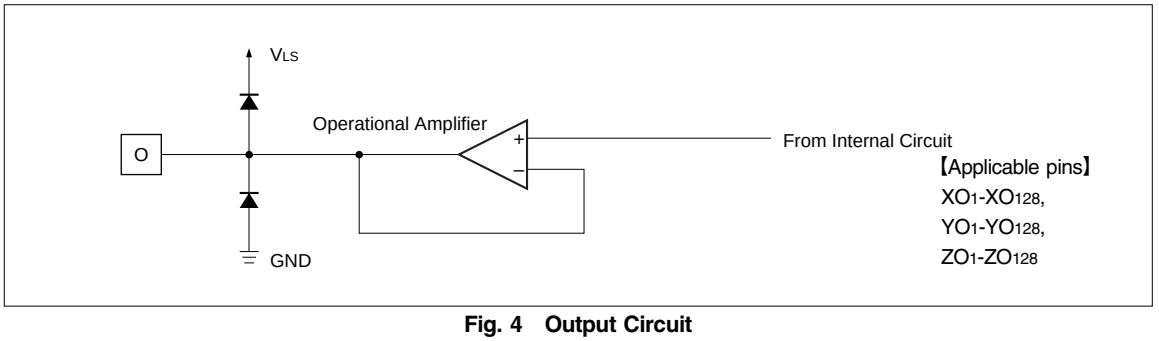


Fig. 4 Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTION
V_{CC}	Used as power supply pin for digital circuit, connected to +2.5 to +3.6 V.
V_{LS}	Used as power supply pin for analog circuit, connected to +8.0 to +13.0 V.
GND	Used as ground pin, connected to 0 V.
SPIO SPOI	Used as input pins of start pulse and also used as output pins for cascade connection. When "H" is input into start pulse input pin, data sampling is started. On completion of sampling, "H" pulse is output to output pin for cascade connection. Pin functions are selected by LBR. For selecting , refer to **"Functional Operations"**.
LBR	Used as input pin for selecting the shift register direction. For selecting, refer to **"Functional Operations"**.
LS	Used as input pin for parallel transfer from sampling memory to hold memory. Data is transferred at the rising edge and output from LCD drive output pin.
CK	Used as shift clock input pin. Data is latched into sampling memory from data input pin at the rising edge.
VH_0-VH_{256} VL_0-VL_{256}	Used as reference voltage input pins. Hold the reference voltage fixed during the period of LCD drive output. For relation between input data and output voltage values, refer to **"Output Voltage Value"**. For internal gamma correction, refer to **"Gamma Correction Value"**. Observe the following relation for input voltage. $V_{LS} > VH_0 \geq VH_{32} \geq \cdots \geq VH_{256} \geq VL_{256} \geq \cdots \geq VL_{32} \geq VL_0 >$ GND.
XA_0-XA_7, YA_0-YA_7 ZA_0-ZA_7, XB_0-XB_7 YB_0-YB_7, ZB_0-ZB_7	Used as data input pins of R, G, and B colors. 8-bit x 2-pixel data are input from data pins at the rising edge of CK. For relation between input data and output voltage values, refer to **"Functional Operations"** and **"Output Voltage Value"**. Select the data to be entered into X, Y, and Z according to picture element arrays of the panel.
XO_1-XO_{128} YO_1-YO_{128} ZO_1-ZO_{128}	Used as LCD drive output pins which output the voltage corresponding to the input of data input pins (XA_0 to XA_7, YA_0 to YA_7, ZA_0 to ZA_7, XB_0 to XB_7, YB_0 to YB_7, ZB_0 to ZB_7). Data of XO_1 to XO_{128} correspond to XA_0 to XA_7 and XB_0 to XB_7. Data of YO_1 to YO_{128} correspond to YA_0 to YA_7 and YB_0 to YB_7, and data of ZO_1 to ZO_{128} correspond to ZA_0 to ZA_7 and ZB_0 to ZB_7. For relation between input data and output voltage values, refer to **"Functional Operations"** and **"Output Voltage Value"**.
POLA POLB	Used as input pins for input data polarity exchange, POLA corresponds to XA_0 to XA_7, YA_0 to YA_7 and ZA_0 to ZA_7, and POLB corresponds to XB_0 to XB_7, YB_0 to YB_7 and ZB_0 to ZB_7. When "L" is entered, display data becomes normal mode. When "H" is entered, input data becomes polarity exchange mode. For relation between input data and output voltage values, refer to **"Output Voltage Value"**. These pins are pulled down at the inside.
REV	Used as polarity exchange pin of LCD drive output. Date is taken at the term when LS is "H" and the output polarity of the LCD drive output pin is determined. For exchanging, refer to **"Output Characteristics"**.

Functional Operations

The following describes the relation between data input pin and output direction.

Data input pin	XA_0-XA_7	YA_0-YA_7	ZA_0-ZA_7	XB_0-XB_7	YB0-YB_7	ZB_0-ZB_7	·····	XB_0-XB_7	YB_0-YB_7	ZB_0-ZB_7
Output direction	XO_1	YO_1	ZO_1	XO_2	YO_2	ZO_2	·····	XO_{128}	YO_{128}	ZO_{128}

The following describes the relation between LBR pin, SPOI pin, SPIO pin and output direction.

PIN	OUTPUT DIRECTION	
	RIGHT SHIFT (XO_1, YO_1, ZO_1→XO_{128}, YO_{128}, ZO_{128})	LEFT SHIFT (ZO_{128}, YO_{128}, XO_{128}→ZO_1, YO_1, XO_1)
LBR	H	L
SPOI	Input	Output
SPIO	Output	Input

NOTE :

Color data corresponding to X, Y, and Z vary depending on the output direction.

Output Characteristics

The following describes the relation between REV pin and output polarity of LCD drive pin.

REV	"H"	"L"
XO_1	+	–
YO_1	–	+
ZO_1	+	–
XO_2	–	+
YO_2	+	–
ZO_2	–	+
XO_3	+	–
YO_3	–	+
:	:	:
XO_{126}	–	+
YO_{126}	+	–
ZO_{126}	–	+
XO_{127}	+	–
YO_{127}	–	+
ZO_{127}	+	–
XO_{128}	–	+
YO_{128}	+	–
ZO_{128}	–	+

NOTES :

+ : The gray scale voltages corresponding to reference voltage VH_0 to VH_{256} are output.

– : The gray scale voltages corresponding to reference voltage VL_0 to VL_{256} are output.

Output Voltage Value

Two voltages are selected from all of the reference voltages (V_0-V_{256}) by the upper 3-bit data (D_7, D_6 and D_5) of the 8-bit input data (D_7, D_6, D_5, D_4, D_3, D_2, D_1 and D_0) taken by time sharing, and intermediate value is determined by the lower 5-bit data (D_4, D_3, D_2, D_1 and D_0).

The V_i is a reference voltage (VH_i or VL_i) that is determined by the polarity exchange input (REV). Relation between input data and output voltage values is shown below.

(i = 0, 32, 64, 96, 128, 160, 192, 224, 256)

INPUT DATA	OUTPUT VOLTAGE	
	POLA (POLB) = "L"	POLA (POLB) = "H"
0	V_0	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 6.61/8.96)/2.13$
1	$V_{32} + (V_0 - V_{32}) \times 31/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 5.74/8.96)/2.13$
2	$V_{32} + (V_0 - V_{32}) \times 30/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 4.87/8.96)/2.13$
3	$V_{32} + (V_0 - V_{32}) \times 29/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 4/8.96)/2.13$
4	$V_{32} + (V_0 - V_{32}) \times 28/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 3/8.96)/2.13$
5	$V_{32} + (V_0 - V_{32}) \times 27/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 2/8.96)/2.13$
6	$V_{32} + (V_0 - V_{32}) \times 26/32$	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 1/8.96)/2.13$
7	$V_{32} + (V_0 - V_{32}) \times 25/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 8/8)/2.13$
8	$V_{32} + (V_0 - V_{32}) \times 24/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 7/8)/2.13$
9	$V_{32} + (V_0 - V_{32}) \times 23/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 6/8)/2.13$
A	$V_{32} + (V_0 - V_{32}) \times 22/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 5/8)/2.13$
B	$V_{32} + (V_0 - V_{32}) \times 21/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 4/8)/2.13$
C	$V_{32} + (V_0 - V_{32}) \times 20/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 3/8)/2.13$
D	$V_{32} + (V_0 - V_{32}) \times 19/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 2/8)/2.13$
E	$V_{32} + (V_0 - V_{32}) \times 18/32$	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 1/8)/2.13$
F	$V_{32} + (V_0 - V_{32}) \times 17/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 8/8)/2.13$
10	$V_{32} + (V_0 - V_{32}) \times 16/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 7/8)/2.13$
11	$V_{32} + (V_0 - V_{32}) \times 15/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 6/8)/2.13$
12	$V_{32} + (V_0 - V_{32}) \times 14/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 5/8)/2.13$
13	$V_{32} + (V_0 - V_{32}) \times 13/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 4/8)/2.13$
14	$V_{32} + (V_0 - V_{32}) \times 12/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 3/8)/2.13$
15	$V_{32} + (V_0 - V_{32}) \times 11/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 2/8)/2.13$
16	$V_{32} + (V_0 - V_{32}) \times 10/32$	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 1/8)/2.13$
17	$V_{32} + (V_0 - V_{32}) \times 9/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 8/8)/2.13$
18	$V_{32} + (V_0 - V_{32}) \times 8/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 7/8)/2.13$
19	$V_{32} + (V_0 - V_{32}) \times 7/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 6/8)/2.13$
1A	$V_{32} + (V_0 - V_{32}) \times 6/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 5/8)/2.13$
1B	$V_{32} + (V_0 - V_{32}) \times 5/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 4/8)/2.13$
1C	$V_{32} + (V_0 - V_{32}) \times 4/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 3/8)/2.13$
1D	$V_{32} + (V_0 - V_{32}) \times 3/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 2/8)/2.13$
1E	$V_{32} + (V_0 - V_{32}) \times 2/32$	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 1/8)/2.13$
1F	$V_{32} + (V_0 - V_{32}) \times 1/32$	V_{224}

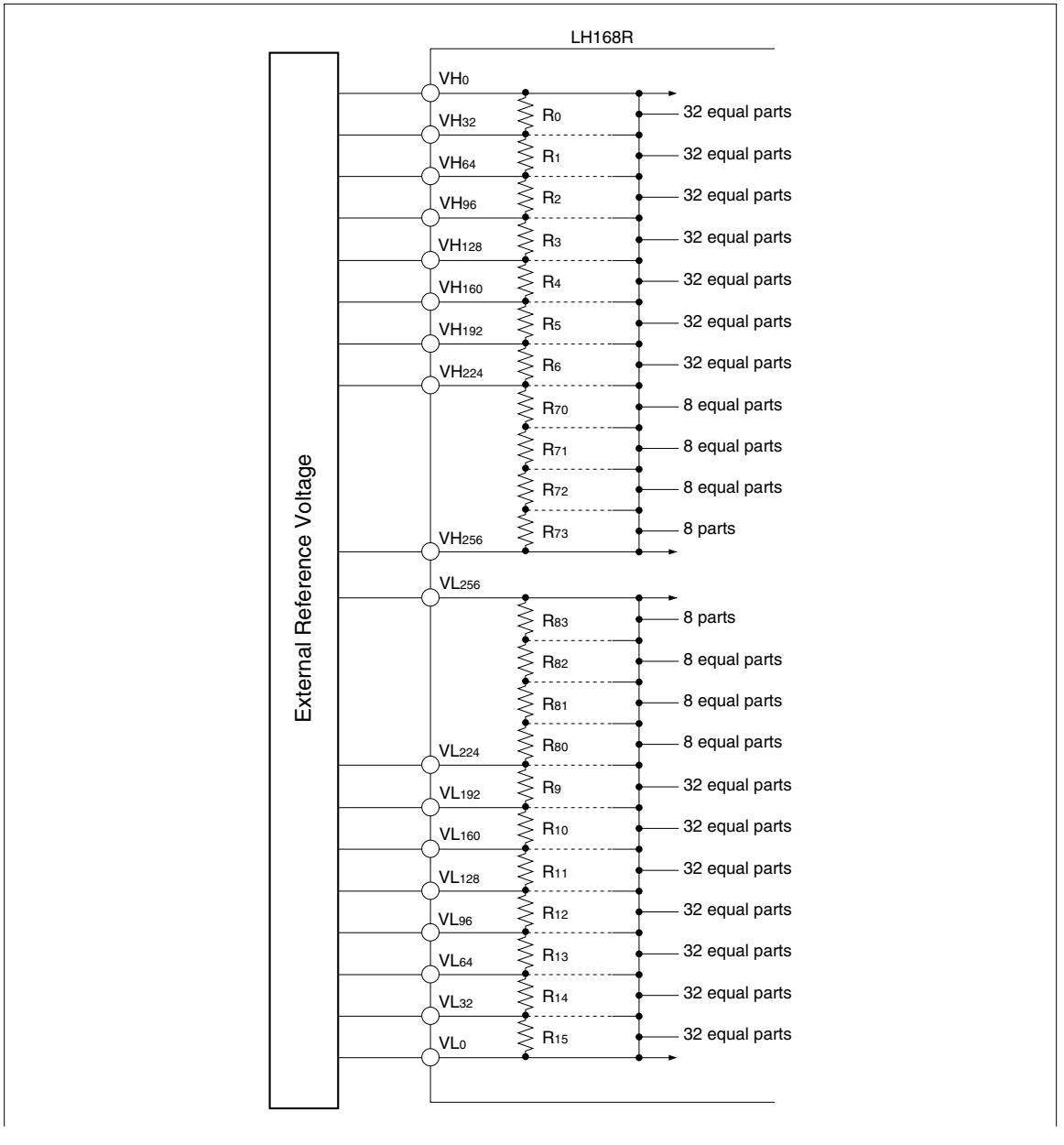
INPUT DATA	OUTPUT VOLTAGE	
	POLA (POLB) = "L"	POLA (POLB) = "H"
20	V_{32}	$V_{224} + (V_{192} - V_{224}) \times 1/32$
21	$V_{64} + (V_{32} - V_{64}) \times 31/32$	$V_{224} + (V_{192} - V_{224}) \times 2/32$
22	$V_{64} + (V_{32} - V_{64}) \times 30/32$	$V_{224} + (V_{192} - V_{224}) \times 3/32$
:	:	:
3D	$V_{64} + (V_{32} - V_{64}) \times 3/32$	$V_{224} + (V_{192} - V_{224}) \times 30/32$
3E	$V_{64} + (V_{32} - V_{64}) \times 2/32$	$V_{224} + (V_{192} - V_{224}) \times 31/32$
3F	$V_{64} + (V_{32} - V_{64}) \times 1/32$	V_{192}
40	V_{64}	$V_{192} + (V_{160} - V_{192}) \times 1/32$
41	$V_{96} + (V_{64} - V_{96}) \times 31/32$	$V_{192} + (V_{160} - V_{192}) \times 2/32$
42	$V_{96} + (V_{64} - V_{96}) \times 30/32$	$V_{192} + (V_{160} - V_{192}) \times 3/32$
:	:	:
5D	$V_{96} + (V_{64} - V_{96}) \times 3/32$	$V_{192} + (V_{160} - V_{192}) \times 30/32$
5E	$V_{96} + (V_{64} - V_{96}) \times 2/32$	$V_{192} + (V_{160} - V_{192}) \times 31/32$
5F	$V_{96} + (V_{64} - V_{96}) \times 1/32$	V_{160}
60	V_{96}	$V_{160} + (V_{128} - V_{160}) \times 1/32$
61	$V_{128} + (V_{96} - V_{128}) \times 31/32$	$V_{160} + (V_{128} - V_{160}) \times 2/32$
62	$V_{128} + (V_{96} - V_{128}) \times 30/32$	$V_{160} + (V_{128} - V_{160}) \times 3/32$
:	:	:
7D	$V_{128} + (V_{96} - V_{128}) \times 3/32$	$V_{160} + (V_{128} - V_{160}) \times 30/32$
7E	$V_{128} + (V_{96} - V_{128}) \times 2/32$	$V_{160} + (V_{128} - V_{160}) \times 31/32$
7F	$V_{128} + (V_{96} - V_{128}) \times 1/32$	V_{128}
80	V_{128}	$V_{128} + (V_{96} - V_{128}) \times 1/32$
81	$V_{160} + (V_{128} - V_{160}) \times 31/32$	$V_{128} + (V_{96} - V_{128}) \times 2/32$
82	$V_{160} + (V_{128} - V_{160}) \times 30/32$	$V_{128} + (V_{96} - V_{128}) \times 3/32$
:	:	:
9D	$V_{160} + (V_{128} - V_{160}) \times 3/32$	$V_{128} + (V_{96} - V_{128}) \times 30/32$
9E	$V_{160} + (V_{128} - V_{160}) \times 2/32$	$V_{128} + (V_{96} - V_{128}) \times 31/32$
9F	$V_{160} + (V_{128} - V_{160}) \times 1/32$	V_{96}
A0	V_{160}	$V_{96} + (V_{64} - V_{96}) \times 1/32$
A1	$V_{192} + (V_{160} - V_{192}) \times 31/32$	$V_{96} + (V_{64} - V_{96}) \times 2/32$
A2	$V_{192} + (V_{160} - V_{192}) \times 30/32$	$V_{96} + (V_{64} - V_{96}) \times 3/32$
:	:	:
BD	$V_{192} + (V_{160} - V_{192}) \times 3/32$	$V_{96} + (V_{64} - V_{96}) \times 30/32$
BE	$V_{192} + (V_{160} - V_{192}) \times 2/32$	$V_{96} + (V_{64} - V_{96}) \times 31/32$
BF	$V_{192} + (V_{160} - V_{192}) \times 1/32$	V_{64}
C0	V_{192}	$V_{64} + (V_{32} - V_{64}) \times 1/32$
C1	$V_{224} + (V_{192} - V_{224}) \times 31/32$	$V_{64} + (V_{32} - V_{64}) \times 2/32$
C2	$V_{224} + (V_{192} - V_{224}) \times 30/32$	$V_{64} + (V_{32} - V_{64}) \times 3/32$
:	:	:
DD	$V_{224} + (V_{192} - V_{224}) \times 3/32$	$V_{64} + (V_{32} - V_{64}) \times 30/32$
DE	$V_{224} + (V_{192} - V_{224}) \times 2/32$	$V_{64} + (V_{32} - V_{64}) \times 31/32$
DF	$V_{224} + (V_{192} - V_{224}) \times 1/32$	V_{32}

INPUT DATA	OUTPUT VOLTAGE	
	POLA (POLB) = "L"	POLA (POLB) = "H"
E0	V_{224}	$V_{32} + (V_0 - V_{32}) \times 1/32$
E1	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 1/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 2/32$
E2	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 2/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 3/32$
E3	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 3/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 4/32$
E4	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 4/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 5/32$
E5	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 5/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 6/32$
E6	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 6/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 7/32$
E7	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 7/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 8/32$
E8	$V_{256} + (V_{224} - V_{256}) \times (2.13 - 0.33 \times 8/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 9/32$
E9	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 1/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 10/32$
EA	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 2/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 11/32$
EB	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 3/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 12/32$
EC	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 4/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 13/32$
ED	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 5/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 14/32$
EE	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 6/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 15/32$
EF	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 7/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 16/32$
F0	$V_{256} + (V_{224} - V_{256}) \times (1.8 - 0.36 \times 8/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 17/32$
F1	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 1/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 18/32$
F2	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 2/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 19/32$
F3	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 3/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 20/32$
F4	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 4/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 21/32$
F5	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 5/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 22/32$
F6	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 6/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 23/32$
F7	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 7/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 24/32$
F8	$V_{256} + (V_{224} - V_{256}) \times (1.44 - 0.45 \times 8/8)/2.13$	$V_{32} + (V_0 - V_{32}) \times 25/32$
F9	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 1/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 26/32$
FA	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 2/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 27/32$
FB	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 3/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 28/32$
FC	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 4/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 29/32$
FD	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 4.87/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 30/32$
FE	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 5.74/8.96)/2.13$	$V_{32} + (V_0 - V_{32}) \times 31/32$
FF	$V_{256} + (V_{224} - V_{256}) \times (0.99 - 0.99 \times 6.61/8.96)/2.13$	V_0

γ (Gamma) Correction Value

Between reference voltage input pins VH_0 and VH_{256}, 256 resistors are connected in series. And between reference voltage input pins VL_0 and VL_{256}, 256 resistors are connected in series. No resistor is connected between reference voltage input pins VH_{256} and VL_{256}.

The γ correction curve is a broken line connected between intermediate voltage inputs (VH_{32}, VH_{64}, VH_{96}, VH_{128}, VH_{160}, VH_{192}, VH_{224}, VL_{32}, VL_{64}, VL_{96}, VL_{128}, VL_{160}, VL_{192} and VL_{224}). Each γ correction value between the intermediate voltage inputs is divided into 32 parts by resistor.



The following shows the ratio of γ correction resistance, when R_0 equals 1.

R_0	1.00	R_{83}	0.99
R_1	0.60	R_{82}	0.45
R_2	0.49	R_{81}	0.36
R_3	0.52	R_{80}	0.33
R_4	0.60	R_9	1.00
R_5	0.74	R_{10}	0.74
R_6	1.00	R_{11}	0.60
R_{70}	0.33	R_{12}	0.52
R_{71}	0.36	R_{13}	0.49
R_{72}	0.45	R_{14}	0.60
R_{73}	0.99	R_{15}	1.00

The following shows the ratio of γ correction resistance of R_{73} and R_{83}, when R_{730} equals 1.

R_{73}	R_{730}	1.00	R_{83}	R_{837} (VL_{256} side)	2.35
	R_{731}	1.00		R_{836}	0.87
	R_{732}	1.00		R_{835}	0.87
	R_{733}	1.00		R_{834}	0.87
	R_{734}	0.87		R_{833}	1.00
	R_{735}	0.87		R_{832}	1.00
	R_{736}	0.87		R_{831}	1.00
	R_{737} (VH_{256} side)	2.35		R_{830}	1.00

PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has some power supply pins, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

V_{CC} → logic input → V_{LS}, VH_0-VH_{256}, VL_0-VL_{256}

When disconnecting the power supply, follow the reverse sequence.

Reference voltage input

The relation of the reference voltage input is shown here.

$V_{LS} > VH_0 \geq VH_{32} \geq \cdots \geq VH_{224} \geq VH_{256} \geq 0.5V_{LS} \geq VL_{256} \geq VL_{224} \geq \cdots \geq VL_{32} \geq VL_0 >$ GND

Maximum ratings

When connecting or disconnecting the power supply, this IC must be used within the range of the absolute maximum ratings.

Target output load

This IC is designed for a 200 pF output load capacity. When using this IC for other than 200 pF panels, confirm the device is having no problem before using it.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage	V_{CC}	V_{CC}	−0.3 to +6.0	V	1, 2
	V_{LS}	V_{LS}	−0.3 to +14.0	V	
Input voltage	V_I	V_{H0}-V_{L0}	−0.3 to V_{LS} + 0.3	V	
	V_I	SPIO, SPOI, CK, LS, REV, LBR, POLA, POLB, XA_0-XA_7, XB_0-XB_7, YA_0-YA_7, YB_0-YB_7, ZA_0-ZA_7, ZB_0-ZB_7	−0.3 to V_{CC} + 0.3	V	
Output voltage	V_O	SPIO, SPOI	−0.3 to V_{CC} + 0.3	V	
	V_O	XO_1-ZO_{128}	−0.3 to V_{LS} + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	˚C	

NOTES :

1. T_A = +25 ˚C
2. The maximum applicable voltage on any pin with respect to GND (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	+2.5		+3.6	V	1
	V_{LS}	+8.0		+13.0	V	
Reference voltage input	V_{H0}-V_{H256}	0.5V_{CC}		V_{LS} − 0.2	V	
	V_{L0}-V_{L256}	+0.2		0.5V_{CC}	V	
Clock frequency	f_{CK}			65	MHz	
LCD drive output load capacity	C_L			200	pF	
Operating temperature	T_{OPR}	−20		+75	˚C	

NOTE :

1. The applicable voltage on any pin with respect to GND (0 V).

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = +2.5 to +3.6 V, V_{LS} = +8.0 to +13.0 V, T_{OPR} = −20 to +75 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT.	NOTE
Input "Low" voltage	V_{IL}		XA_0-XA_7, YA_0-YA_7, ZA_0-ZA_7, XB_0-XB_7, YB_0-YB_7, ZB_0-ZB_7, SPIO, SPOI, CK, LS, LBR, REV, POLA, POLB	GND		0.3V_{CC}	V	
Input "High" voltage	V_{IH}			0.7V_{CC}		V_{CC}	V	
Output "Low" voltage	V_{OL}	I_{OL} = 0.3 mA	SPIO, SPOI	GND		GND + 0.4	V	
Output "H" voltage	V_{OH}	I_{OH} = −0.3 mA		V_{CC} − 0.4		V_{CC}	V	
Input "Low" current	I_{ILL1}		XA_0-XA_7, YA_0-YA_7, ZA_0-ZA_7, XB_0-XB_7, YB_0-YB_7, ZB_0-ZB_7, SPIO, SPOI, CK, LS, LBR, REV, POLA, POLB			10	µA	
Input "High" current	I_{ILH1}		XA_0-XA_7, YA_0-YA_7, ZA_0-ZA_7, XB_0-XB_7, YB_0-YB_7, ZB_0-ZB_7, SPIO, SPOI, CK, LS, LBR, REV			10	µA	
	I_{ILH2}		POLA, POLB			400	µA	
Supply current (In operation mode)	I_{CC1}	f_{CK} = 65 MHz f_{LS} = 50 kHz (Data sampling state)	V_{CC}-GND			14	mA	
Supply current (In standby mode)	I_{CC2}	f_{CK} = 65 MHz f_{LS} = 50 kHz SPI = GND is fixed. (Standby state)	V_{CC}-GND			1.5	mA	
Supply current (In operation mode)	I_{LS1}	f_{CK} = 65 MHz f_{LS} = 50 kHz (Data sampling state)	V_{LS}-GND			5	mA	
Supply current (In standby mode)	I_{LS2}	f_{CK} = 65 MHz f_{LS} = 50 kHz SPI = GND is fixed. (Standby state)	V_{LS}-GND			4	mA	
Output voltage range	V_{OUT}		XO_1-ZO_{128}	GND + 0.2		V_{LS} − 0.2	V	1
Deviations between output voltage pins	V_{OD}			−10		+10	mV	
Output current	I_{O1}-I_{O4}				200		µA	2
Resistance between reference voltage input pins	R_{GMAH}		VH_0-VH_{256}		20		kΩ	
	R_{GMAL}		VL_0-VL_{256}		20		kΩ	

NOTES :

1. Criterion of evaluating voltage deviations.
   (a) Between output voltage pins
   Measuring values : Output voltage value at the time after 10 µs at the rising edge of LS. (Average of several times)
   (Conditions) Output load capacity is 200 pF.
   In a state when the reference voltage is fixed.
   Expecting values : Calculated following these specifications.
   (Conditions) In a state when the reference voltage is fixed.
   (b) Between LCD drivers
   Measuring values : Applicable to (a).
   (Conditions) Applicable to (a).
   Expecting values : Applicable to (a).
   (Conditions) Applicable to (a).
   Each input voltage between the LCD drivers must be made perfectly equal by connecting corresponding reference voltage input pins.

2. I_{O1} : Applied voltage = 8.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 7.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 10.0 V
   I_{O2} : Applied voltage = 7.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 7.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 10.0 V
   I_{O3} : Applied voltage = 3.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 2.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 10.0 V
   I_{O4} : Applied voltage = 2.0 V for output pins XO_1 to ZO_{128}.
   Output voltage = 2.5 V for output pins XO_1 to ZO_{128}.
   V_{LS} = 10.0 V

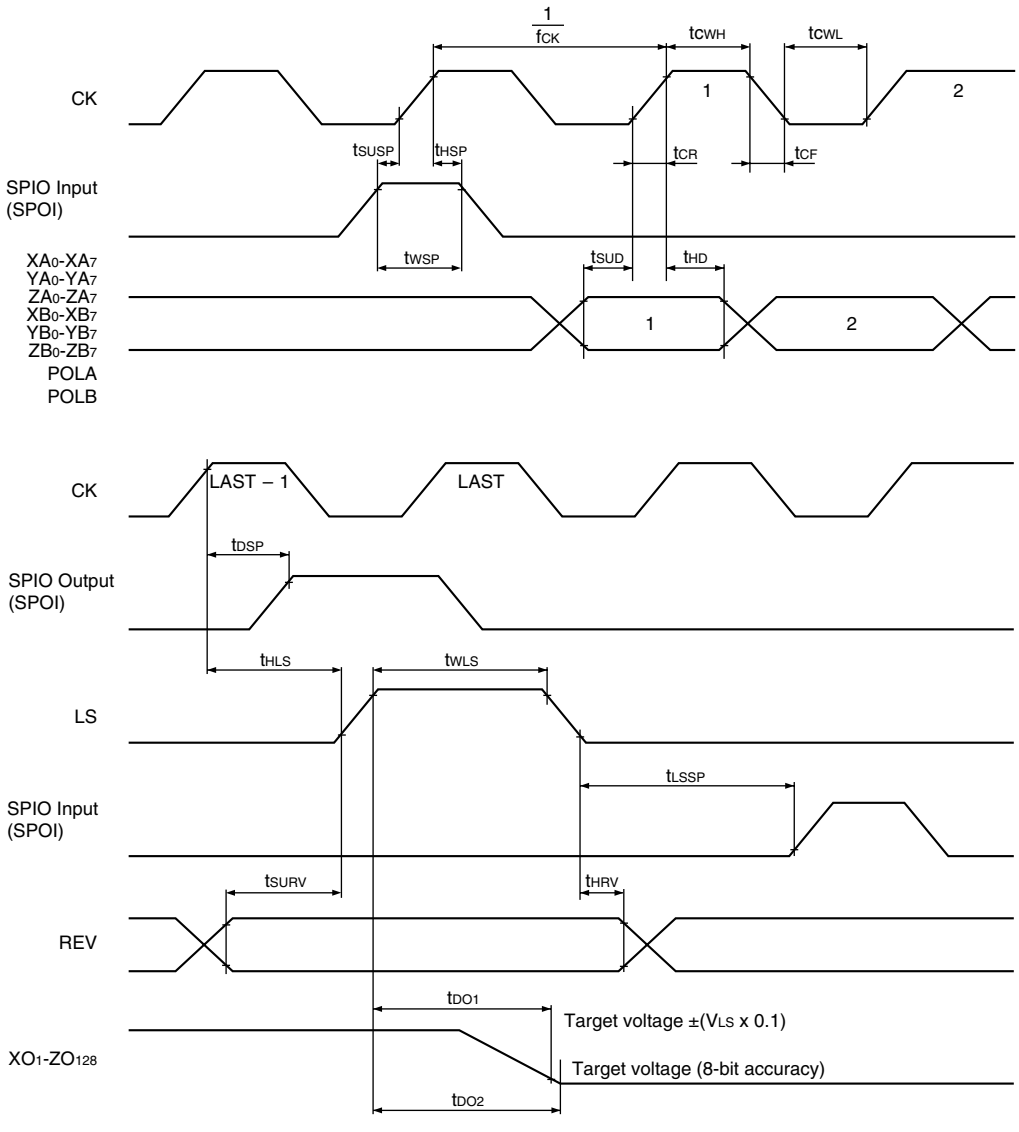
AC Characteristics (V_{CC} = +2.5 to +2.7 V, V_{LS} = +8.0 to +13.0 V, T_{OPR} = –20 to +75 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f_{CK}		CK			40	MHz
"H" level pulse width	t_{CWH}			8			ns
"L" level pulse width	t_{CWL}			8			ns
Input rise time	t_{CR}					10	ns
Input fall time	t_{CF}					10	ns
Data setup time	t_{SUD}		XA_0-XA_7, YA_0-YA_7, ZA_0-ZA_7, XB_0-XB_7, YB_0-YB_7, ZB_0-ZB_7, POLA, POLB	6			ns
Data hold time	t_{HD}			6			ns
Start pulse setup time	t_{SUSP}		SPIO, SPOI	6			ns
Start pulse hold time	t_{HSP}			6			ns
Start pulse width	t_{WSP}					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t_{DSP}	C_L = 15 pF				19	ns
LCD drive output delay time 1	t_{DO1}	C_L = 200 pF	XO_1-ZO_{128}			3	µs
LCD drive output delay time 2	t_{DO2}	C_L = 200 pF				10	µs
LS signal-SPI signal setup time	t_{LSSP}		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t_{HLS}			7			ns
LS signal "H" level width	t_{WLS}			$\frac{1}{f_{CK}}$			ns
REV signal-LS signal setup time	t_{SURV}		REV	14			ns
REV signal-LS signal hold time	t_{HRV}			10			ns

(V_{CC} = +2.7 to +3.6 V, V_{LS} = +8.0 to +13.0 V, T_{OPR} = –20 to +75 ˚C)

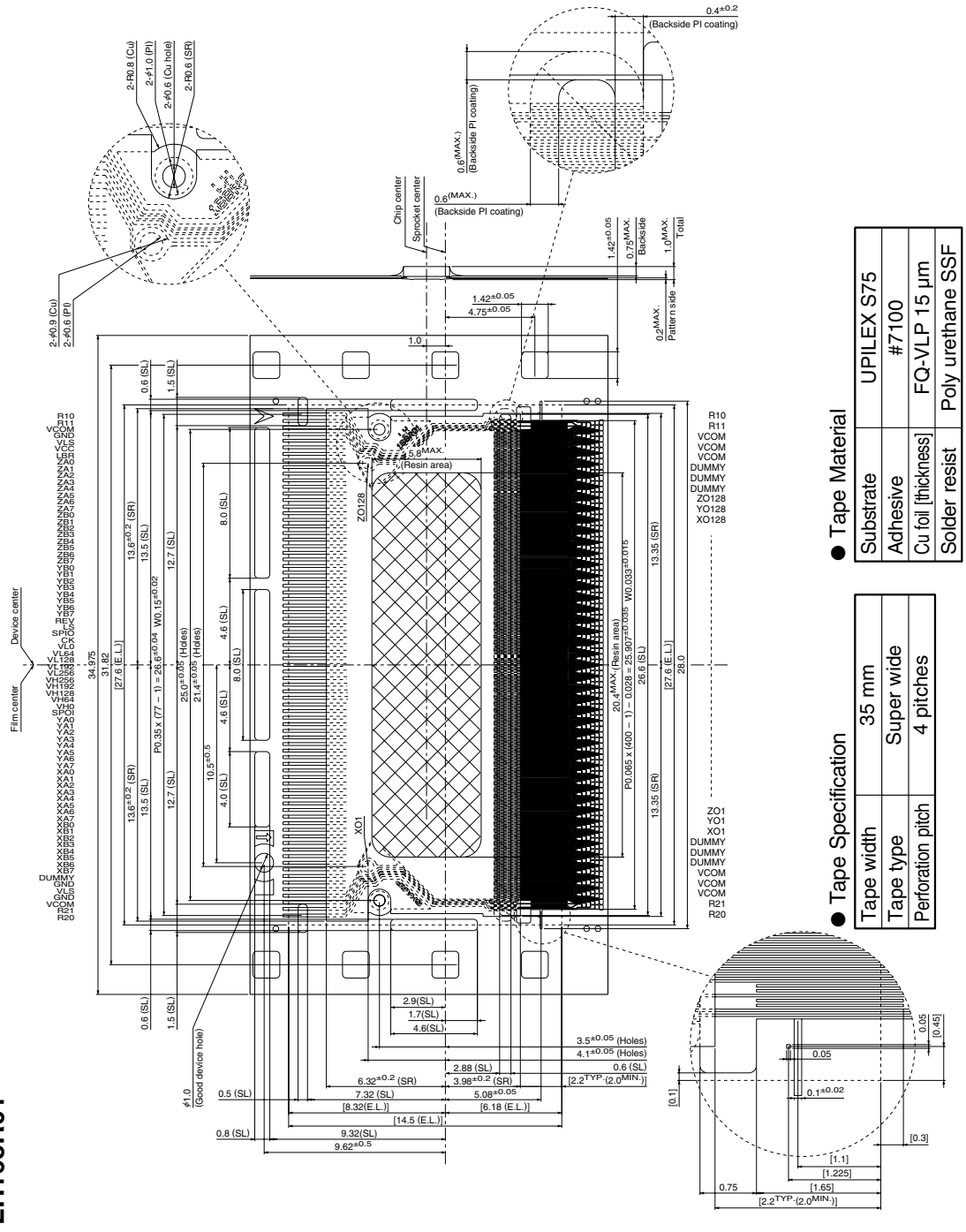
PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT
Clock frequency	f_{CK}		CK			65	MHz
"H" level pulse width	t_{CWH}			4			ns
"L" level pulse width	t_{CWL}			4			ns
Input rise time	t_{CR}					10	ns
Input fall time	t_{CF}					10	ns
Data setup time	t_{SUD}		XA_0-XA_7, YA_0-YA_7, ZA_0-ZA_7, XB_0-XB_7, YB_0-YB_7, ZB_0-ZB_7, POLA, POLB	4			ns
Data hold time	t_{HD}			1			ns
Start pulse setup time	t_{SUSP}		SPIO, SPOI	3			ns
Start pulse hold time	t_{HSP}			2			ns
Start pulse width	t_{WSP}					$\frac{1}{f_{CK}}$	ns
Start pulse output delay time	t_{DSP}	C_L = 15 pF				11	ns
LCD drive output delay time 1	t_{DO1}	C_L = 200 pF	XO_1-ZO_{128}			3	µs
LCD drive output delay time 2	t_{DO2}	C_L = 200 pF				10	µs
LS signal-SPI signal setup time	t_{LSSP}		LS	$\frac{1}{f_{CK}}$			ns
LS signal-CK signal hold time	t_{HLS}			7			ns
LS signal "H" level width	t_{WLS}			$\frac{1}{f_{CK}}$			ns
REV signal-LS signal setup time	t_{SURV}		REV	14			ns
REV signal-LS signal hold time	t_{HRV}			10			ns

Timing Chart



PACKAGE

(Unit : mm)



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