SHARP

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To :

SPECIFICATIONS

Product Type 5 V Drive 240 Outputs TFT-LCD Source Driver

Model No. LH1684F

※This specifications contains 34 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

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ENGINEERING DEPARTMENT I
LOGIC IC ENGINEERING CENTER
TENRI INTEGRATED CIRCUITS (IC) GROUP
SHARP CORPORATION

○When using the products covered herein , please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2) , even for the following application areas , be sure to observe the precautions given in Paragraph (2) . Never use the products for the equipment listed in Paragraph (3) .

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability , should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation , redundancy , and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes , trains , automobiles , and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment , etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality , reliability , or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support , etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

○Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

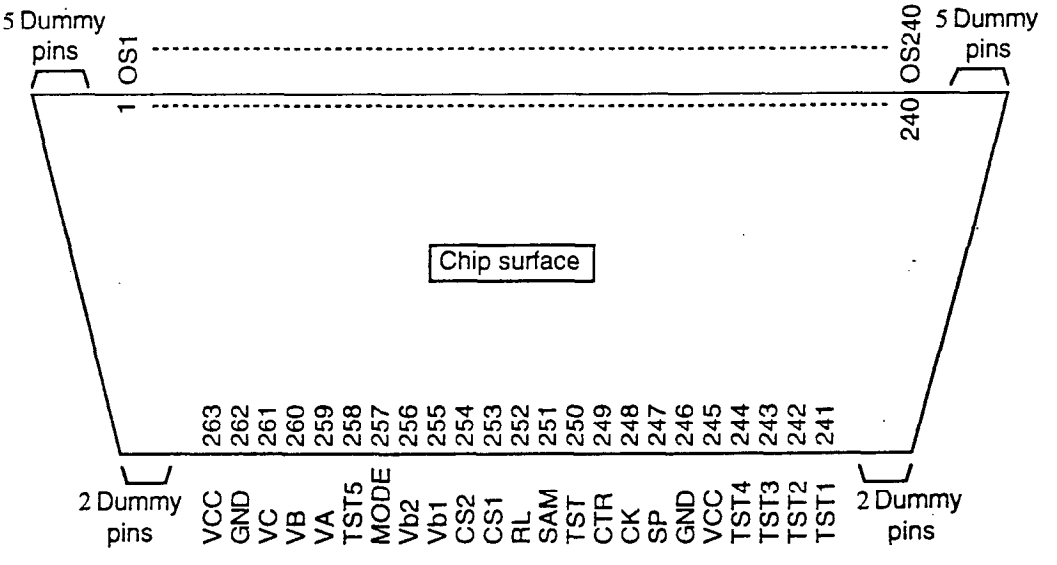
1. Summary

The LH1684F is a source driver for the TFT liquid crystal panel used for LCD unit such as a TV set and has 240 LCD drive outputs.
The LH1684F samples and holds three video signals of R, G, and B by the sample and hold circuits at the synchronized with the clock CK , and output simultaneously the output voltage from all output pins.

2. Features

- No. of LCD drive outputs : 240 outputs
- Supply voltage : 4.5 to 5.5 V
- Output amplitude voltage : 4.0 V_{P-P} (at 5.0 V supply voltage)
- Sampling frequency : 20 MHz (MAX)
- Video signals sampling : Shift direction can be selected. (OS1 → OS240 or OS240 → OS1)
- Sampling timing : Normal sampling operation and 3-point simultaneous sampling operation can be selected.
- Video signal setting : Compatible to stripe pixel array panels and delta pixel array panels by mode setting circuit.
- Cascade connection : Max. 4 cascades (Internal counting system)
- Package : 263 pins TCP (Tape Carrier Package)
- Process configuration : C-MOS silicon gate (p-type silicon substrate)
- Not designed or rated as radiation hardened.

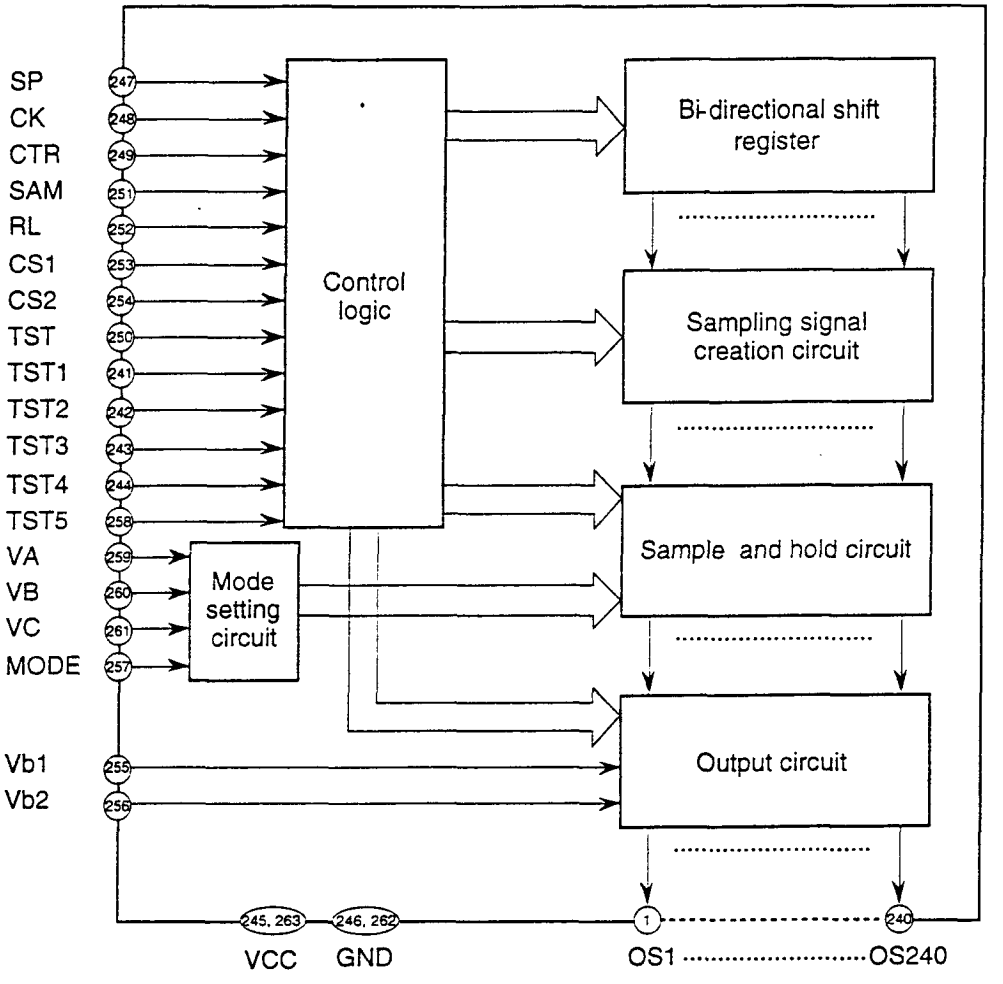
3. Pin Configuration (Does not prescribe TCP outline)



Notes: 1. This TCP has 14 dummy pins which are not electrically connected.
2. The above pin configuration shows the pins as seen from the TCP surface.

4. Block Diagram

Numerals in circles indicate the pin number.



Block name	Block function
Control logic	Used to create signals necessary for controlling cascade sequence and for discharge signal and sampling signals creation circuits, etc.
Bi-directional shift register	Used as transfer circuit of video sampling start signals. It is possible to set the direction of sampling start signals sequence by setting the R/L pin, from OS1 to OS240 or from OS240 to OS1.
Sampling signal creation circuit	Used to create the sampling signals corresponding to each output pin based on the sampling start signals transferred by the bi-directional shift register.
Mode setting circuit	Used to set the form of the video signals to be sent to the sample and hold circuits.
Sample and hold circuit	Used to sample the video signals input from the mode setting circuit at the timing of the sampling signals and hold the sampling datas until the next sampling operation.
Output circuit	The circuit comprises an operational amplifier and an output buffer and outputs the voltage corresponding to the data held in the sample and hold circuit.

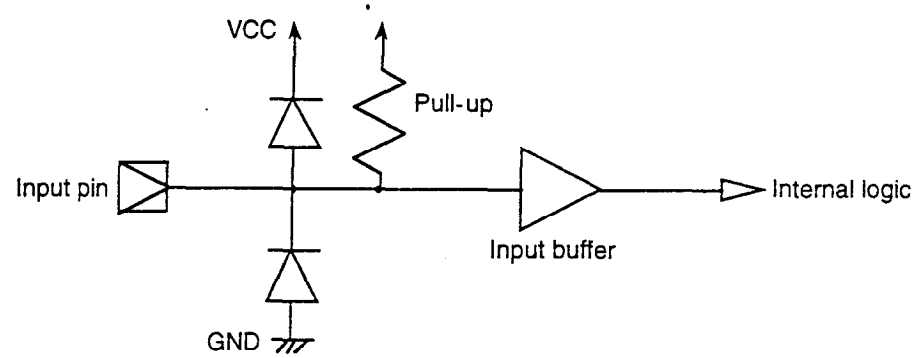
5. Description of Pins

5.1 Designation of pins

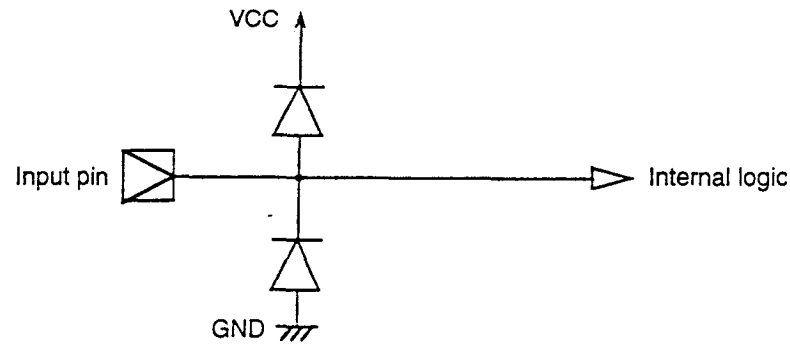
Pin No.	Pin symbol	I/O	Designation	Remarks
1 to 240	OS1 to OS240	O	LCD drive output pins	
241	TST1	I	LSI test pin	
242	TST2	I	LSI test pin	
243	TST3	I	LSI test pin	
244	TST4	I	LSI test pin	
245, 263	VCC	—	Power supply pins	
246, 262	GND	—	GND pins	
247	SP	I	Horizontal scanning start pulse input pin	
248	CK	I	Horizontal shift clock input pin	
249	CTR	I	Analog circuit operation selecting pin	
250	TST	I	LSI test pin	
251	SAM	I	Sampling mode selecting pin	
252	RL	I	Sampling sequence selecting pin	
253	CS1	I	Cascade sequence setting pin 1	
254	CS2	I	Cascade sequence setting pin 2	
255	Vb1	I	Bias voltage setting pin for output operational amplifiers	
256	Vb2	I	Bias voltage setting pin for output buffers	
257	MODE	I	Video signals form setting pin	
258	TST5	I	LSI test pin	
259	VA	I	Video signal input pin	
260	VB	I	Video signal input pin	
261	VC	I	Video signal input pin	

5.2 Input/output circuit types

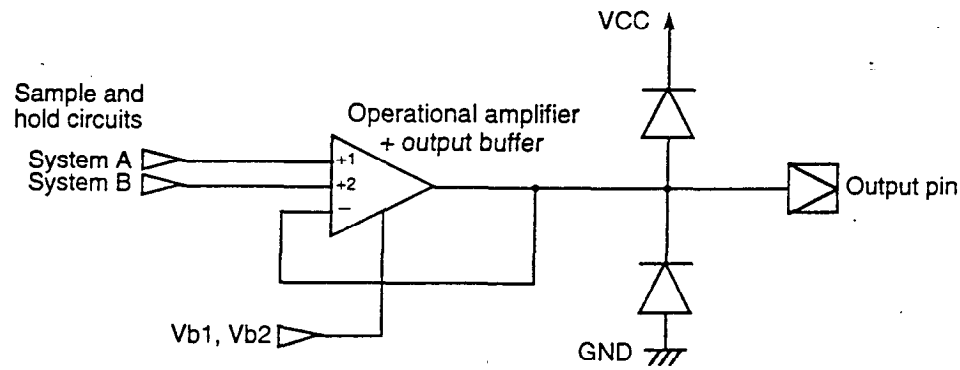
(1) Input pin 1 (SP, CK, CTR, RL, SAM, CS1, CS2, MODE, TST, TST1, TST2, TST3, TST4, and TST5 pins)
Note that SP, CK, CTR, and MODE pins do not have pull-up functions.
The TST5 pin has the pull-down function.



(2) Input pin 2 (VA, VB, VC, Vb1, and Vb2 pins)



(3) Output pin (OS1 to OS240 pins)



6. Description of Functions and Operations

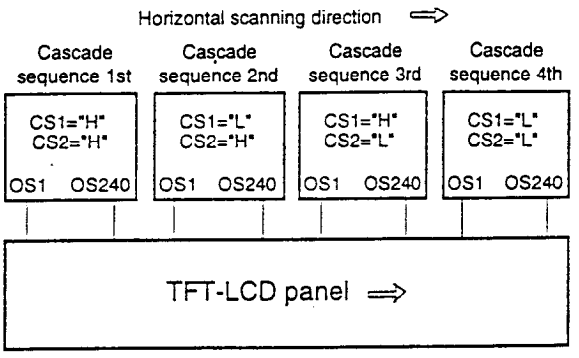
6.1 Functions of pin

Pin symbol	Pin functions
VCC	Used as power supply pin, which is normally connected to +5.0 V.
GND	Used as GND pin, which is connected to 0V.
TST	Used as pin for LSI testing. Must be connected to VCC.
TST1 to TST4	Used as pins for LSI testing. Must be connected to VCC.
TST5	Used as pin for LSI testing. Must be connected to GND.
SP	Used as input pin of horizontal scanning start pulse.
CK	Used as input pin of horizontal shift clock. Video signals are sampled in order at rise timing and fall timing of CK.
CTR	Used as input pin of selecting video signals sampling circuits and selecting input signals of output operational amplifiers.
SAM	Used as input pin for setting the selecting of normal sampling operation or 3-point simultaneous sampling operation. For normal sampling operation, video signals are sampled in order 1 LCD drive output. For 3-point simultaneous sampling operation, video signals are sampled in order simultaneously 3 LCD drive outputs. For either operation, sampling signals are shifted at every rise timing and fall timing of horizontal shift clock of CK pin (half clock) , and their sampling period is equal to the period of one clock.
RL	Used as input pin for setting the shift direction of video signals sampling sequence. Video signals are sampled in the order of from OS1 to OS240 when set to "H" and in the order of from OS240 to OS1 when set to "L".
CS1, CS2	Used as input pins for setting of chip cascade sequence. Set chip cascade sequence as shown in the table below. Cascade sequence / CS1 / CS2: 1st H H; 2nd L H; 3rd H L; 4th L L For details, refer to "6-2. Operation of function" on page 7.
MODE	Used as input pin for setting form of video signals for sampling. By mode setting circuit, video signals are sampled and output with respect to OS1 to OS240 in the order of VB, VA, and VC when set to "H" and in the order of VC, VB, and VA when set to "L". For details, refer to "6-2. Operation of function" on page 7. Do not use this function in "OPEN" condition.
Vb1	Used as pin for setting the bias voltage of operational amplifiers in output circuits.
Vb2	Used as pin for setting bias voltage of buffers in output circuits.
VA, VB, VC	Used as input pins of video signals. VB, VA, VC, ... VB, VA, VC or VC, VB, VA, ... VC, VB, VA are input with respect to LCD drive outputs OS1, OS2, OS3, ... OS238, OS239, OS240 by MODE pin setting condition.
OS1 to OS240	Used as LCD drive output pins. All output pins discharge simultaneously at the timing of internal discharge signal and after discharge is completed, they output voltage corresponding to sampled video signals.

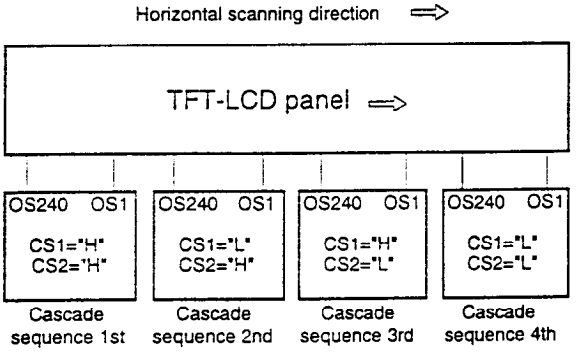
6.2 Operation of function

(1) Examples of cascade sequence

When RL="H"



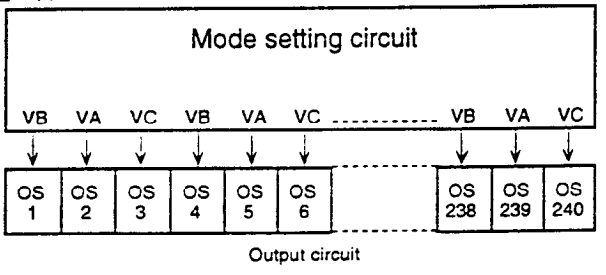
When RL="L"



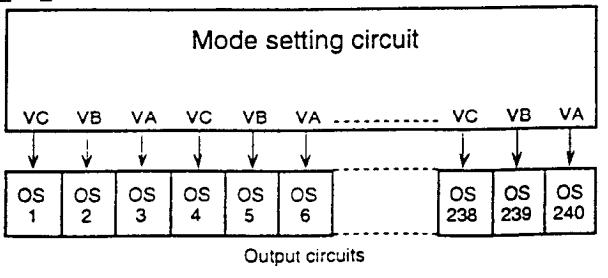
(2) Video signal mode setting function

With MODE pin condition, it is possible to set the form of video signals corresponding to each output pins by selecting the mode setting circuit.

When MODE="H"

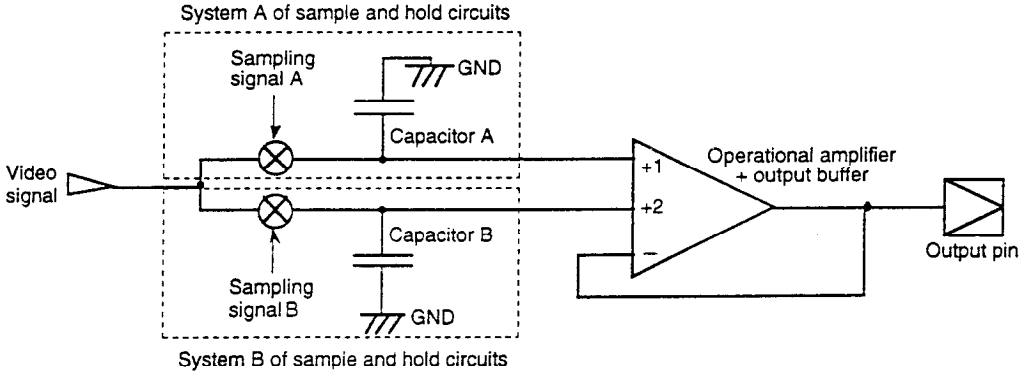


When MODE="L"

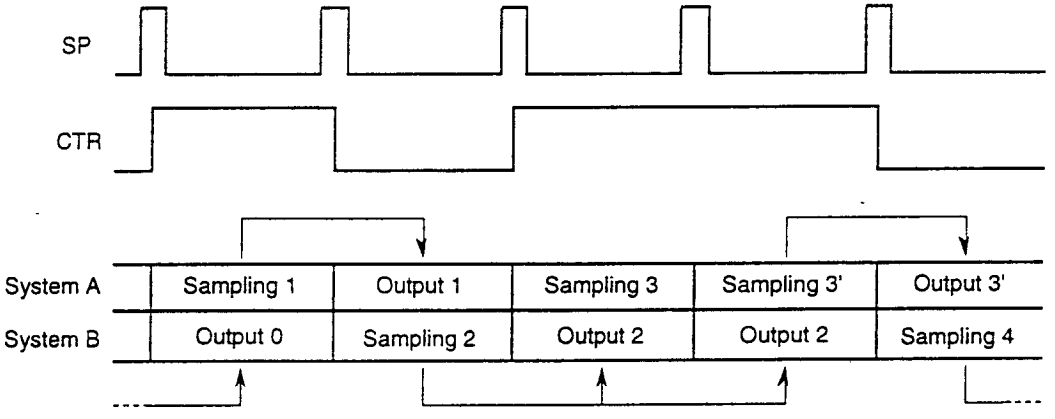


(3) Output circuit type

The LH1684F samples video signals by the sample and hold circuits of 2 systems and outputs the voltage corresponding to the sampled data by the input switching operational amplifiers. Sample and hold circuits and output circuits are as shown in the diagram below.
When CTR="H", the LH1684F samples the data to system A of the sample and hold circuits and outputs the voltage corresponding to the voltage sampled by capacitor B of system B.
When CTR="L", the LH1684F samples the data to system B of the sample and hold circuits and outputs the voltage corresponding to the voltage sampled by capacitor A of system A.



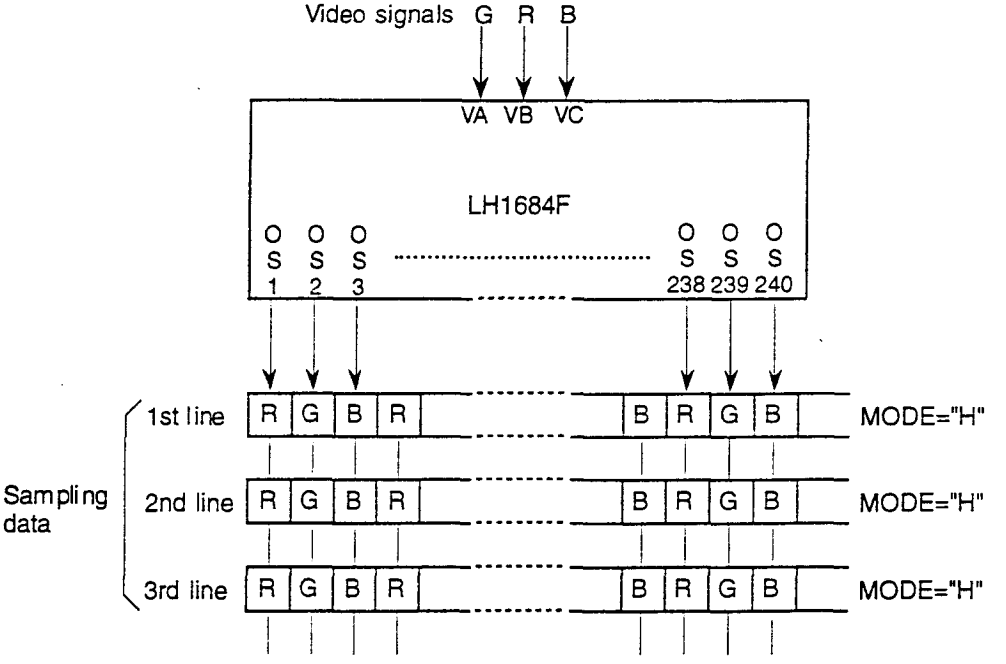
Therefore, it is necessary to repeat sampling operation and output operation by exchanging CTR signal to "H" and "L" for every SP signal, usually.
When CTR signal is set to "H" or "L" several times for SP signal, the same voltage is output continuously during such period.
The output voltage corresponds to the data sampled by the previous sampling operation.
Timing of operation is as follows.



(4) Examples of LCD panel connection

With the video signal mode setting function of (2), it is possible to connect LCD panel to the stripe pixel array panel and delta pixel array panel as shown in the following examples.

(a) Example of stripe pixel array panel connection



Connection of video signal input pins

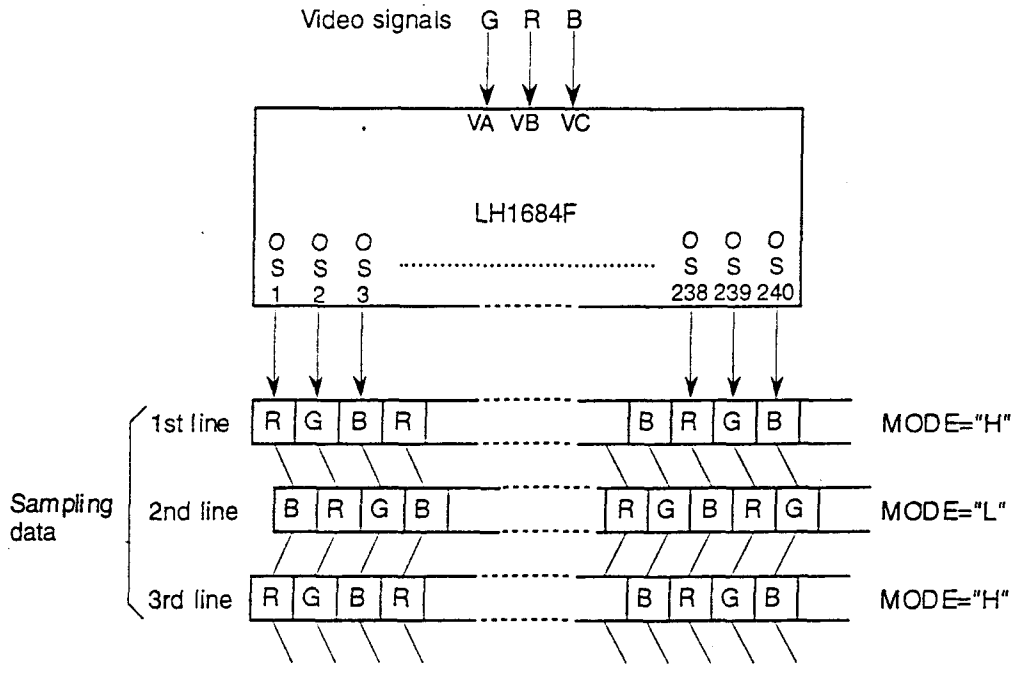
Video signal input pin	VA	VB	VC
Video signal	G	R	B

Setting of video signals sampled by output circuits and MODE pin condition

	1st line	2nd line	3rd line	After 4th line
OS (3n+1)	R	R	R	R
OS (3n+2)	G	G	G	G
OS (3n+3)	B	B	B	B
MODE pin setting	"H"	"H"	"H"	"H"

(n=0, 1, 2, . . . , 79)

(b) Examples of delta pixel array panel connection



Connection of video signal input pins

Video signal input pin	VA	VB	VC
Video signal	G	R	B

Setting of video signals sampled by output circuits and MODE pin condition

	1st line	2nd line	3rd line	After 4th line
OS (3n+1)	R	B	R	B and R are alternately selected.
OS (3n+2)	G	R	G	R and G are alternately selected.
OS (3n+3)	B	G	B	G and B are alternately selected.
MODE pin setting	"H"	"L"	"H"	"L" and "H" are alternately selected.

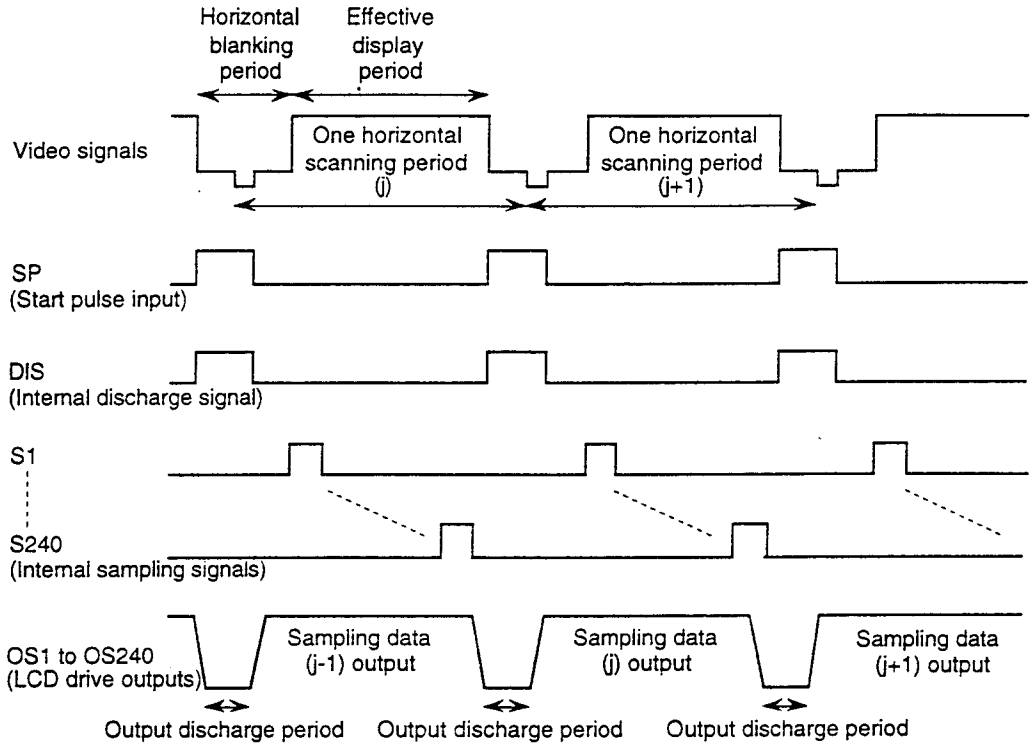
(n=0, 1, 2, . . . , 79)

Note 1. Set the MODE pin condition during output discharge period.

Note 2. Input the horizontal shift clock signal of CK pin by shifting the phase for each line according to the shift of the pixels connected to the same source bus line.
If the pixels connected to the same source bus line is shifted by half the pixels, change the clock phase 180 degrees.
Clock phase must be changed during output discharge period.

6.3 Outline of operation timing

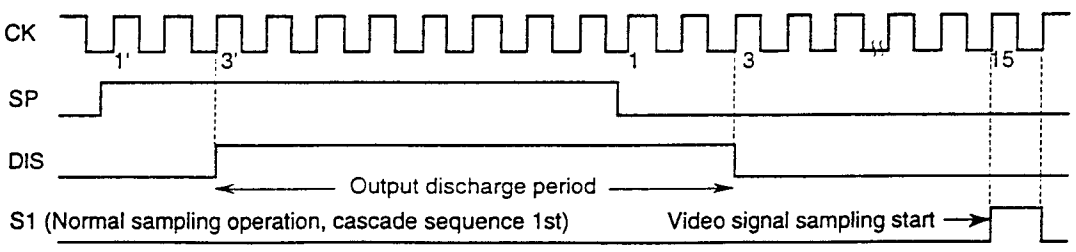
(1) Overall operation timing



Video signals of one horizontal scanning period are sampled into the sample and hold circuits at the timing of the internal sampling pulses of each output circuits, outputs are discharged once on the GND level by the internal discharge signal, and data corresponding to the sampled data are output.
This discharge operation is performed simultaneously for all output pins.

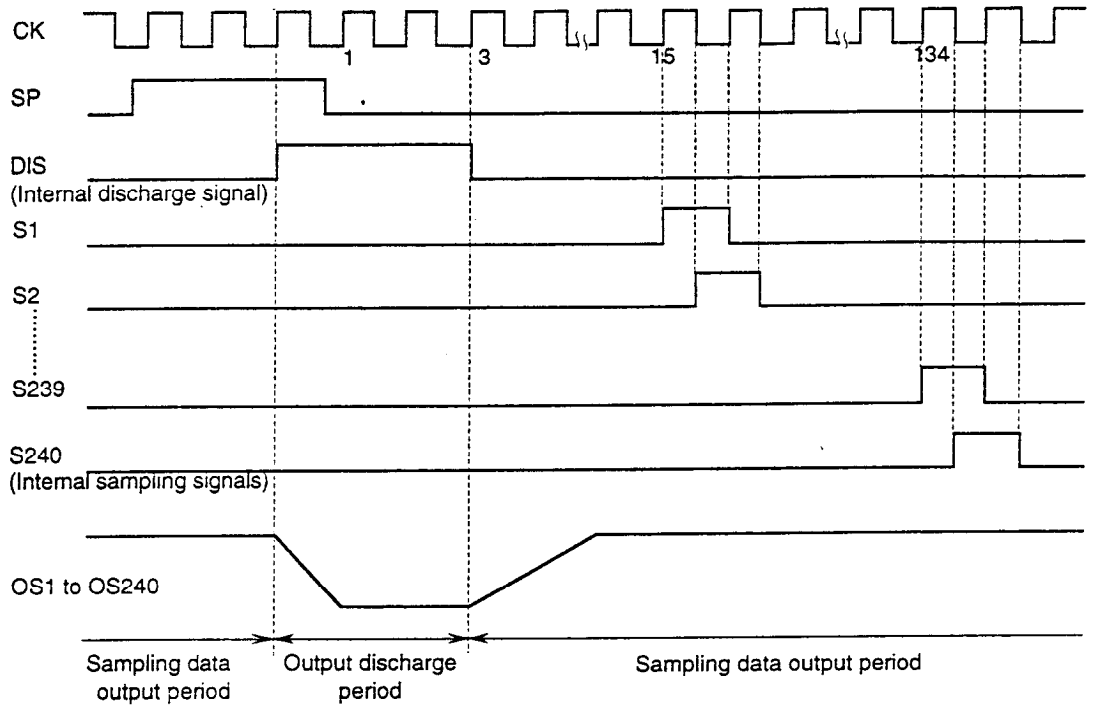
(2) Timing of output discharge and video signal sampling

The output discharge period (period "H" of the internal discharge signal DIS) is after 3 cycles of clock CK from the "H" period of start pulse SPD. Therefore, the output discharge period is almost the same period as the "H" period of start pulse SPD.
If the normal sampling operation and cascade sequence is 1st, the video signal sampling (internal sampling signal Sn) is started after 15 cycles of clock CK following the fall of start pulse SPD.

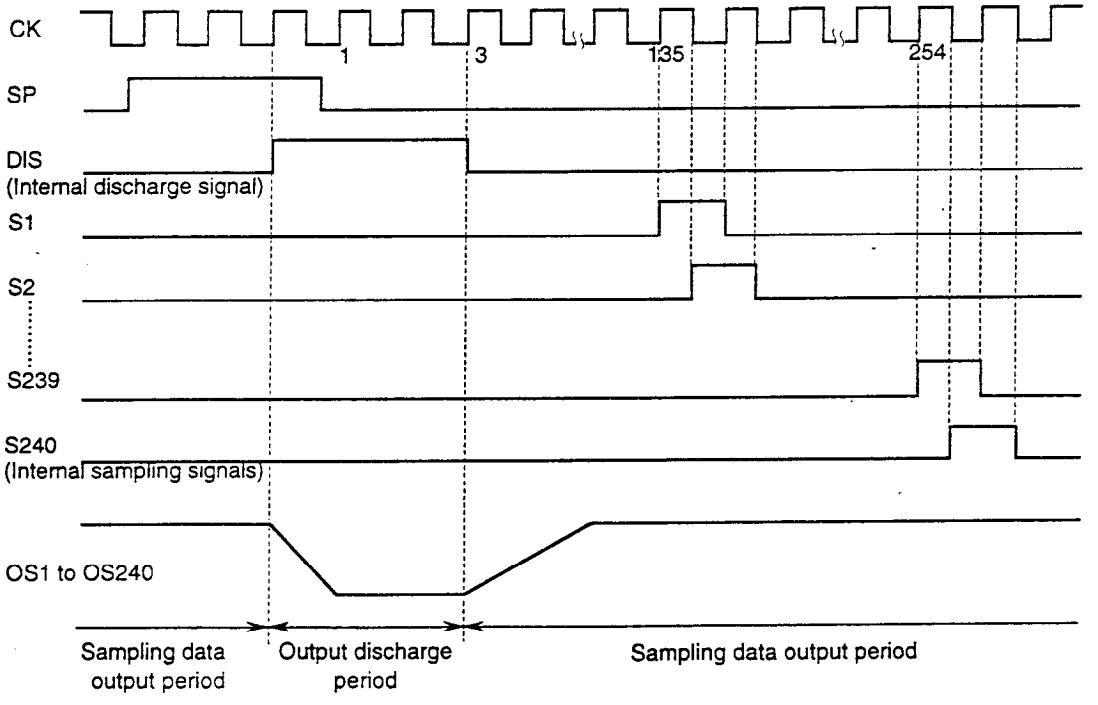


6.4 Timing chart for normal sampling operation

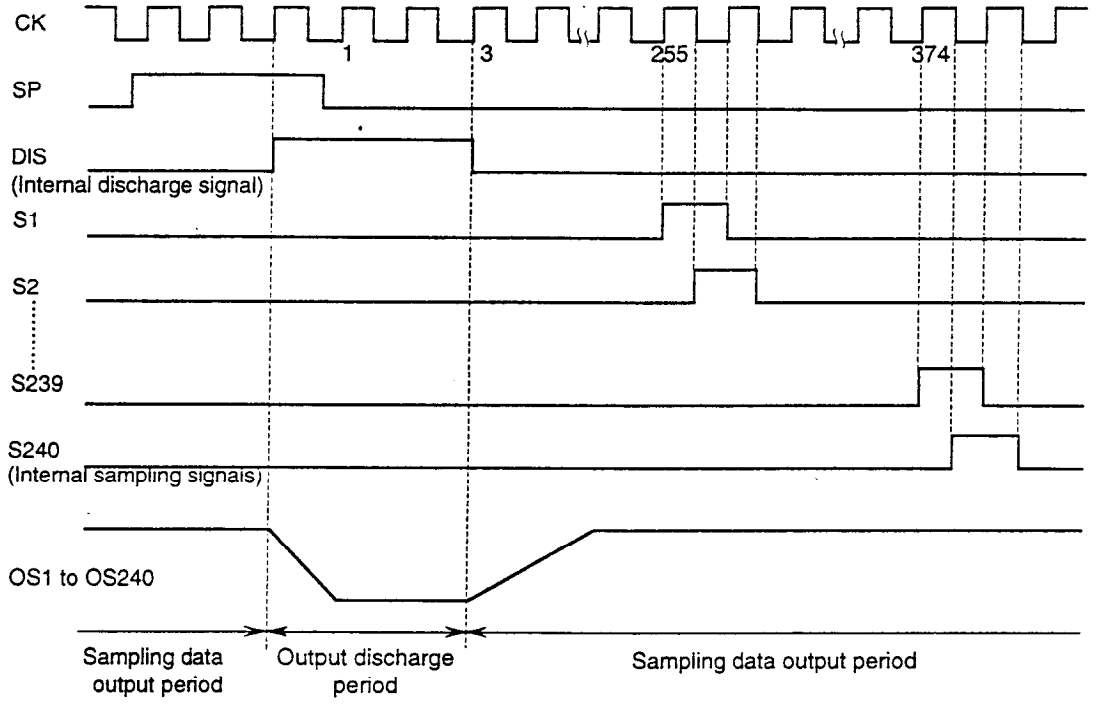
(1) When RL="H", CS1="H", and CS2="H"



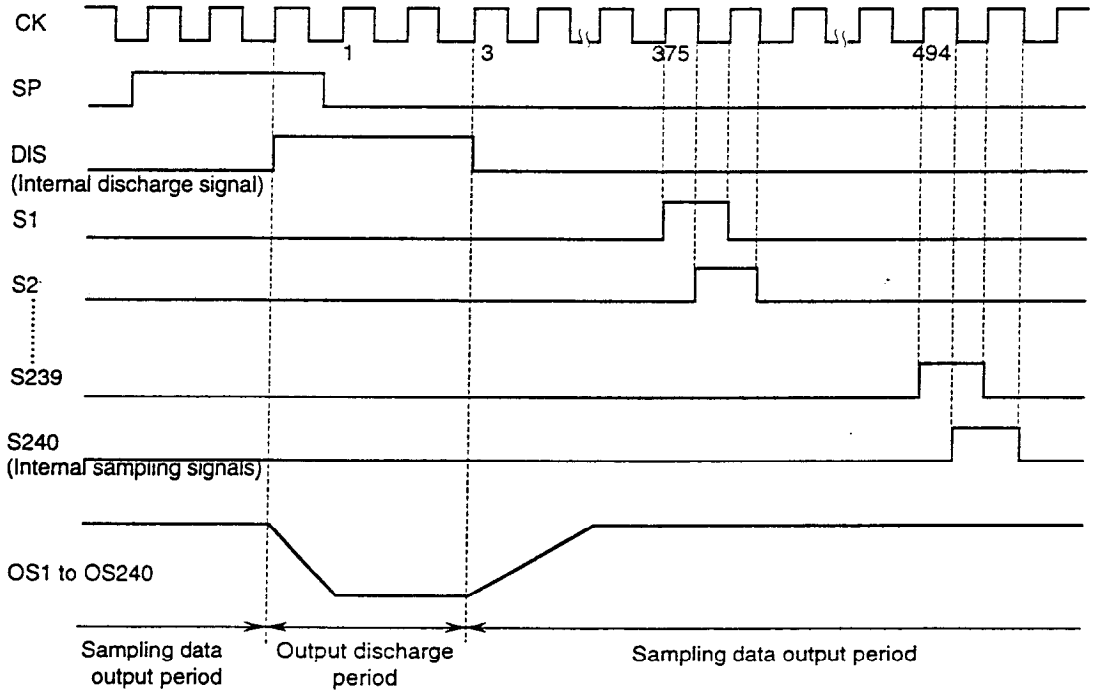
(2) When RL="H", CS1="L", and CS2="H"



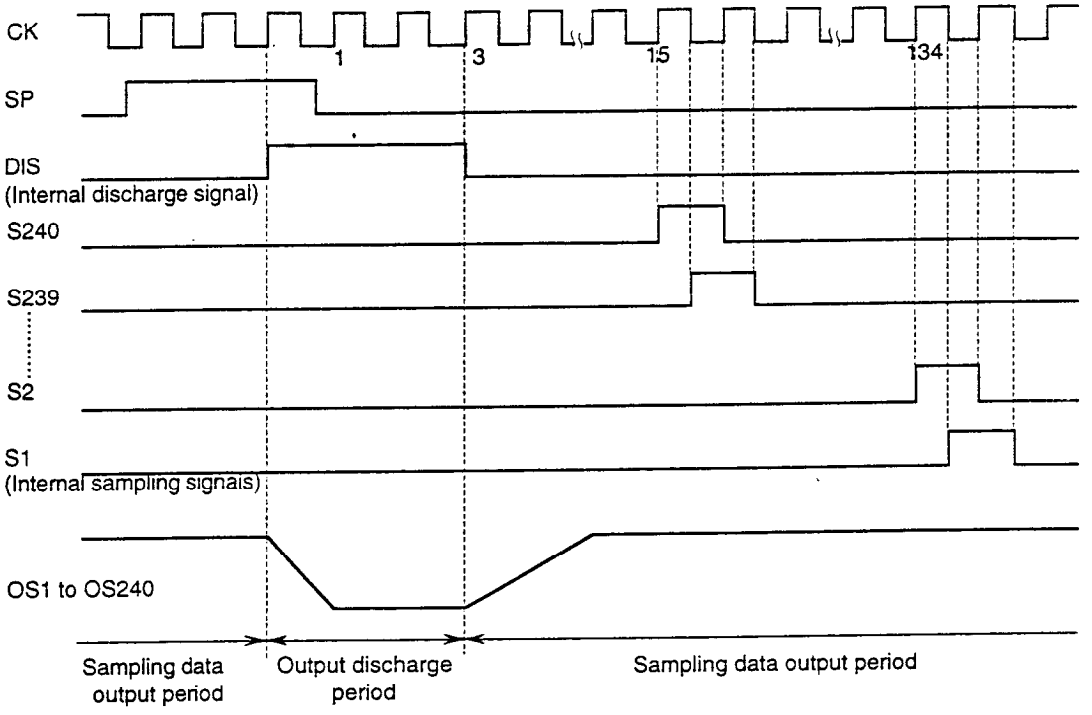
(3) When RL="H", CS1="H", and CS2="L"



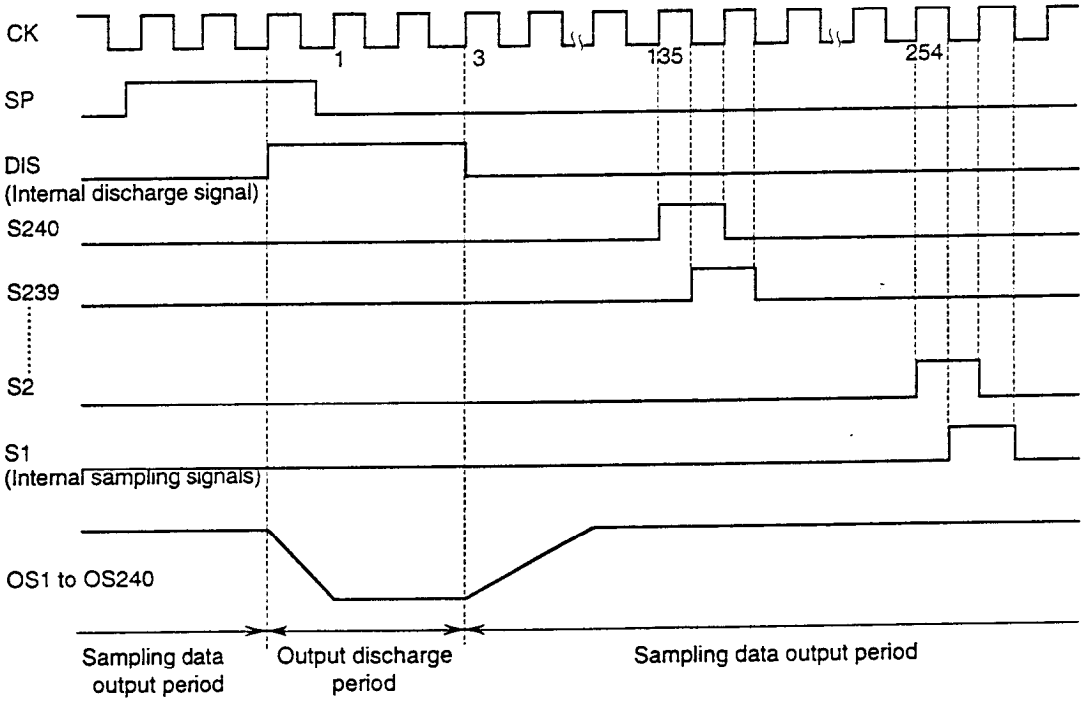
(4) When RL="H", CS1="L", and CS2="L"



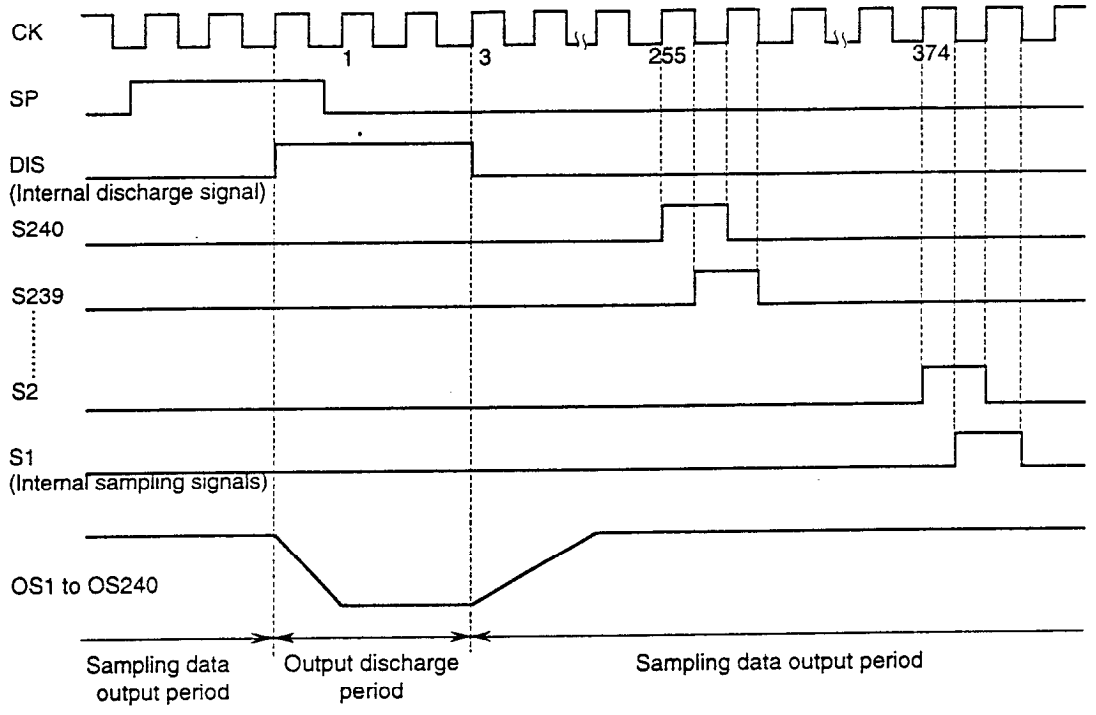
(5) When RL="L", CS1="H", and CS2="H"



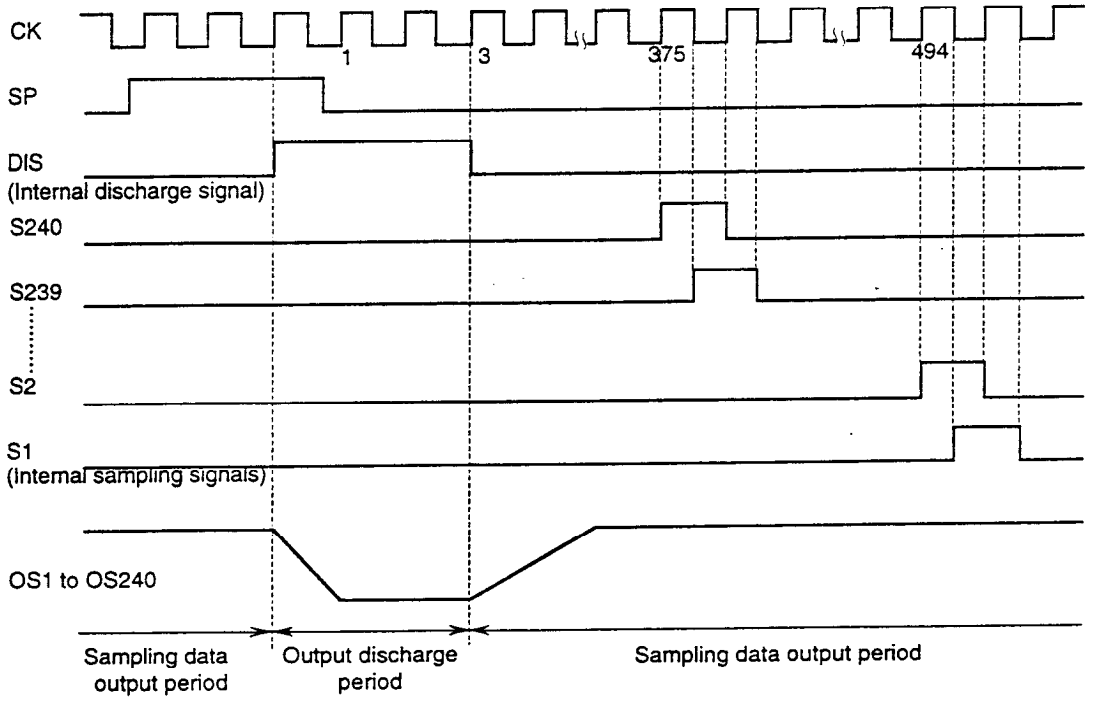
(6) When RL="L", CS1="L", and CS2="H"



(7) When RL="L", CS1="H", and CS2="L"

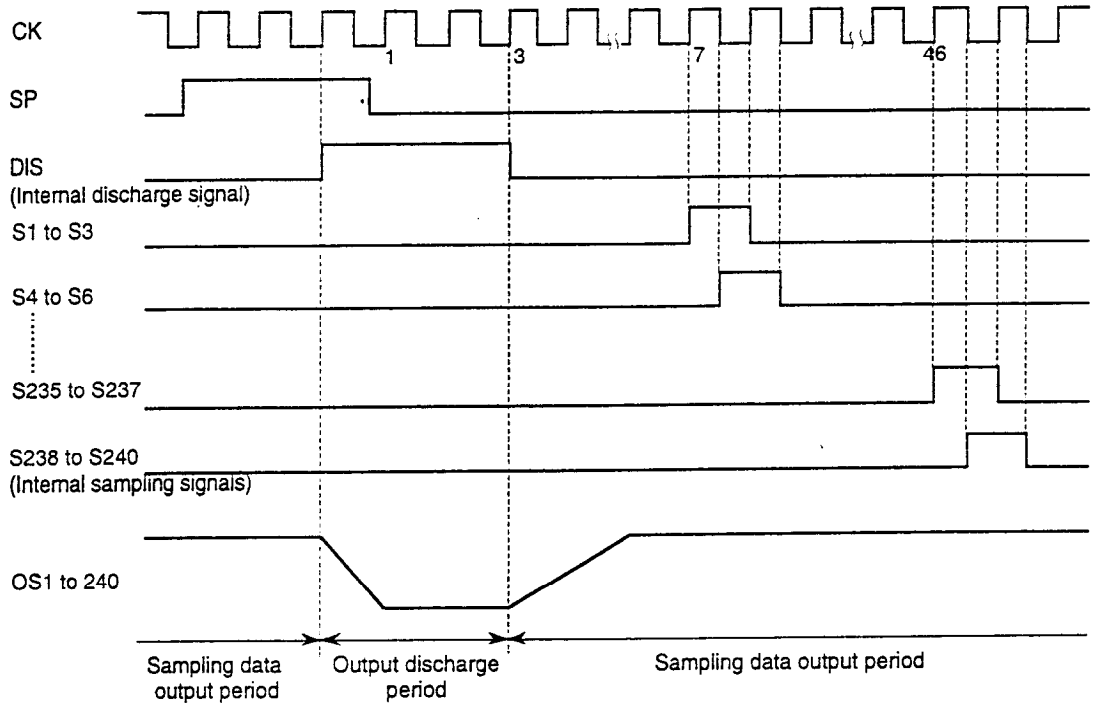


(8) When RL="L", CS1="L", and CS2="L"

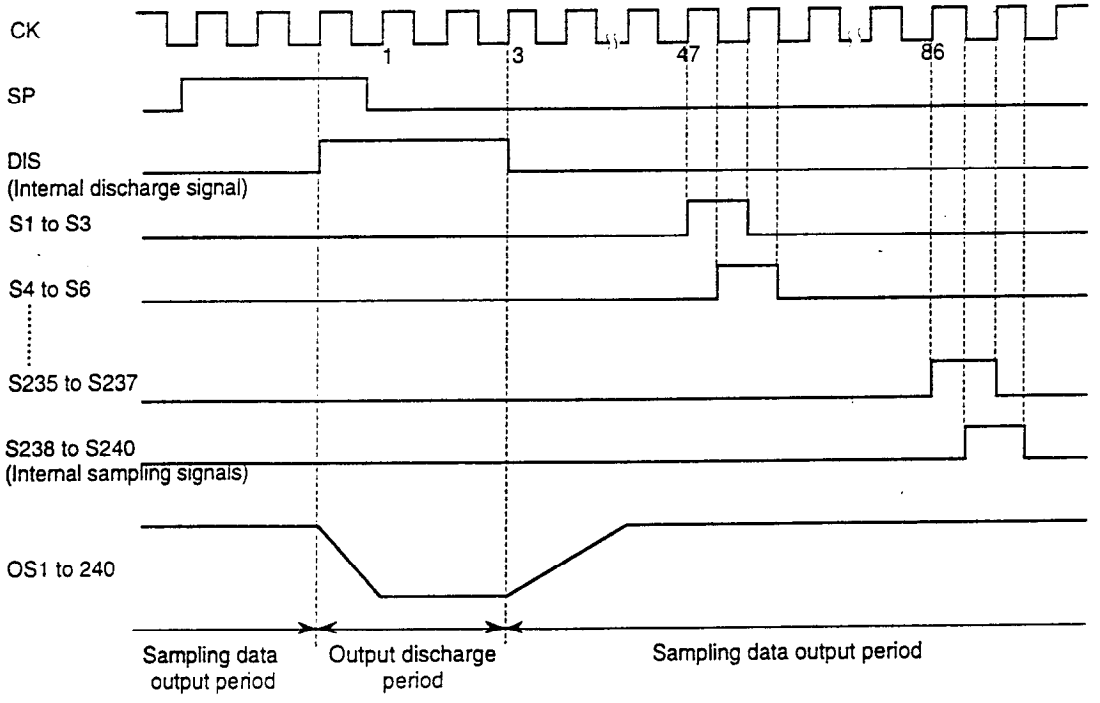


6.5 Timing chart for 3-point simultaneous sampling operation

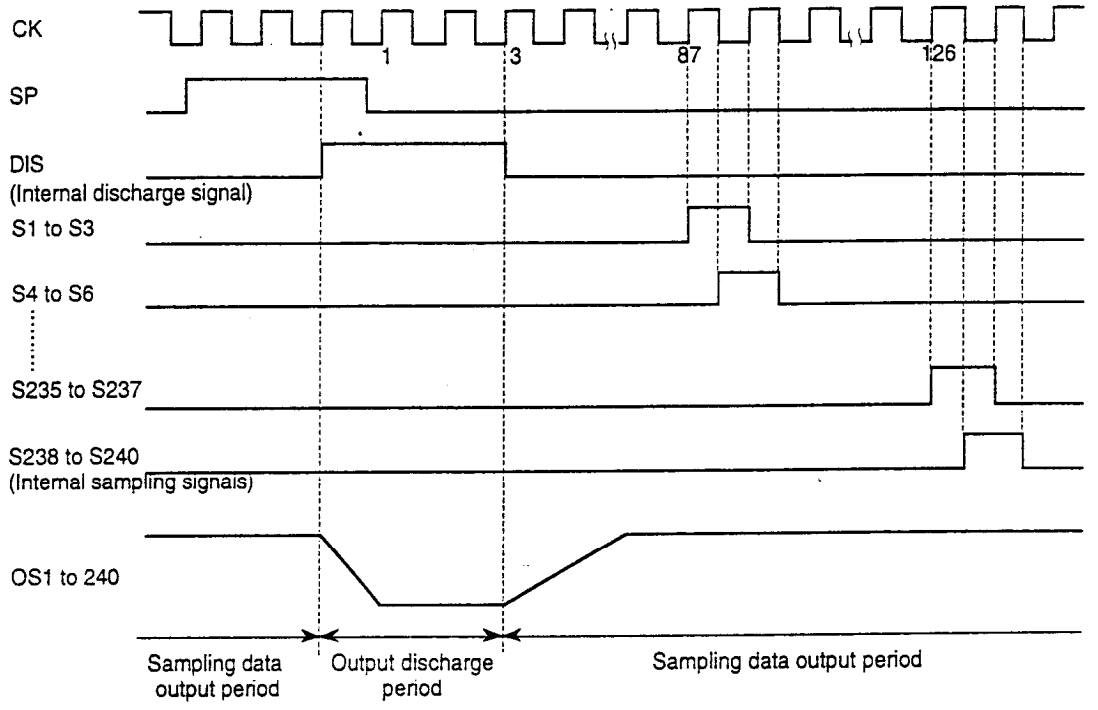
(1) When RL="H", CS1="H", and CS2="H"



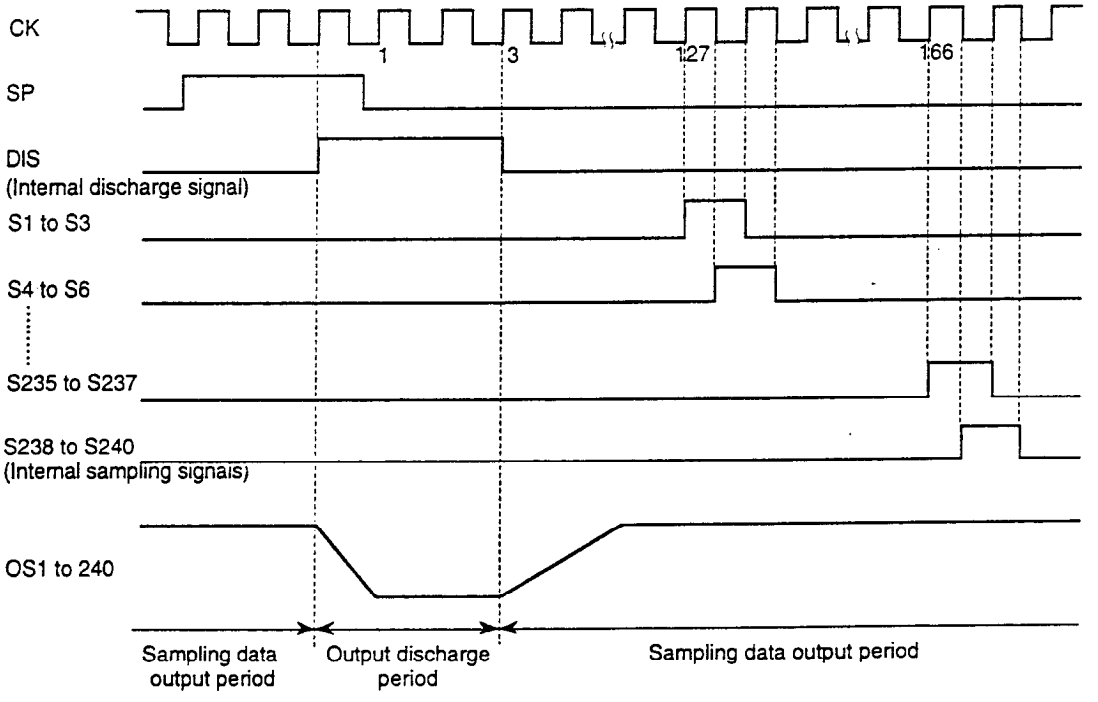
(2) When RL="H", CS1="L", and CS2="H"



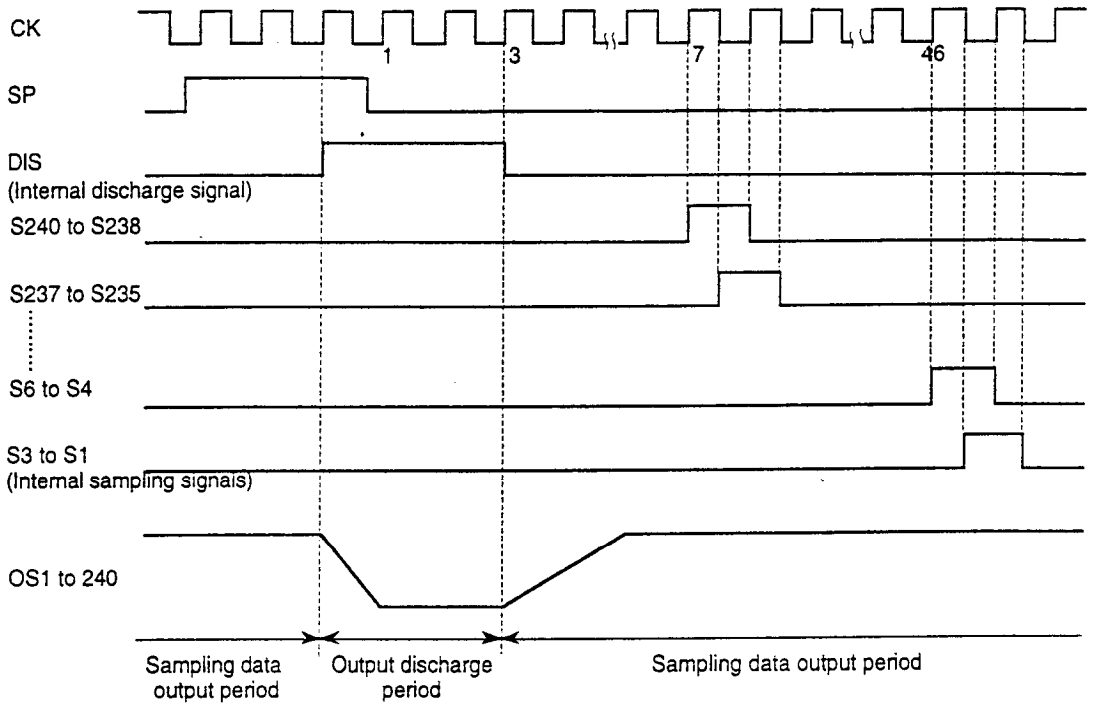
(3) When RL="H", CS1="H", and CS2="L"



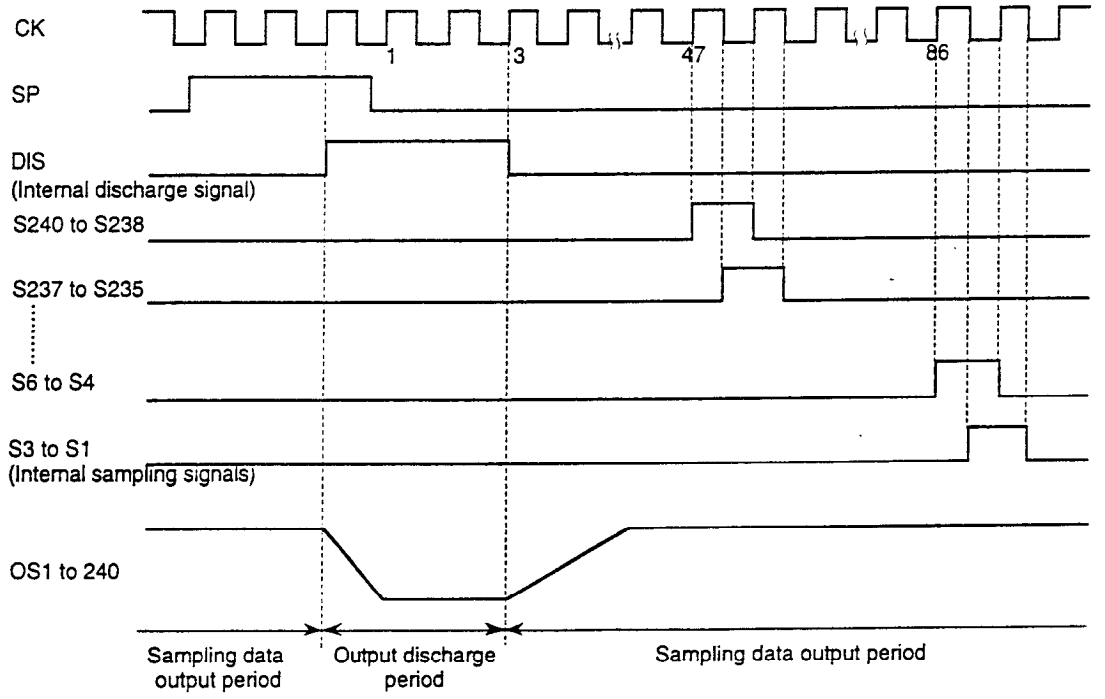
(4) When RL="H", CS1="L", and CS2="L"



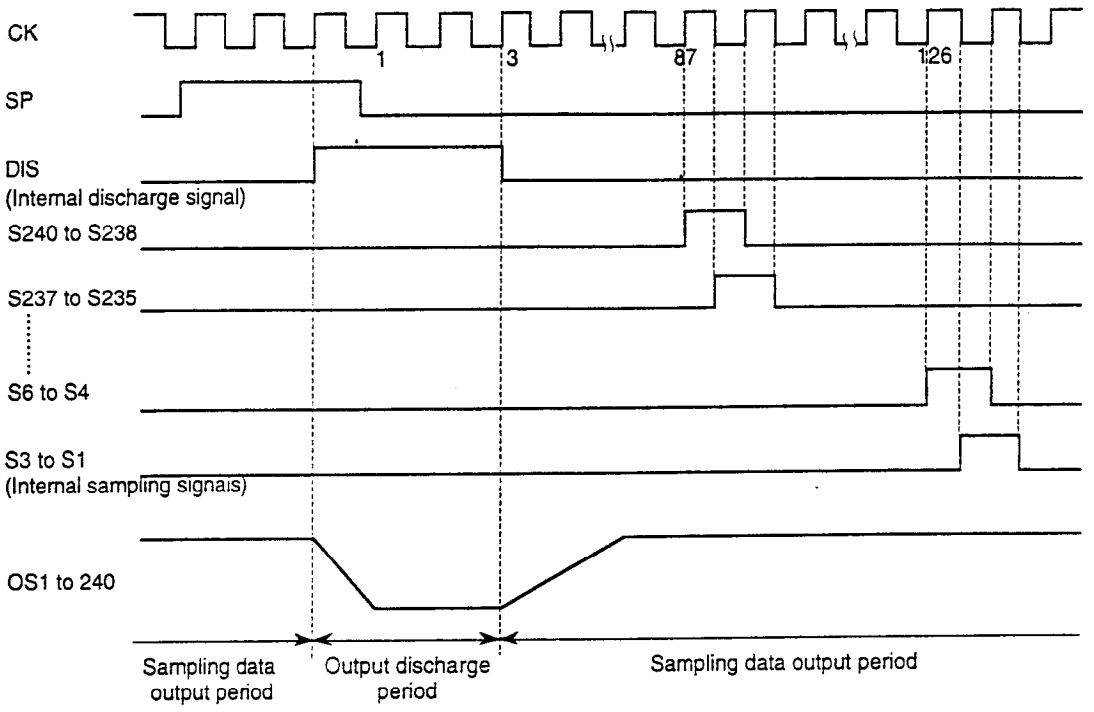
(5) When RL="L", CS1="H", and CS2="H"



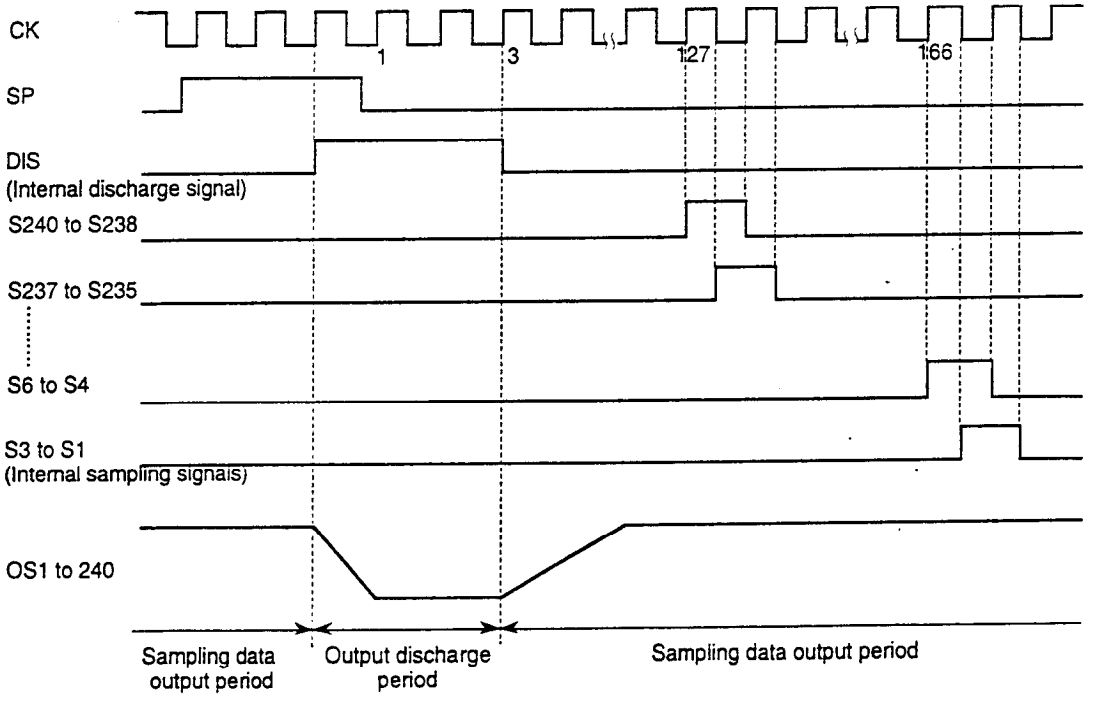
(6) When RL="L", CS1="L", and CS2="H"



(7) When RL="L", CS1="H", and CS2="L"



(8) When RL="L", CS1="L", and CS2="L"

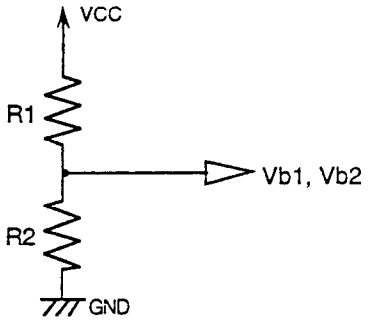


6.6 Precautions

(1) Setting of external voltage of Vb1 and Vb2 pins

The LH1684F does not have the bias voltage setting circuit for the output operational amplifiers and the output buffers. Therefore it is necessary to input the suitable voltage to Vb1 pin and Vb2 pin.
Set the voltage value to an optimum value in the range of Vcc to GND as shown in the diagram below, fully evaluating the current consumption, picture quality, etc.

(Example of bias circuit)



Set the resistance to R1+R2=50 kΩ

(2) Setting of Input pins

Since 6 pins of SP, CK, CTR, MODE, Vb1, and Vb2 of the input pins are not pulled up or pulled down in the LSI, never use these 6 pins in the "OPEN" condition.
Since VA, VB, and VC pins are for inputting video signals, necessary video signals must be input always.
Except VA, VB, VC, Vb1, Vb2, SP, CK, CTR, and MODE, all other input pins are pulled up or pulled down in the LSI. However,because of preventing malfunction due to noise, etc., avoid using the "OPEN" condition whenever possible, and set to "H" level or "L"level.

(3) Input video signals

Input video signals are target for analog signals (continuous signals).
The input band of video signals is applicable up to the maximum of 10 MHz.

(4) Bypass capacitor

If the noise of a logic system is superposed on analog circuits such as the sample and hold circuits, analog characteristics (such as output voltage deviation and dynamic range,etc.) may deteriorate. For this reason, insert bypass capacits or of about 1 µF between VCC and GND. Fully evaluate and determine the value of bypass capacits or with actually mounted on the LCD panel.

7. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	Ta=+25 °C	−0.3 to +7.0	V
Input voltage	V_{INCC}	Ta=+25 °C	−0.3 to V_{CC} +0.3	V
Storage temperature	T_{stg}		−45 to +125	°C

Note:Standard voltage is GND (0 V).

8. Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		+4.5 to +5.5	V
Input voltage	V_{INCC}		0 to V_{CC}	V
Operating temperature	T_{opr}		−30 to +85	°C

Note:Standard voltage is GND (0 V).

9. Electrical Characteristics

9.1 DC characteristics

Parameter	Symbol	Measuring condition	MIN	TYP	MAX	Unit	Applicable pin
Input "L" voltage	V_{IL}		0		0.3V_{CC}	V	Pins 1, 2, and 3
Input "H" voltage	V_{IH}		0.7V_{CC}		V_{CC}	V	
Input "L" current	I_{IL1}	V_{IN}=0 V			1.0	µA	Pins 1, and 3
	I_{IL2}				50.0	µA	Pins 2
Input "H" current	I_{IH1}	V_{IN}=V_{CC}			1.0	µA	Pins 1, and 2
	I_{IH2}				50.0	µA	Pins 3
Dynamic range	V_{PP}		0.5		V_{CC}−0.5	V	VA, VB, VC
Output voltage deviation	V_{OD}	(Condition 1)			50.0	mV	OS1 to OS240
Current consumption	I_{CC}	(Condition 2)			6.0	mA	VCC

Unless otherwise specified, GND=0 V, Vb1=Vb2=2.0 V, Ta=−30 to +85 °C.

[Applicable pins]

(Pin 1) Applicable to CK, CTR, SP, and MODE pins.
(Pin 2) Applicable to RL, CS1, CS2, SAM, TST, and TST1 to 4 pins.
(Pin 3) Applicable to TST5 pin.

[Measuring condition]

(Condition 1) SP signal : Cycle t_{SP} = 63.5 µs, "H" period width t_{WHP} = 5.0 µs
CTR signal : Cycle t_{CTR} = 127.0 µs, "H" period width t_{WHCT} = 63.5 µs
Change from "H" to "L" and vice versa during "H" period of SP signal.
CK signal : Frequency f_{CK} = 10.0 MHz
Pin to be set to 2.0 V : Vb1, Vb2
Pin to be set to GND : TST5
VA=VB=VC=0.5 V to V_{CC}−0.5 V
Connect all other pins to V_{CC}.
Difference between the output voltage mean value of all OS output pins in the chip and the output voltage of each OS output pin.
Ta=25 °C

(Condition 2) SP signal : Cycle t_{SP} = 63.5 µs, "H" period width t_{WHP} = 5.0 µs
CTR signal : Cycle t_{CTR} = 127.0 µs, "H" period width t_{WHCT} = 63.5 µs
Change from "H" to "L" and vice versa during "H" period of SP signal.
CK signal : Frequency f_{CK} = 10.0 MHz
Pin to be set to 2.0 V : Vb1, Vb2
Pin to be set to GND : TST5
Connect all other pins to Vcc.

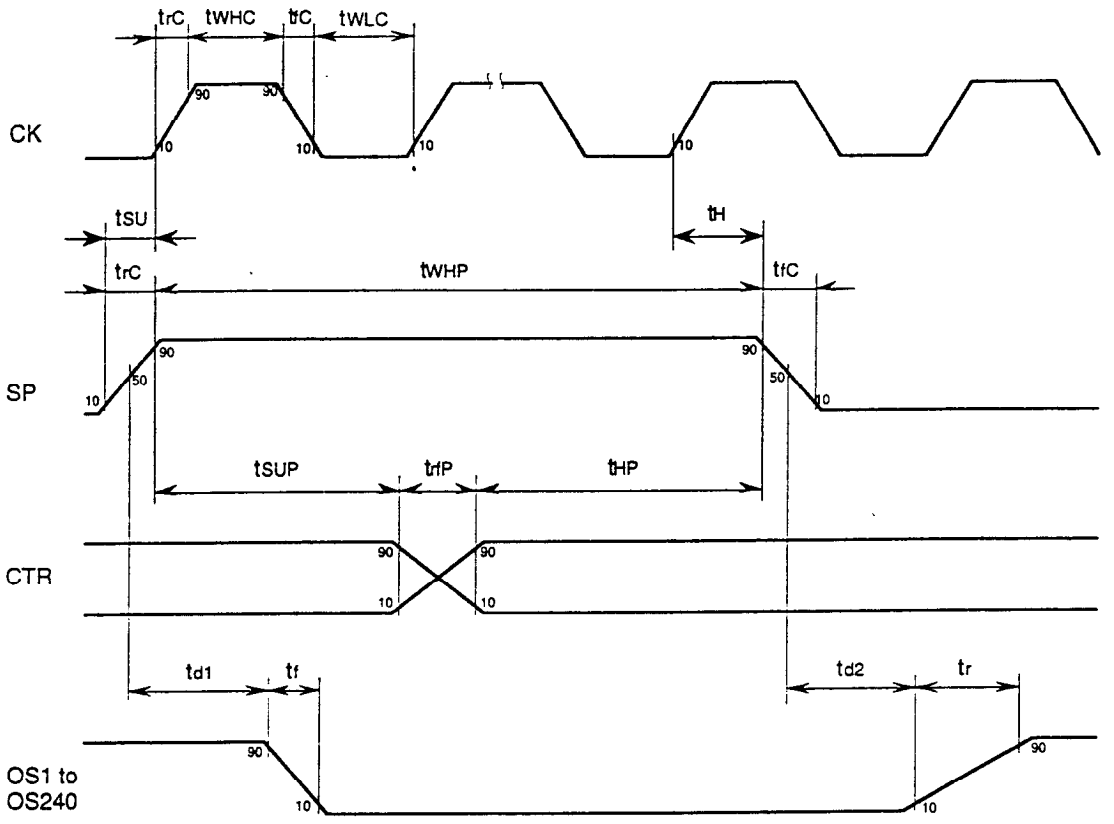
9.2 AC characteristics

Parameter	Symbol	Measuring condition	MIN	TYP	MAX	Unit	Applicable pin
Clock frequency	f_{CK}	SAM="H"			10.0	MHz	CK
		SAM="L"			4.0	MHz	
"H" level clock width	t_{WHC}	SAM="H"	40.0			ns	
		SAM="L"	90.0			ns	
"L" level clock width	t_{WLC}	SAM="H"	40.0			ns	
		SAM="L"	90.0			ns	
Clock rise time	t_{rC}	SAM="H"			10.0	ns	CK, SP
		SAM="L"			35.0	ns	
Clock fall time	t_{fC}	SAM="H"			10.0	ns	
		SAM="L"			35.0	ns	
Data setup time	t_{SU}		30.0			ns	
Data hold time	t_H		30.0			ns	
Pulse setup time	t_{SUP}		0.5			µs	SP, CTR
Pulse hold time	t_{HP}		0.5			µs	
"H" level pulse width	t_{WHP}		5.0			µs	SP
Pulse alteration time	t_{rfP}				1.0	µs	CTR
Output transfer delay time	t_{d1}	(Condition)			0.7	µs	SP
	t_{d2}				2.0	µs	OS1 to OS240
Output rise time	t_r			1.5	3.0	µs	OS1 to OS240
Output fall time	t_f			1.0	2.0	µs	

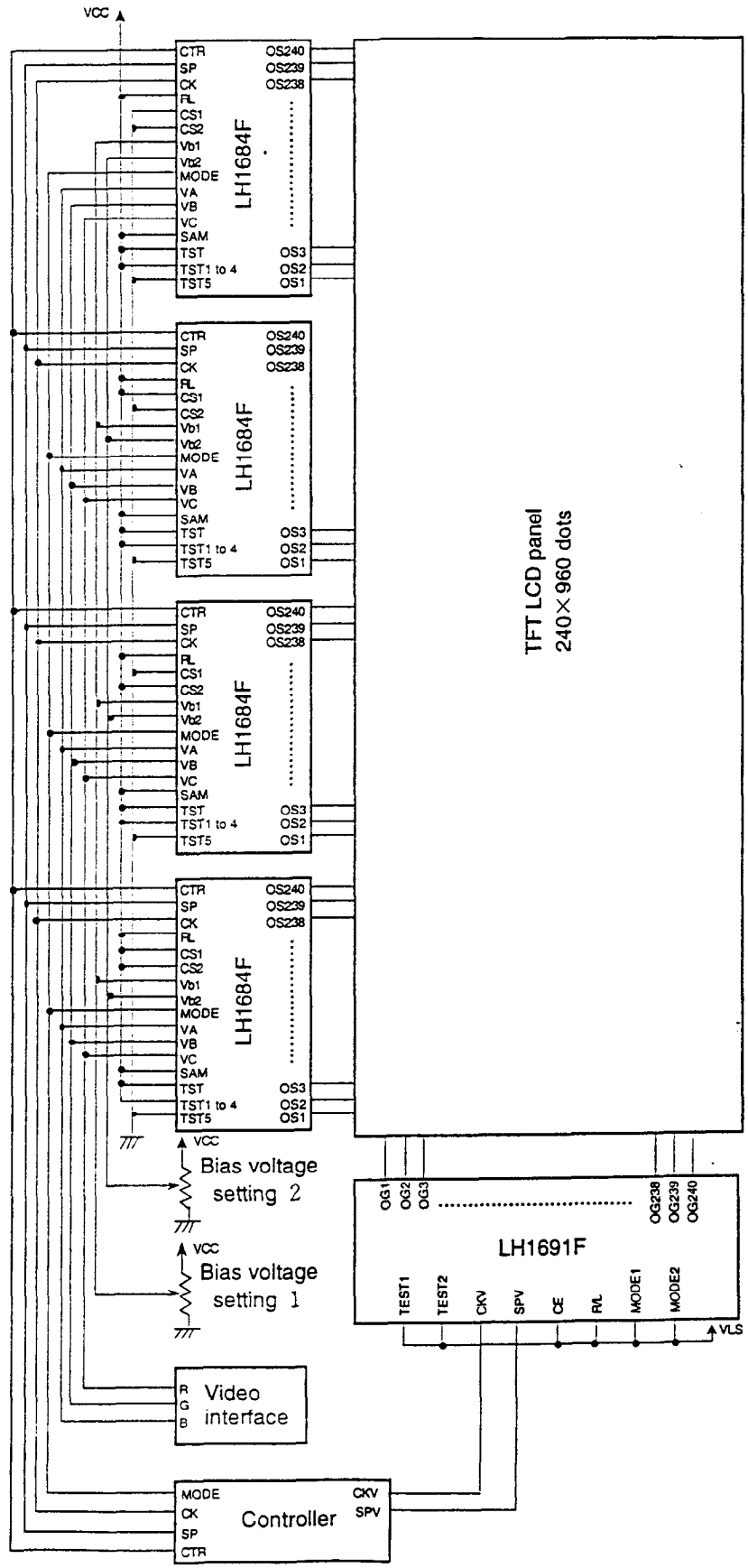
Unless otherwise specified, GND=0 V, Vb1=Vb2=2.0 V, Ta=−30 to +85 °C.

[Measuring condition]
(Condition) SP signal : Cycle t_{SP} = 63.5 µs, "H" period width t_{WHP} = 5.0 µs
CTR signal : Cycle t_{CTR} = 127.0 µs, "H" period width t_{WHCT} = 63.5 µs
Change from "H" to "L" and vice versa during "H" period of SP signal.
CK signal : Frequency f_{CK} = 10.0 MHz
Pin to be set to 2.0 V : Vb1, Vb2
Pin to be set to GND : TST5
Connect all other pins to Vcc.
Capacity of output load C_L=150pF

9.3 Timing diagram



10. Example of System Configuration



11. Example of Typical Characteristics

Parameter	Conditions	MIN	TYP	MAX	Unit
Basic gate propagation delay time	GND=0 V, Vcc=+5.0 V, Ta=+25 ℃		10		ns

12. PACKAGE AND PACKING SPECIFICATION

1. Package Outline Specification
   Refer to drawing No. SPN4701-00
2. Markings
   The meanings of the device code printed on each tape carrier package are as follows.
   (1) Date code (example) : 5 3 8 D 0
   a) b) c) d)
   a) denotes the last figure of Anno Domini (of production)
   b) denotes the week (of production)
   c) denotes factory code (of production)
   d) denotes the number of times of alteration
3. Packing Specifications
   3-1 Packing Materials

Item	Material	Purpose
Reel	Anti-static treated plastic (405 mm dia.)	Packing of tape carrier package.
Separator	Anti-static treated PET (188 μ mt)	Protects device and prevents ESD (Electro Static Discharge)
Alminium laminated bag	(520×600 mm)	Keeping dry.
Adhesive tape paper		Fixing of tape carrier package and sparator.
Label	Paper	Indicates production name, lot.No., and quantity.
Desiccant	Silica gel	Drying of device
Inner carton	Cardboard(420×420×50mm)	Contains a reel.
Outer carton	Cardboard(445×285×450mm)	Contain 4 inner cartons.

   3-2 Packing Form
   a) Tape carrier package(TCP) is wound on a reel with separator and the ends of them are fixed with adhesive tape.
   b) A label indicating production name, lot no. and quantity is stuck on one side of the reel.
   c) The reel and silica gel is put in a laminated aluminium bag. Nitrogen gas is enclosed in the bag and the bag is sealed. The same label(b) is affixed to the bag. The bag is put in a carton and the same label(b) is affixed to one side of the inner carton.
   d) 5 inner cartons are put in an outer carton and the same label(b) is affixed to one side of the outer carton.

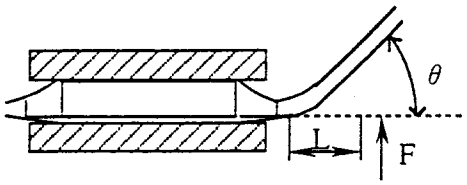
   * Specification of label

TYPE	
	Production name Lot No.
QUANTITY	Quantity
LOT(DATE)	Shipping date

   3-3 Other
   (1) The length of the TCP is typically 40 m per reel, but this may change in accordance with the inventory quantity.
   (2) Faulty devices is conpletely punched out at the part of the device.
   (3) The maximum number of continuous faulty devices is 9.

ISSUE DATE	AUG 28.1996	APPROVE	CHECK	DESIGN	(NOTE)
ISSUE NUMBER	H8801				
S/C NUMBER		M. Kanishi	Y. Honda	T. Yamasita	

4. Cautions concerning handling.
Althrough the strength of the device has been verified in accodance with the test method shown below, do not subject the resin parts or the slit terminals to any excessive bending or pressure.

Test	Test method	Rating
Flexure test		Indicate as moment M. M=F×L (N·m) $M=1.47\times10^{-3}$ N·m MAX. (for both $+\theta$ and $-\theta$)

5. Cautions concerning storage.

· When storing the product, it is recommended that it be left in its shipping package. After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.

· Strage conditions

Strage state	Strage conditions
Unopened(less than 60 days)	Temperature: 5 to 30℃; humidity : 80% RH or less.
After seal of broken	Room temperature, dry nitrogen atomosphere.

· Don't store in a location exposed to corrosive gas or excessive dust.

· Don't store in a location exposed to direct sunlight or subject to sharp changes in temperature.

· Don't store the product such that it subjected to an excessive load weight, such as by stacking.

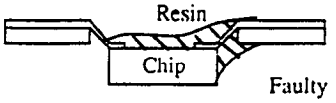
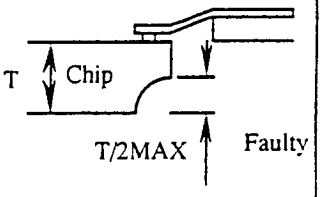
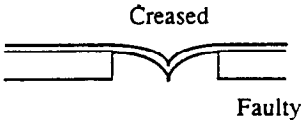
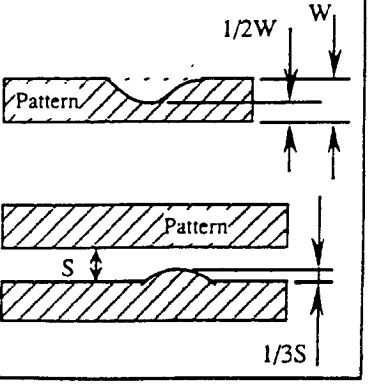
· Deterioration of the plating may occor after long-term storage, so special care is required.
It is recommended that the products be inspected before use.

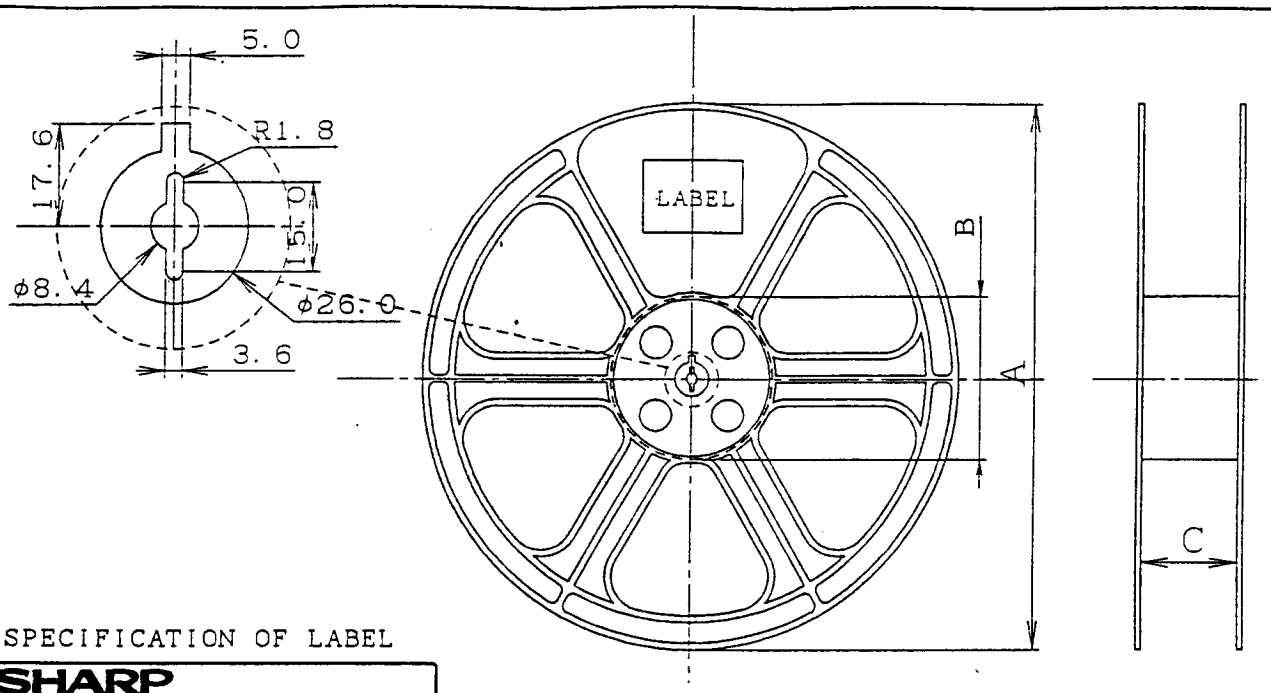
6. Other cautions.

· Immediately after opening the moisture-proof packing, the mesurement will shrink slightly. In oder to return the mesurements to those shown in the drawing, it is nessesary to store the product for at least 48 hours at a temperature of 20 to 25℃ and humidity of 50 to 60%.

7. External appearance inspection

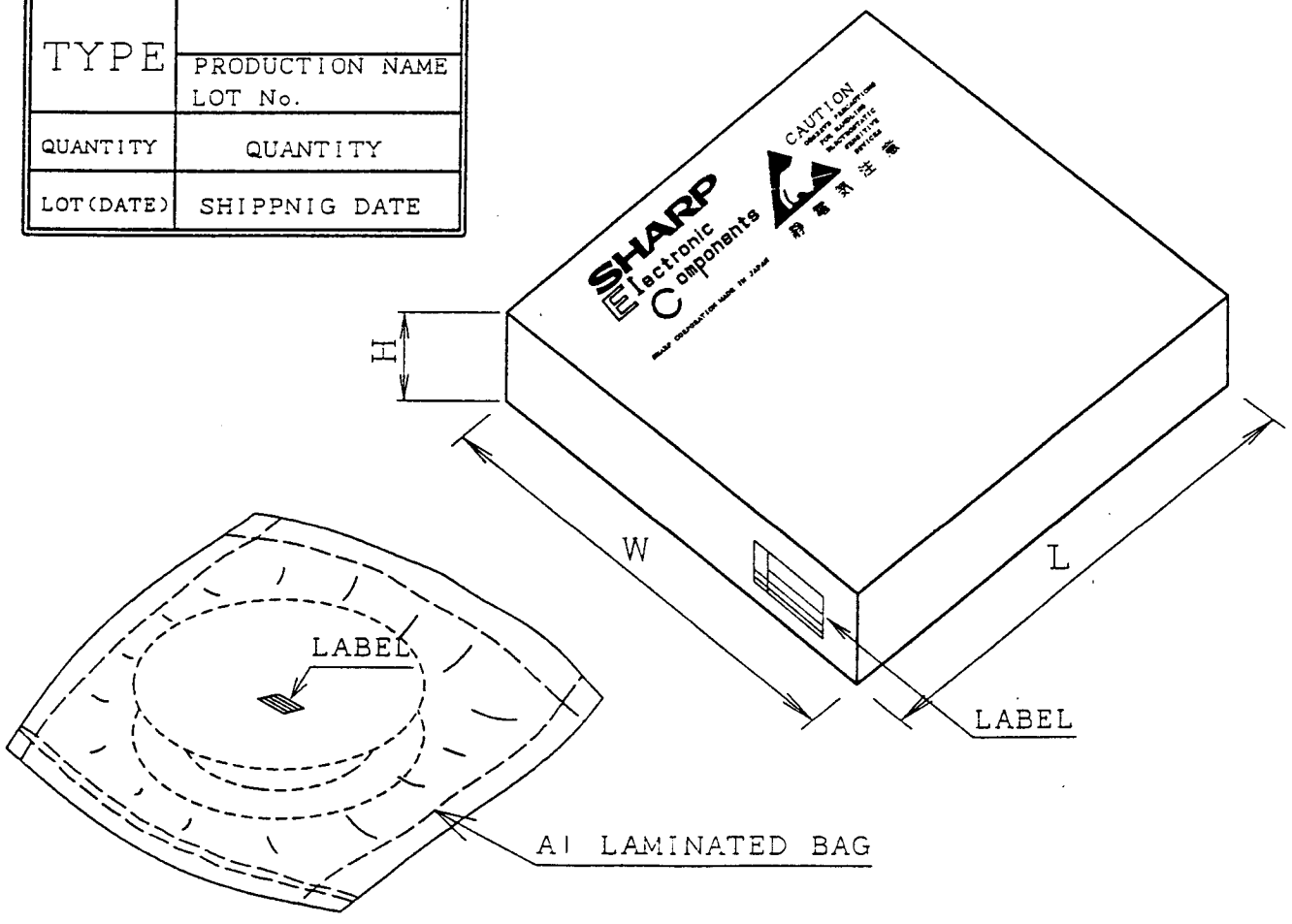
The standards for the inspection of the external appearance of the package are shown below.

Item	Inspection standards	Remarks
1. Exposure of the inner leads and device holes	·Faulty if the chip or inner leads are completely exposed. ·Faulty if the device holes are not completely filled with resin.	
2. Air bubbles	·Faulty if there are air bubbles extending as far as the suaface of the chip. ·Faulty if there are air bubbles at the inner leads.	
3. Seal resin area	·Faulty if the area of the seal resin area exceeds the specifications.	Upperside:16.5×5.2 mmMAX Underside:16.5×5.2 mmMAX
4. Seal resin thickness	·Faulty if the thickness of the device exceeds the specifications.	Upperside:0.30 mmMAX Underside:0.75 mmMAX Total thickness:1.20 mmMAX
5. Adherance of resin or foreign matter except the seal resin area.	·Faulty if there is anything adhering to the tin plating. ·Faulty if any resin or forein matter adhered to the copper pattern is wider than the width of the pattern. (If the forein matter is easily moved, it is not a cause for concern.)	
6. Undrside of the chip	·Faulty if there are any cracks in the chip. ·Faulty if there is any chipping in the underside of the chip that is lager than one-half the thickness of the chip. ·Faulty if adherance of the resin to the underside of the chip that causes the thickness of the devices exceed the specifications.	
7. Scratches, cracks and chipping in the tape carrier	·Faulty if there are any scratches exposing the sustrate (chip, pattern, or inner leads) at the seal resin. ·Faulty if there are any scratches extending as far as the copper foil at the sorder resists. ·Faulty if there are any cracks or chipping at the perforations.	
8. Pattern deformation	·Faulty if the pattern overhanging the slits is markedly deformed	
9. Discoloration	·Faulty if the tin plating is markedly discolored. ·Faulty if the cover coating is markedly discolored.	
10. Markings	·Faulty if the markings are illegible.	
11. Missing parts of output leads	·Faulty if the width of the output lead is reduced to less than one-half of the standard. ·Faulty if copper foil remnants reduce the clearance between the output leads to less than two-thirds of the standards.	
12. Other	·Faulty if there is any warping, twisting, bending, etc., of the tape that would impair use. ·Faulty if there are no indication holes at the non-effective indication holes.	

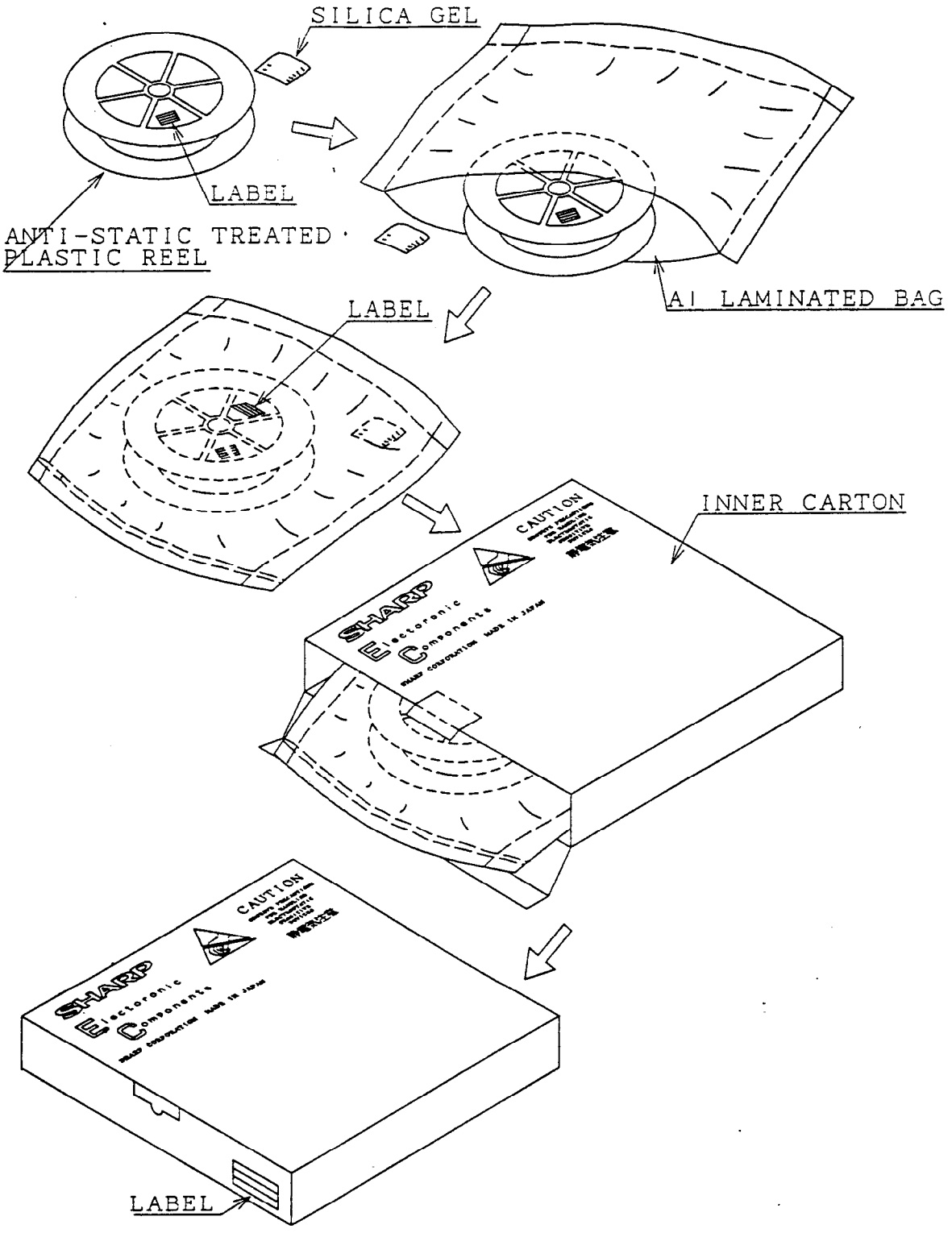


SPECIFICATION OF LABEL

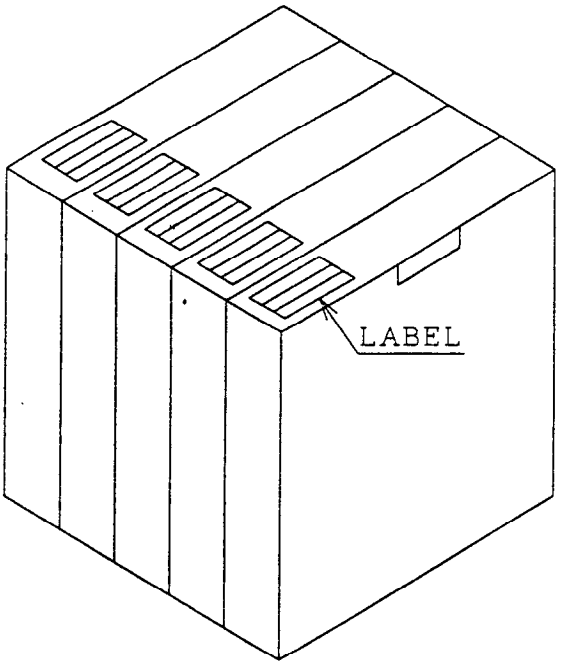
SHARP	
TYPE	PRODUCTION NAME LOT No.
QUANTITY	QUANTITY
LOT(DATE)	SHIPPNIG DATE

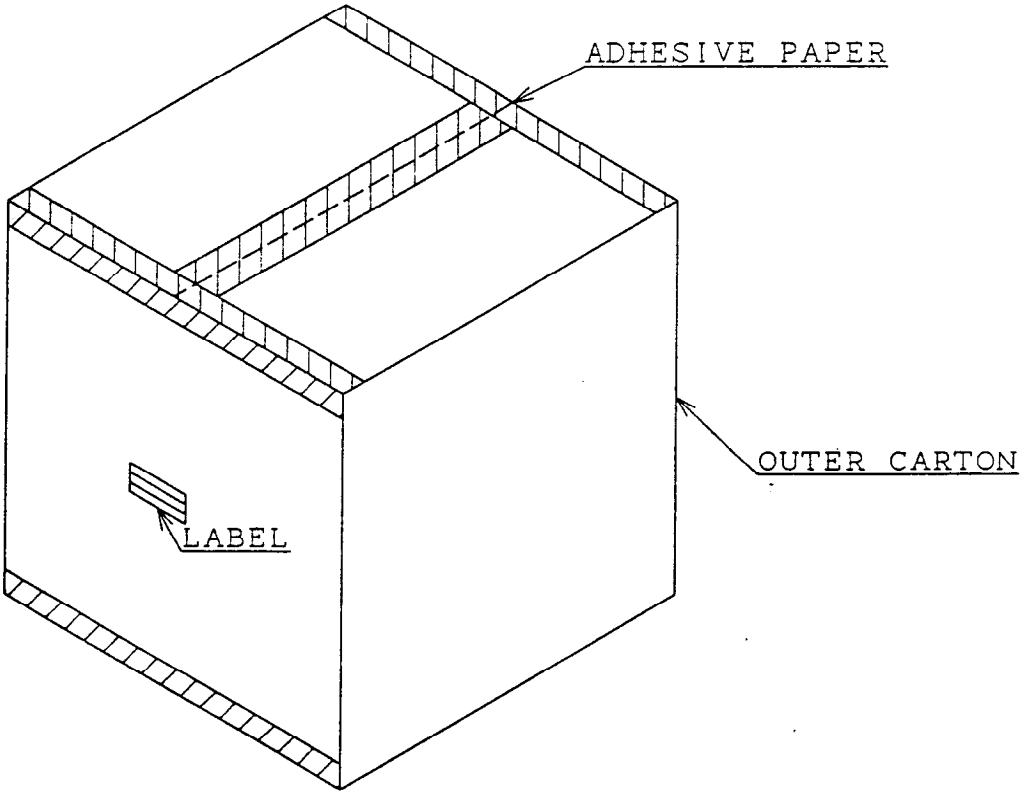


REEL			INNER CARTON			DATE	AUG. 31. 1995		TITLE	REEL AND INNER CARTON OF TCP PACKING
SIZE	A	φ405	SIZE	L	420	UNIT	mm			
	B	φ127		W	420	APROVE	CHECK	DESIGN	DRAWING No.	KPN 023
	C	36		H	50				ASSEMBLY ENGNEERING DEPT.	
MATERIAL	ANTI-STATIC TREATED PLASTIC		MATERIAL	CARDBOARD		M. Kinishi	Y. Honda	T. Kidoguchi	IC GROUP	
									SHARP CORPORATION	



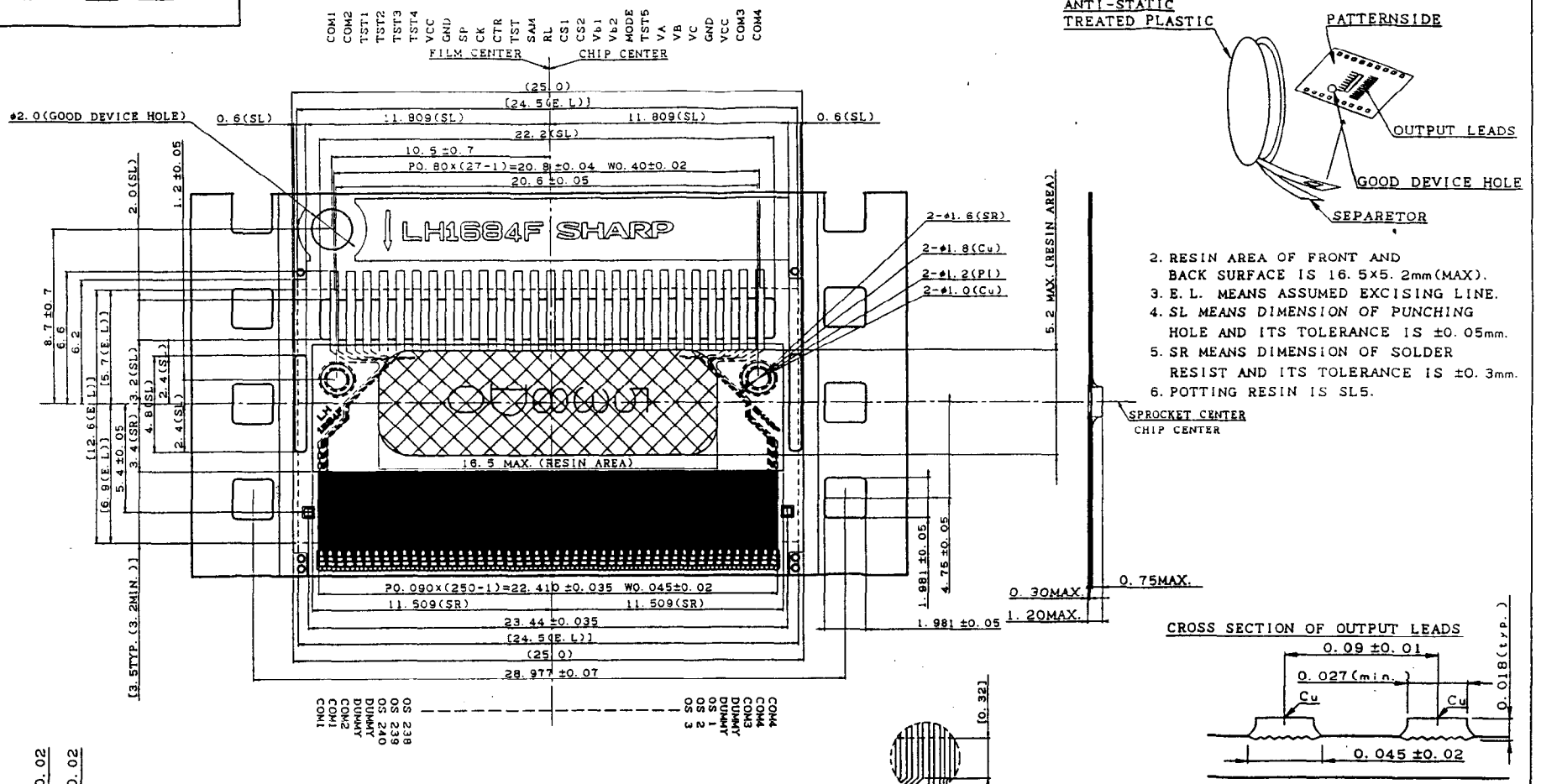
DATE	MARCH 29. 1995					
ITEM		MATERIAL	NUMBER			
ANTI-STATIC TREATED PLASTIC REEL		ANTI-STATIC TREATED PORYSTYLENE	1 REEL			
DESICCANT		SILICA GEL	10g	TITLE	PACKING VIEW OF TCP (1)	
BAG		Al LAMINATED BAG	1PACK			
LABEL		PAPER	3PEACES			
INNER CARTON		CARDBOARD	1CASE			
APROVE	CHECK	DESIGN	ASSEMBLY ENGNEERING DEPT.	CODE		
M. Kanishi	Y. Honda	T. Kidoguchi	IC GROUP	DRAWING No		
			SHARP CORPORATION			





DATE	MARCH 29. 1995					
ITEM	MATERIAL	NUMBER				
OUTER CARTON	CARDBOARD	1CASE				
ADHESIVE TAPE	PAPER					
			TITLE	PACKING VIEW OF TCP (2)		
APROVE	CHECK	DESIGN	ASSEMBLY ENGNEERING DEPT.	CODE		
M. Konishi	Y. Honda	T. Kidoguchi	IC GROUP SHARP CORPORATION	DRAWING No.		

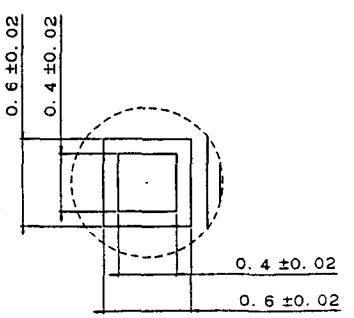
SHARP



NOTES: 1. REEL WINDING

2. RESIN AREA OF FRONT AND BACK SURFACE IS 16.5×5.2mm(MAX).
3. E.L. MEANS ASSUMED EXCISING LINE.
4. SL MEANS DIMENSION OF PUNCHING HOLE AND ITS TOLERANCE IS ±0.05mm.
5. SR MEANS DIMENSION OF SOLDER RESIST AND ITS TOLERANCE IS ±0.3mm.
6. POTTING RESIN IS SL5.

CROSS SECTION OF OUTPUT LEADS



APPLICATION	LH1684F	SCALE 5/1	UNIT mm	DATE / REVISE / CHARGE	
TOLERANCE ±0.05	TAPE FORMAT 35mmWIDE TYPE 4 PERFO-PITCH	TAPE MATERIALS UPILEX S75 ADHESIVE #7100 ED Cu(SLP 1/2oz) SOLDER RESIST	FINISH TIN PLATING	TITLE	OUT LINE DRAWING OF LH1684F
DATE	AUG 28, 1996			CODE	
DESIGN	T. Yasuda	ASSEMBLY ENGINEERING DEPT.			
CHECK	H. Honda	IC FUKUYAMA GROUP		DRAWING NO.	SPN4701-00
APPROVE	M. Kimishi	SHARP CORPORATION			