

Document Title

**128Kx8 Bit High-Speed CMOS Static RAM(3.3V Operating).
Operated at Commercial and Industrial Temperature Ranges.**

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>																			
Rev. 0.0	Initial release with Preliminary.	Aug. 5. 1998	Preliminary																			
Rev. 1.0	Relax DC characteristics.	Sep. 7. 1998	Preliminary																			
	<table><tr><th colspan="2">Item</th><th>Previous</th><th>Changed</th></tr><tr><td rowspan="3">Icc</td><td>12ns</td><td>70mA</td><td>75mA</td></tr><tr><td>15ns</td><td>68mA</td><td>73mA</td></tr><tr><td>20ns</td><td>65mA</td><td>70mA</td></tr></table>	Item		Previous	Changed	Icc	12ns	70mA	75mA	15ns	68mA	73mA	20ns	65mA	70mA							
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Icc	12ns	70mA	75mA																			
	15ns	68mA	73mA																			
	20ns	65mA	70mA																			
Rev. 2.0	Release to Final Data Sheet. 2.1. Delete Preliminary. 2.2. Changed Standby Current.	Mar. 3. 1999	Final																			
	<table><tr><th>Item</th><th>Previous</th><th>Changed</th></tr><tr><td>Standby Current(Isb1)</td><td>0.3mA</td><td>0.5mA</td></tr></table> 2.3. Added Data Retention Characteristics.	Item	Previous	Changed	Standby Current(Isb1)	0.3mA	0.5mA															
Item	Previous	Changed																				
Standby Current(Isb1)	0.3mA	0.5mA																				
Rev. 3.0	Add 10ns part.	Apr. 24. 2000	Final																			
Rev. 3.1	V _{IH} /V _{IL} Change	Oct. 2. 2000	Final																			
	<table><tr><th rowspan="2">Item</th><th colspan="2">Previous</th><th colspan="2">Changed</th></tr><tr><th>Min</th><th>Max</th><th>Min</th><th>Max</th></tr><tr><td>V_{IH}</td><td>2.0</td><td>V_{CC}+0.5</td><td>2.0</td><td>V_{CC}+0.3</td></tr><tr><td>V_{IL}</td><td>-0.5</td><td>0.8</td><td>-0.3</td><td>0.8</td></tr></table>	Item	Previous		Changed		Min	Max	Min	Max	V _{IH}	2.0	V _{CC} +0.5	2.0	V _{CC} +0.3	V _{IL}	-0.5	0.8	-0.3	0.8		
Item	Previous		Changed																			
	Min	Max	Min	Max																		
V _{IH}	2.0	V _{CC} +0.5	2.0	V _{CC} +0.3																		
V _{IL}	-0.5	0.8	-0.3	0.8																		
Rev. 4.0	Delete 20ns speed bin	Sep. 24. 2001	Final																			

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

FEATURES

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 30mA(Max.)
 - (CMOS) : 5mA(Max.)
 - 0.5mA(Max.) L-ver. only
 - Operating K6R1008V1C-10 : 80mA(Max.)
 - K6R1008V1C-12 : 75mA(Max.)
 - K6R1008V1C-15 : 73mA(Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention : L-ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
 - K6R1008V1C-J : 32-SOJ-400
 - K6R1008V1C-T : 32-TSOP2-400CF

The K6R1008V1C is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The K6R1008V1C uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAM-SUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R1008V1C is packaged in a 400mil 32-pin plastic SOJ or TSOP2 forward.

K6R1008V1C-C10/C12/C15	Commercial Temp.
K6R1008V1C-I10/I12/I15	Industrial Temp.

The block diagram illustrates a 512x256 DRAM architecture. It features a central **Memory Array** with 512 Rows and 256x8 Columns. The array is connected to a **Row Select** circuit, which is driven by address inputs A₀ through A₈ via inverters. A **Pre-Charge Circuit** is connected to the top of the memory array. The array is also connected to an **I/O Circuit** with **Column Select** circuitry, which is driven by address inputs A₉ through A₁₆ via inverters. A **Data Cont.** (Data Controller) is connected to the I/O circuit and the memory array. A **CLK Gen.** (Clock Generator) is connected to the data controller and the memory array. The I/O circuit is connected to the system bus (I/O₁~I/O₈). The system bus is also connected to a **CS** (Chip Select) input, a **WE** (Write Enable) input, and a **OE** (Output Enable) input, which are connected to the memory array via inverters.

A0	1		32	A16
A1	2		31	A15
A2	3		30	A14
A3	4		29	A13
$\overline{\text{CS}}$	5		28	$\overline{\text{OE}}$
I/O1	6		27	I/O8
I/O2	7		26	I/O7
V _{CC}	8		25	V _{SS}
V _{SS}	9		24	V _{CC}
I/O3	10		23	I/O6
I/O4	11		22	I/O5
$\overline{\text{WE}}$	12		21	A12
A4	13		20	A11
A5	14		19	A10
A6	15		18	A9
A7	16		17	A8

Pin Name	Pin Function
A ₀ - A ₁₆	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O ₁ ~ I/O ₈	Data Inputs/Outputs
V _{CC}	Power(+3.3V)
V _{SS}	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V _{CC}	-0.5 to 4.6	V
Power Dissipation		P _d	1	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} + 0.3***	V
Input Low Voltage	V _{IL}	-0.3**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.

** V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

*** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS*(T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{CC}		-2	2	μA
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =V _{SS} to V _{CC}		-2	2	μA
Operating Current	I _{CC}	Min. Cycle, 100% Duty $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	10ns	-	80	mA
			12ns	-	75	
			15ns	-	73	
Standby Current	I _{SB}	Min. Cycle, $\overline{CS}=V_{IH}$		-	30	mA
	I _{SB1}	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V	Normal	-	5	mA
			L-ver.	-	0.5	
Output Low Voltage Level	V _{OL}	I _{OL} =8mA		-	0.4	V
Output High Voltage Level	V _{OH}	I _{OH} =-4mA		2.4	-	V

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

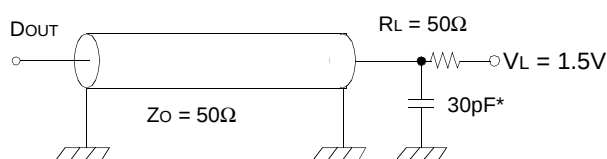
* Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS($T_A=0$ to 70°C , $V_{CC}=3.3\pm0.3\text{V}$, unless otherwise noted.)**TEST CONDITIONS***

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

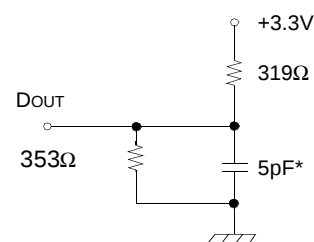
* The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, toW, toLZ & toHZ



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	K6R1008V1C-10		K6R1008V1C-12		K6R1008V1C-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	toLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	toHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	toH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	10	-	12	-	15	ns

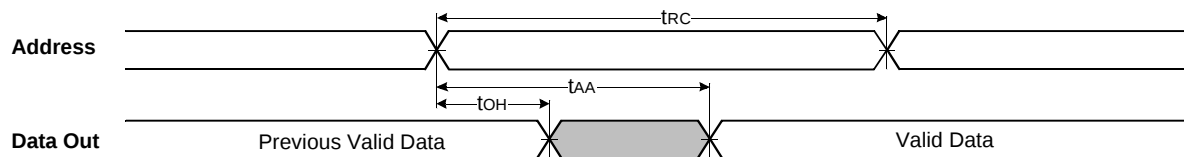
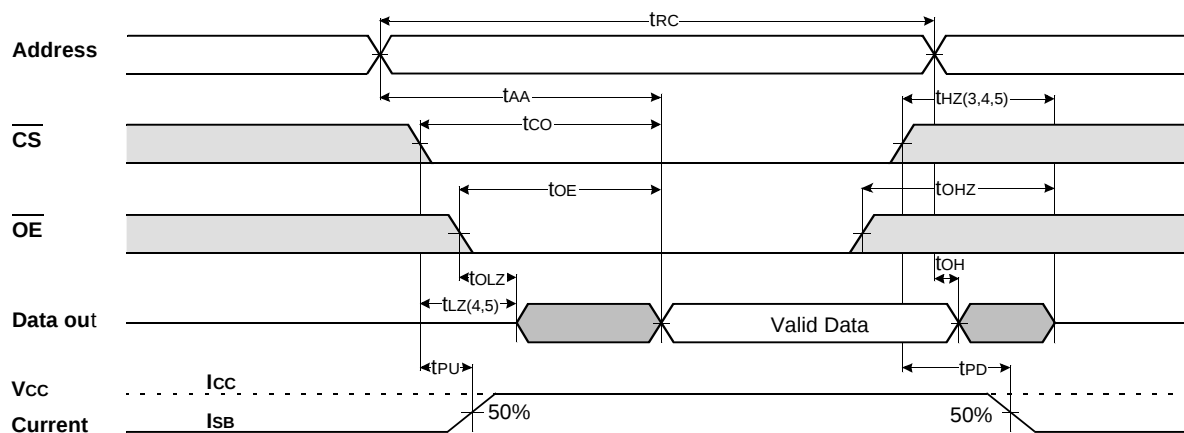
* The above parameters are also guaranteed at industrial temperature range.

WRITE CYCLE*

Parameter	Symbol	K6R1008V1C-10		K6R1008V1C-12		K6R1008V1C-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t _{CW}	7	-	8	-	9	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	7	-	8	-	9	-	ns
Write Pulse Width($\overline{\text{OE}}$ High)	t _{WP}	7	-	8	-	9	-	ns
Write Pulse Width($\overline{\text{OE}}$ Low)	t _{WP1}	10	-	12	-	15	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	5	0	6	0	7	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	ns

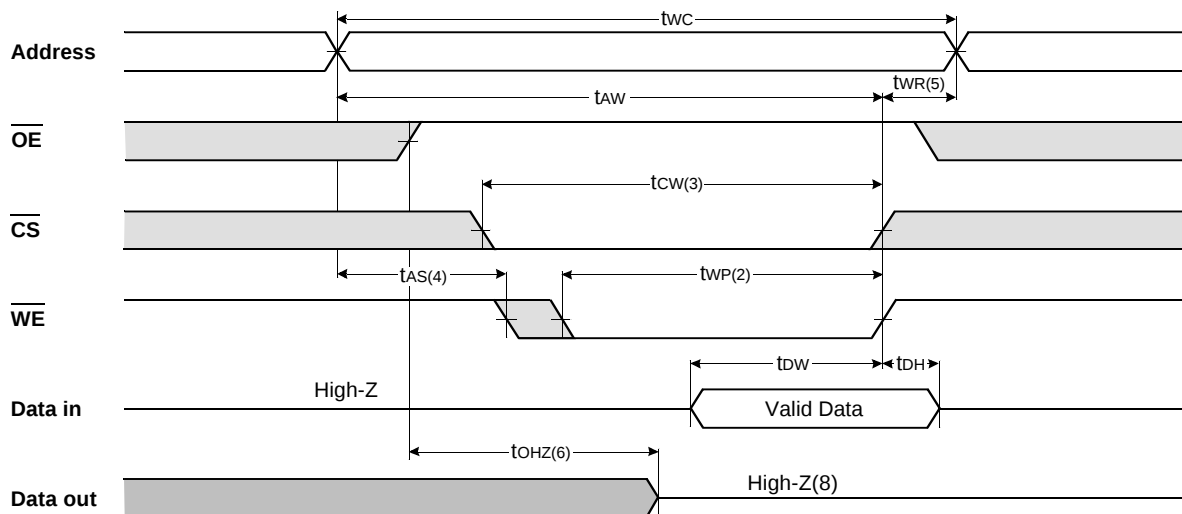
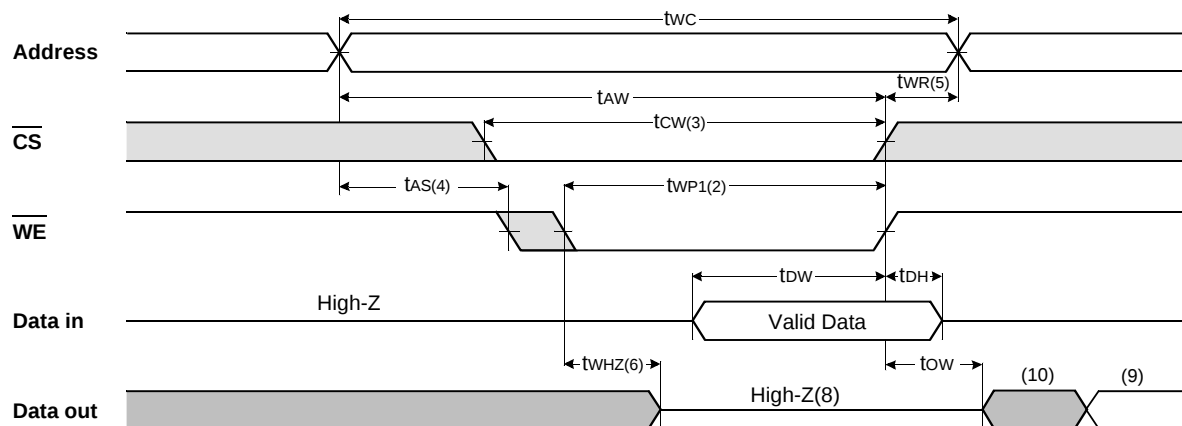
* The above parameters are also guaranteed at industrial temperature range.

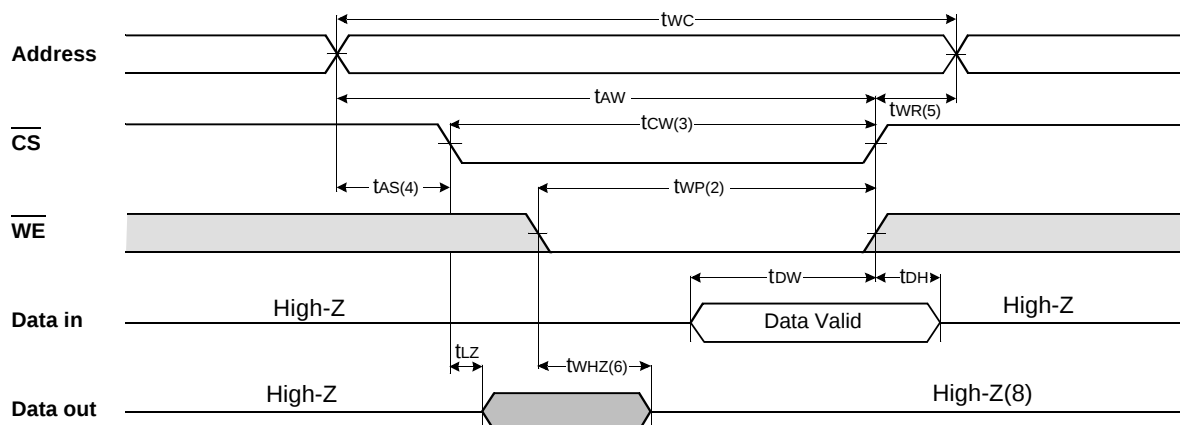
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$, $\overline{\text{WE}}=V_{\text{IH}}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{\text{WE}}=V_{\text{IH}}$)

NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ = Clock)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ =Low Fixed)

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{\text{CS}}$ = Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low ; A write ends at the earliest transition $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{\text{CS}}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.
6. If $\overline{\text{OE}}$, $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
9. DOUT is the read data of the new address.
10. When $\overline{\text{CS}}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB} , I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	DOUT	I_{CC}
L	L	X	Write	DIN	I_{CC}

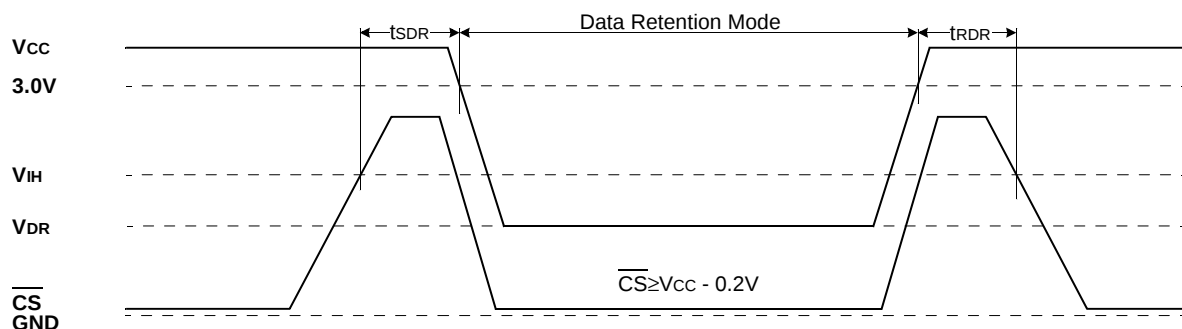
* X means Don't Care.

DATA RETENTION CHARACTERISTICS*($T_A=0$ to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V _{CC} for Data Retention	V _{DR}	$\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$	2.0	-	3.6	V
Data Retention Current	I _{DR}	$V_{\text{CC}}=3.0\text{V}$, $\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	-	-	0.4	mA
		$V_{\text{CC}}=2.0\text{V}$, $\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	-	-	0.3	
Data Retention Set-Up Time	t _{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	t _{RDR}		5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-ver only.

DATA RETENTION WAVE FORM

 $\overline{\text{CS}}$ controlled

CMOS SRAM

Units:millimeters/Inches

