Chrontel

Chrontel CH7301C DVI Transmitter Device

Features

- DVI Transmitter up to 165M pixels/second
- DVI low jitter PLL
- DVI hot plug detection
- Supporting graphics resolutions up to1600 x 1200 pixels
- Providing RGB output
- DAC connection detection
- Programmable power management
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device
- Three 10-bit video DAC outputs
- Offered in a 64-pin LQFP package

General Description

The CH7301C is a display controller device which accepts a digital graphics input signal, and encodes and transmits data through a DVI or DFP (Digital flat panel). The device accepts data over one 12-bit wide variable voltage data port which supports different data formats including RGB and YCrCb.

The DVI processor includes a low jitter PLL for generation of the high frequency serialized clock, and all circuitry required to encode, serialize and transmit data. The CH7301C comes in versions able to drive a DFP display at a pixel rate of up to 165MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device. See Figure 1 for the functional block diagram of the CH7301C.

Color space conversion from YCrCb to RGB is supported in both DVI and VGA bypass modes.
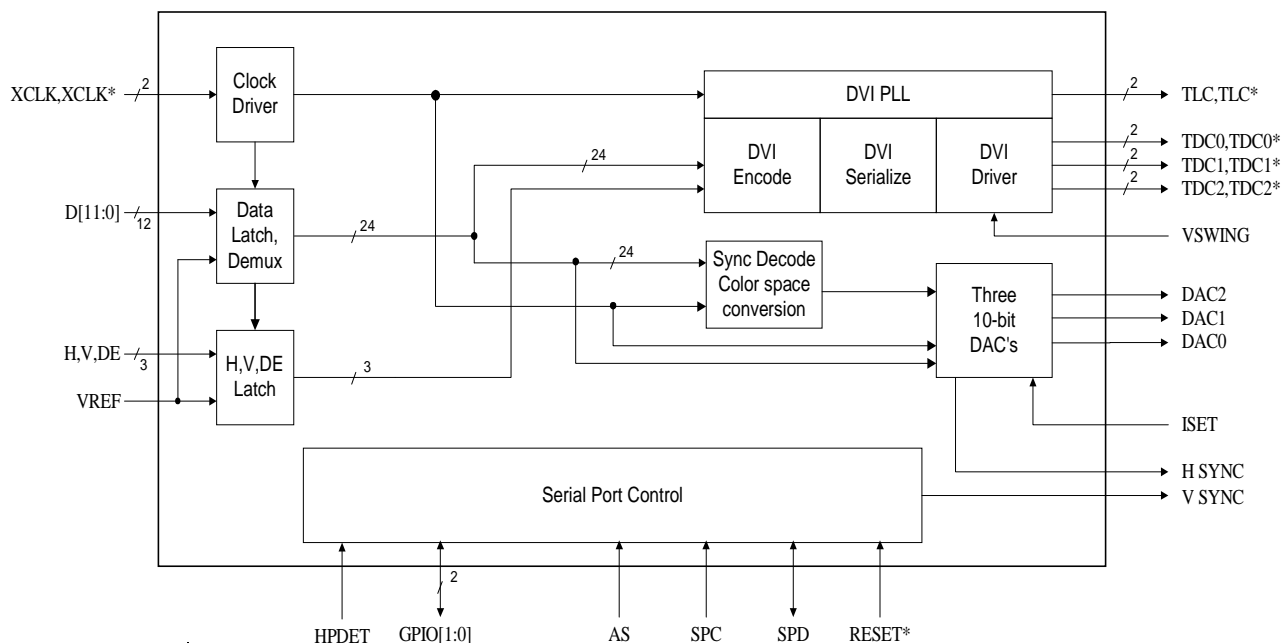

Figure 1. Functional Block Diagram
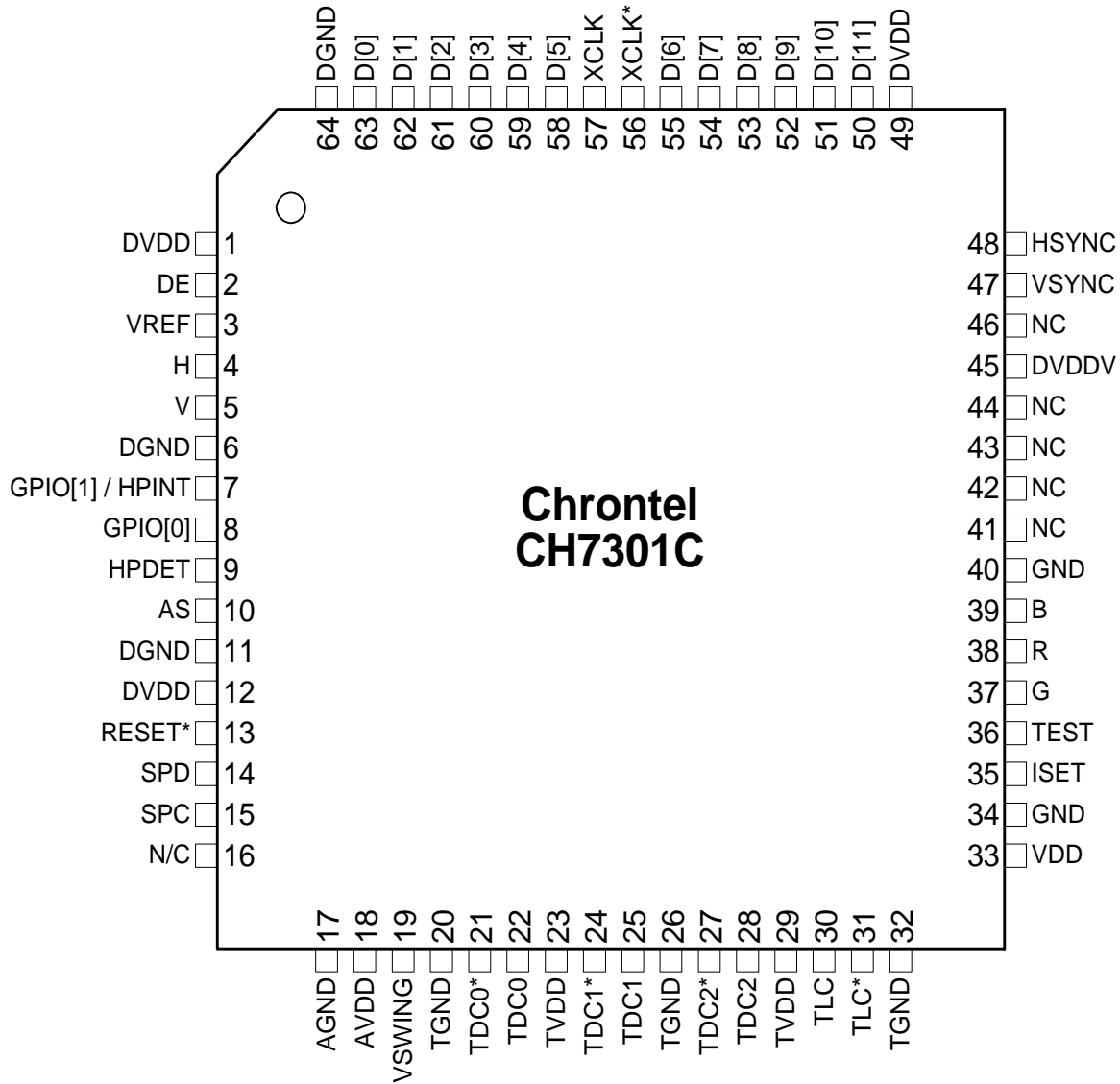
1. PIN DESCRIPTIONS

1.1 Package Diagram

Figure 2. 64-Pin LQFP

1.2 Pin Description

Table 1. Pin Description

64-Pin LQFP	# Pins	Type	Symbol	Description
2	1	In	DE	**Data Enable** This pin accepts a data enable signal which is high when active video data is input to the device, and low all other times. The levels are 0 to DVDDV, and the VREF signal is used as the threshold level. This input is used by the DVI.
3	1	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of DVDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync, data enable and clock inputs.
4	1	In/Out	H	**Horizontal Sync Input / Output** This pin receives / sends out horizontal sync input from / output to the graphics controller.
5	1	In/Out	V	**Vertical Sync Input / Output** This pin receives / sends vertical sync input from / output to the graphics controller.
7	1	In/Out	GPIO[1] / HPINT	**General Purpose Input - Output[1] /** **DVI Detect Output** (Open drain or internal weak pull-up) This pin provides a general purpose I/O controlled via the serial port bus. The internal pull-up will be to the DVDD supply. When the GPIO[1] pin is configured as an input, this pin can be used to output the DVI detect signal (pulls low when a termination change has been detected on the HPDET input). This is an open drain output. The output is released through serial port control.
8	1	In/Out	GPIO[0]	**General Purpose Input - Output[0]** (Open drain or internal weak pull-up) This pin provides a general purpose I/O controlled via the serial port.
9	1	In	HPDET	**Hot Plug Detect** (internal pull-down) This input pin determines whether the DVI is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the HPINT or GPIO[1]/HPINT pin pulling low.
10	1	In	AS	**Address Select** (Internal pull-up) This pin determines the serial port address of the device (1,1,1,0,1,AS*,AS).
13	1	In	RESET*	**Reset * Input** (Internal pull-up) When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
14	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the serial data pin of the serial port interface, and uses the DVDDV supply.

Table 1. Pin Description

64-Pin LQFP	# Pins	Type	Symbol	Description
15	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port interface, and uses the DVDDV supply.
19	1	In	VSWING	**DVI Swing Control** This pin sets the swing level of the DVI outputs. A 2.4K ohm resistor should be connected between this pin and TGND using short and wide traces.
22, 21	2	Out	TDC0, TDC0*	**DVI Data Channel 0 Outputs** These pins provide the DVI differential outputs for data channel 0 (blue).
25, 24	2	Out	TDC1, TDC1*	**DVI Data Channel 1 Outputs** These pins provide the DVI differential outputs for data channel 1 (green).
28, 27	2	Out	TDC2, TDC2*	**DVI Data Channel 2 Outputs** These pins provide the DVI differential outputs for data channel 2 (red).
30, 31	2	Out	TLC, TLC*	**DVI Clock Outputs** These pins provide the differential clock output for the DVI interface corresponding to data on the TDC[0:2] outputs.
35	1	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 140 ohm resistor should be connected between this pin and GND (DAC ground) using short and wide traces.
36	1	In	TEST	**TEST Input** This pin is used for factory test and should be tied to GND or left N/C.
37	1	Out	G	**Green Output** This pin will output the Green component of RGB when RGB bypass mode is used.
38	1	Out	R	**Red Output** This pin will output the Red component of RGB when RGB bypass mode is used.
39	1	Out	B	**Blue Output** This pin will output the Blue component of RGB when RGB bypass mode is used.
16, 41, 42, 43, 44, 46	6		NC	**No Connect**
47	1	Out	VSYNC	**Vertical Sync Output** A buffered version of VGA vertical sync can be acquired from this pin. (Refer to Register 21h, DC register)

Table 1. Pin Description

64-Pin LQFP	# Pins	Type	Symbol	Description
48	1	Out	HSYNC	**Horizontal Sync Output** A buffered version of VGA horizontal sync can be acquired from this pin. (Refer to Register 21h, DC register)
50 – 55, 58 – 63	12	In	D[11] - D[0]	**Data[11] through Data[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to DVDDV, and the VREF signal is used as the threshold level.
57, 56	2	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the CH7301C for use with the H, V, DE and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The output clocks from this pad cell are able to have their polarities reversed under the control of the MCP bit (in register 1Ch).
1, 12, 49	3	Power	DVDD	**Digital Supply Voltage (3.3V)**
6, 11, 64	3	Power	DGND	**Digital Ground**
45	1	Power	DVDDV	**I/O Supply Voltage (1.1V to 3.3V)**
23, 29	2	Power	TVDD	**DVI Transmitter Supply Voltage (3.3V)**
20, 26, 32	3	Power	TGND	**DVI Transmitter Ground**
18	1	Power	AVDD	**PLL Supply Voltage (3.3V)**
17	3	Power	AGND	**PLL Ground**
33	1	Power	VDD	**DAC Supply Voltage (3.3V)**
34, 40	2	Power	GND	**DAC Ground**

2. MODES OF OPERATION

The CH7301C is capable of being operated as a single DVI output link. Descriptions of the single DVI output link operating mode, with a block diagram of the data flow within the device is shown on **Figure 1**.

2.1 RGB Bypass

In RGB Bypass mode, data, sync and clock signals are input to the CH7301C from a graphics device, and bypassed directly to the D/A converters to implment a second CRT DAC function. External sync signals must be supplied from the graphics device. These sync signals are buffered internally, and can be output to drive the CRT. The input data format can be either YCrCb or RGB in this operating mode (See description for register 56h, bit[0]). Input data is 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The CH7301C can support a pixel rate of 165MHz. This operating mode uses all 10 bits of the DAC's 10-bit range, and provides a nominal signal swing of 0.661V (or 0.7V depending on DAC Gain setting in control registers) when driving a 75Ω doubly terminated load. No scaling, scan conversion or flicker filtering is applied in RGB bypass.

2.2 DVI Output

In DVI Output mode, multiplexed input data, sync and clock signals are input to the CH7301C from the graphics controller's digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. Some examples of modes supported are shown in the table below, and a block diagram of the CH7301C is shown on the following page. For the table below, clock frequencies for given modes were taken from VESA DISPLAY MONITOR TIMING SPECIFICATIONS if they were detailed there, not VESA TIMING DEFINITION FOR FLAT PANEL MONITORS. The device is not dependent upon this set of timing specifications. Any values of pixels/line, lines/frame and clock rate are acceptable, as long as the pixel rate remains below 165MHz. For correct DVI operation, the input data format must be selected to be one of the RGB input formats.

Table 2. DVI Outputs

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	Refresh Rate (Hz)	XCLK Frequency (MHz)	DVI Frequency (Mbits)
720x400	4:3	1.35:1.00	<85	<35.5	<355
640x400	8:5	1:1	<85	<31.5	<315
640x480	4:3	1:1	<85	<36	<360
720x480	4:3	9:8	59.94	27	270
720x576	4:3	15:12	50	27	270
800x600	4:3	1:1	<85	<57	<570
1024x768	4:3	1:1	<85	<95	<950
1280x720	16:9	1:1	<85	<110	<1100
1280x768	15:9	1:1	<85	<119	<1190
1280x1024	4:3	1:1	<85	<158	<1580
1366x768	16:9	1:1	<85	<140	<1400
1360x1024	4:3	1:1	<75	<145	<1450
1400x1050	4:3	1:1	<75	<156	<1560
1600x1200	4:3	1:1	<60	<165	<1650
1920x1080[1]	16:9	1:1	<60	<165	<1650

[1]This mode is implemented with reduced blanking.

3. INPUT INTERFACE

Two distinct methods of transferring data to the CH7301C are described. They are:

- Multiplexed data, clock input at 1X pixel rate
- Multiplexed data, clock input at 2X pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7301C is latched with both edges of the clock (also referred to as dual-edge transfer mode or DDR). For the multiplexed data, clock at 2X pixel rate, the data applied to the CH7301C is latched with one edge of the clock (also known as single edge transfer mode or SDR). The polarity of the pixel clock can be reversed under serial port control. In single edge transfer modes, the clock edge used to latch data is programmable. In dual edge transfer modes, the clock edge used to latch the first half of each pixel is programmable.

3.1 Interface Voltage Levels

The graphics controller interface can operate at a variable voltage level controlled by the voltage on the **DVDDV** pin. This should be set to the maximum voltage of the interface (typically 3.3V or adjustable between 1.1 and 1.8V). The VREF pin is the voltage reference for the data, date enable, clock and sync inputs and must be tied to DVDDV/2. This is typically done using a resistor divider.

3.2 Input Clock and Data Timing Diagram

The figure below shows the timing diagram for input data and clocks. The first XCLK/XCLK* waveform represents the input clock for the multiplexed data, clock at 2X pixel rate method. The second XCLK/XCLK* waveform represents the input clock for the multiplexed data, clock at 1X pixel rate method.
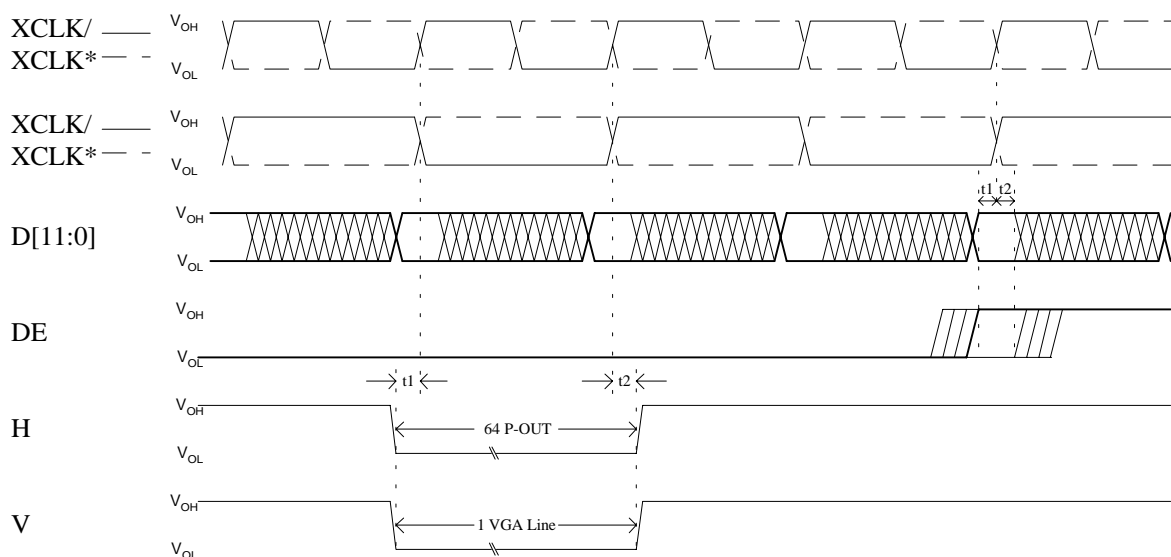
Figure 3. Interface Timing

Table 3. Interface Timing

Symbol	Parameter	Min	Typical	Max	Unit
V_{OH}	Output high level of interface signals	DVDDV - 0.2		DVDDV + 0.2	V
V_{OL}	Output Low level of interface signals	-0.2		0.2	V
t1[1]	D[11:0] & DE to XCLK = XCLK* Delay (setup time)	0.5			ns
t2[1]	XCLK = XCLK* to D[11:0] & DE Delay (hold time)	0.5			ns
DVDDV	Digital I/O Supply Voltage	1.1 – 5%		3.3 + 5%	V

[1] D[11:0], H, V DE times measured when input equals Vref+100mV on rising edges, Vref-100mV on falling edges.

3.3 Input Clock and Data Formats

The 12 data inputs support 5 different multiplexed data formats, each of which can be used with a 1X clock latching data on both clock edges, or a 2X clock latching data with a single edge. The data received by the CH7301C can be used to drive the DVI output, the VGA to TV encoder, or directly drive the DAC's. The multiplexed input data formats are (IDF[2:0]):

IDF   Description

0   12-bit multiplexed RGB input (24-bit color), (multiplex scheme 1)

1   12-bit multiplexed RGB2 input (24-bit color), (multiplex scheme 2)

2   8-bit multiplexed RGB input (16-bit color, 565)

3   8-bit multiplexed RGB input (15-bit color, 555)

4   8-bit multiplexed YCrCb input (24-bit color), (Y, Cr and Cb are multiplexed)

For multiplexed input data formats, either both transitions of the XCLK/XCLK* clock pair, or each rising or falling edge of the clock pair (depending upon MCP bit, rising refers to a rising edge on the XCLK signal, a falling edge on the XCLK* signal) will latch data from the graphics chip. The multiplexed input data formats are shown in the figures below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (eg; P0a and P0b) will contain a complete pixel encoded as shown in the tables 4 ~ 7 below. It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per CCIR-656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in CCIR-656). All non-active pixels should be 0 in RGB formats, and 16 for Y and 128 for CrCb in YCrCb formats.

3.3.1   Data De-skew Feature

The de-skew feature allows adjustment of the input setup and hold time. The input data D[11:0] can be latched slightly before or after the latching edge of XCLK depending on the amount of the de-skew. Note that the XCLK is not changed, only the time at which the data is latch relative to XCLK. .The de-skew is controlled using the XCMD[3:0] bits located in register 1Dh. The delay t_{CD} between clock and data is given by the following formula:

t_{CD} = - XCMD[3:0] * t_{STEP} for $0 \leq$ XCMD[3:0] ≤ 7

t_{CD} = (XCMD[3:0] – 8) * t_{STEP} for $8 \leq$ XCMD[3:0] ≤ 15

where   XCMD is a number between 0 and 15 represented as a binary code
         t_{STEP} is the adjustment increment (See **Table 17**)

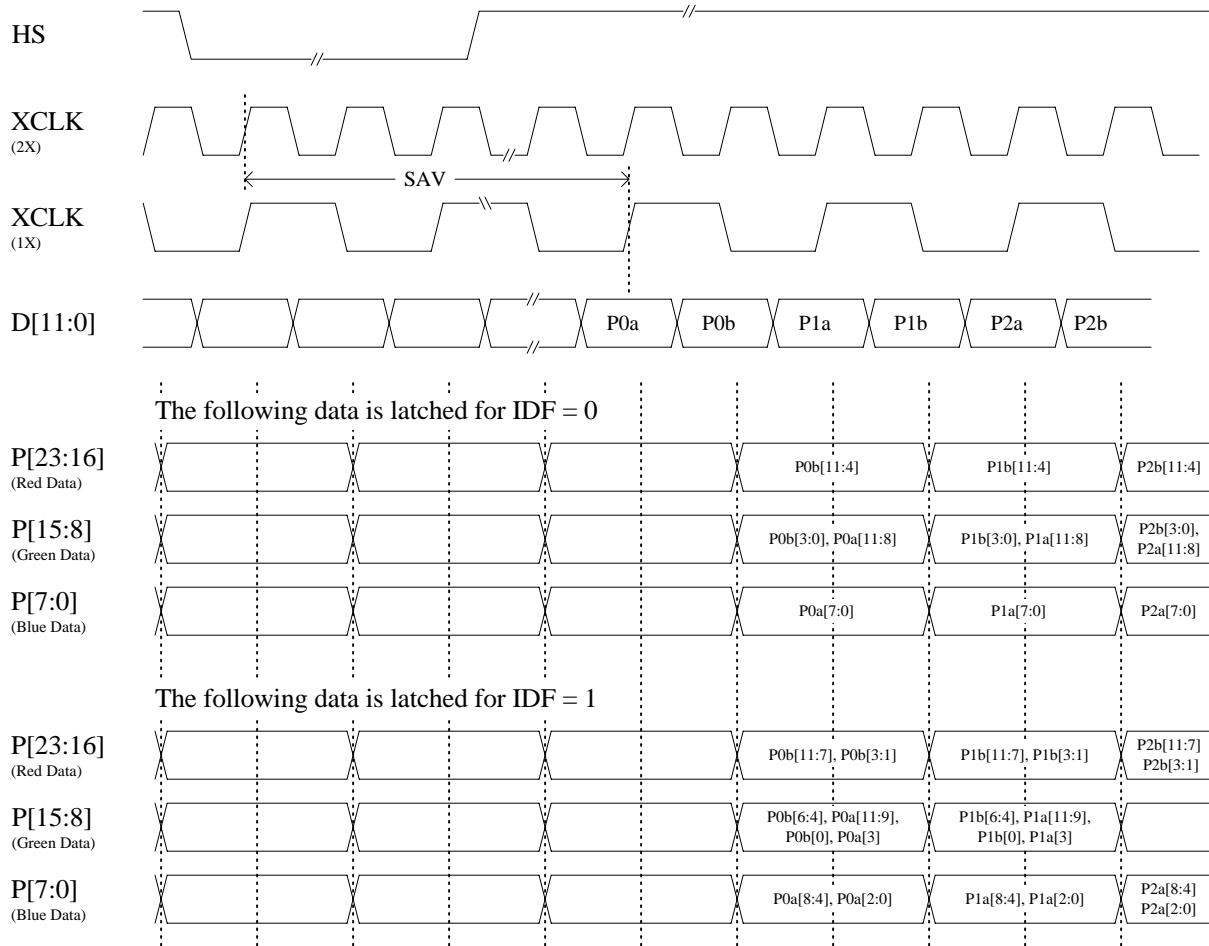The delay is also tabulated in **Table 9**.

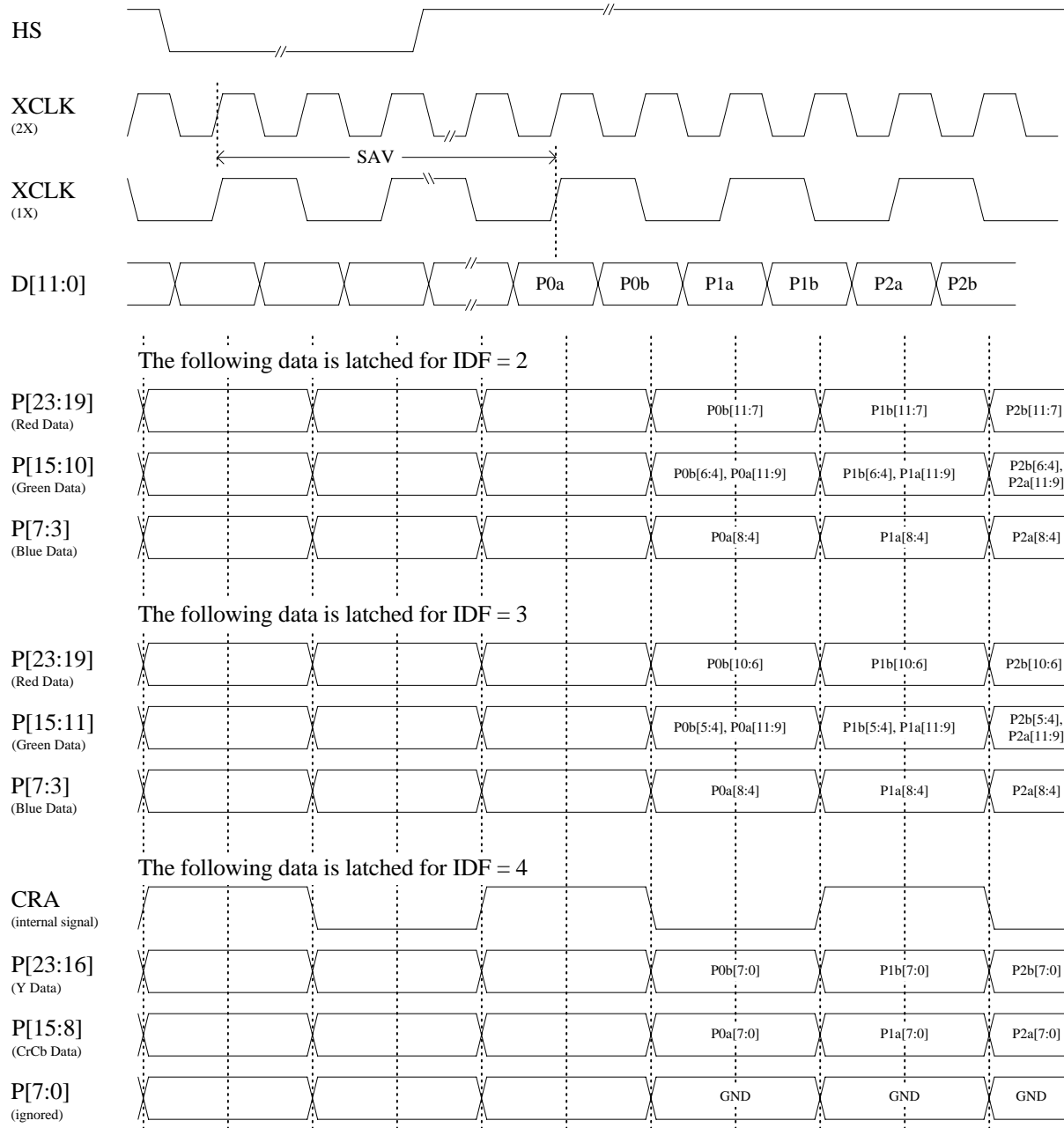**Figure 4. Multiplexed Input Data Formats (IDF = 0, 1)**

Figure 5. Multiplexed Input Data Formats (IDF = 2, 3, 4)

Table 4. Multiplexed Input Data Formats (IDF = 0, 1)

IDF =		0				1			
Format =		12-bit RGB (12-12)				12-bit RGB (12-12)			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	D[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 5. Multiplexed Input Data Formats (IDF = 2, 3)

IDF =		2				3			
Format =		RGB 5-6-5				RGB 5-5-5			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	D[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	D[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	D[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	D[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	D[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	D[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	D[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 6. Multiplexed Input Data Formats (IDF = 4)

IDF =		4							
Format =		YCrCb 8-bit							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	D[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

When IDF = 4 (YCrCb mode), the data inputs can also be used to transmit sync information to the device. In this mode, the embedded sync will follow the VIP2 convention, and the first byte of the 'video timing reference code' will be assumed to occur when a Cb sample would occur, if the video stream was continuous. This is shown below:

Table 7. Embedded Sync

IDF = Format =		4 YCrCb 8-bit							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	Dx[7]	FF	00	00	S[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	Dx[6]	FF	00	00	S[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	Dx[5]	FF	00	00	S[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	Dx[4]	FF	00	00	S[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	Dx[3]	FF	00	00	S[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	Dx[2]	FF	00	00	S[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	Dx[1]	FF	00	00	S[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	Dx[0]	FF	00	00	S[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

In this mode, the S[7..0] byte contains the following data:

S[6]   =   F   =   1 during field 2, 0 during field 1

S[5]   =   V   =   1 during field blanking, 0 elsewhere

S[4]   =   H   =   1 during EAV (synchronization reference at the end of active video)

          0 during SAV (synchronization reference at the start of active video)

Bits S[7] and S[3..0] are ignored.

4. REGISTER CONTROL

The CH7301C is controlled via a serial port. The serial port bus uses only the SPC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device retains all register states.

4.1 Control Registers Map

The controls are listed below, divided into three sections: general controls, input / output controls, DVI controls. A register map and register description follows.

• General Controls

ResetIB	Software serial reset
ResetDB	Software datapath reset
PD[7:0]	Power down controls (DVIP, DVIL, TVD, DACPD[2:0], FDP)
VID[7:0]	Version ID register
DID[7:0]	Device ID register
TSTP[1:0]	Enable/select test pattern generation (color bar, ramp)

• Input/Output Controls

XCM	XCLK 1X, 2X select
XCMD[3:0]	Delay adjust between XCLK and D[11:0]
MCP	XCLK polarity control
IDF[2:0]	Input data format
GPIOL[1:0]	Read or write level for GPIO pins
GOENB[1:0]	Direction control for GPIO pins
SYNCO[1:0]	Enables/selects sync output for RGB and bypass modes
DACG[1:0]	DAC gain control
DACBP	DAC bypass
DES	Decode embedded sync
HSP	H sync polarity control
VSP	V sync polarity control
T_RGB	YCrCb to RGB enable

• DVI Controls

CTL[3:0]	DVI Control Inputs
DVID[2:0]	DVI transmitter drive strength control
DVIP	DVI Power Down Control
DVIL	DVI Power Down Control
DVIT	Hot Plug Detection Pin Level
HPDD	Hot Plug Detection Disable
HPIE	Hot Plug Interrupt Enable on GPIO[1]
HPIR	Hot Plug Interrupt Reset
TPFBD[3:0]	DVI PLL feed back divider
TPCP[1:0]	DVI PLL charge pump trim
TPFFD[1:0]	DVI PLL feed forward divider
TPPSD[1:0]	DVI PLL post scale divider
TPLPF[3:0]	DVI PLL low pass filter
DVII	DVI output invert
TMSYO	DVI Sync Direction

4.2 Registers Read/Write

Regarding the CH7301C registers read/write operation, please see applications note AN-41 for details.

Table 8. Serial Port Register Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Ch	Reserved	Reserved	Reserved	Reserved	Reserved	MCP	Reserved	XCM
1Dh	Reserved	Reserved	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
1Eh	GOENB1	GOENB0	GPIOL1	GPIOL0	HPIR	Reserved	Reserved	Reserved
1Fh	Reserved	DES	Reserved	VSP	HSP	IDF2	IDF1	IDF0
20h	HPIE	Reserved	DVIT	Reserved	DACT2	DACT1	DACT0	SENSE
21h	Reserved	Reserved	Reserved	Reserved	SYNCO0	DACG1	DACG0	DACBP
23h	Reserved	Reserved	Reserved	Reserved	Reserved	HPDD	Reserved	Reserved
31h	TPPD3	TPPD2	TPPD1	TPPD0	CTL3	CTL2	CTL1	CTL0
33h	DVID2	DVID1	DVID0	DVII	TPPSD1	TPPSD0	Reserved	TPCP0
34h	Reserved	Reserved	TPFFD1	TPFFD0	TPFBD3	TPFBD2	TPFBD1	TPFBD0
35h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
36h	TPLPF3	TPLPF2	TPLPF1	TPLPF0	Reserved	Reserved	Reserved	Reserved
37h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48h	Reserved	Reserved	Reserved	ResetIB	ResetDB	Reserved	TSTP1	TSTP0
49h	DVIP	DVIL	Reserved	Reserved	DACPD2	DACPD1	DACPD0	FPD
4Ah	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
4Bh	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
56h	Reserved	Reserved	TMSYO	Reserved	Reserved	Reserved	Reserved	T_RGB

All register bits not defined in the register map are reserved bits, and should be left at the default value.

Clock Mode Register   **Symbol: CM**

                                                           Address: 1Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	MCP	Reserved	XCM
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Bit 0 of register CM signifies the XCLK frequency. A value of '0' is used when the XCLK is at the pixel frequency (duel edge clocking mode) and a value of '1' is used when the XCLK is twice the pixel frequency (single edge clocking mode).

Bit 2 of register CM controls the phase of the XCLK clock input to the CH7301C. A value of '1' inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching input data.

Input Clock Register   **Symbol:**   **IC**

         Address: **1Dh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	1	0	0	0

XCMD[3:0] (bits 3-0) of register IC control the delay applied to the XCLK signal before latching input data D[11:0] per the following table. t_{STEP} is given in **Table 17**.

Table 9. Delay applied to XCLK before latching input data D[11:0]

XCMD3	XCMD2	XCMD1	XCMD0	Adjust phase of Clock relative to Data
0	0	0	0	0 * t_{STEP}, XCLK ahead of Data
0	0	0	1	1 * t_{STEP}, XCLK ahead of Data
0	0	1	0	2 * t_{STEP}, XCLK ahead of Data
0	0	1	1	3 * t_{STEP}, XCLK ahead of Data
0	1	0	0	4 * t_{STEP}, XCLK ahead of Data
0	1	0	1	5 * t_{STEP}, XCLK ahead of Data
0	1	1	0	6 * t_{STEP}, XCLK ahead of Data
0	1	1	1	7 * t_{STEP}, XCLK ahead of Data
1	0	0	0	0 * t_{STEP}, XCLK behind Data
1	0	0	1	1 * t_{STEP}, XCLK behind Data
1	0	1	0	2 * t_{STEP}, XCLK behind Data
1	0	1	1	3 * t_{STEP}, XCLK behind Data
1	1	0	0	4 * t_{STEP}, XCLK behind Data
1	1	0	1	5 * t_{STEP}, XCLK behind Data
1	1	1	0	6 * t_{STEP}, XCLK behind Data
1	1	1	1	7 * t_{STEP}, XCLK behind Data

GPIO Control Register   **Symbol:**   **GPIO**

         Address: **1Eh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	GOENB1	GOENB0	GPIOL1	GPIOL0	HPIR	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	0	0	0	0	0	0

Bit 3 of register GPIO resets the hot plug detection circuitry. A value of '1' causes the CH7301C to release the GPIO[1]/HPINT pin. When a hot plug interrupt is asserted by the CH7301C, the CH7301C driver should read the DVIT bit in register 20h to determine the state of the DVI termination. After having read this, the HPIR bit should be set high to reset the circuit, and then set low again.

Bits 5-4 of register GPIO defines the GPIO Read or Write Data bits [1:0]. When the corresponding GOENB bits (GOENB[1:0]) are '0', the values in GPIOL[1:0] are driven out at the corresponding GPIO pins. When the corresponding GOENB bits are '1', the values in GPIOL[1:0] can be read to determine the level forced into the corresponding GPIO pins.

Bits 7-6 of register GPIO are GPIO Direction Control bits [1:0]. GOENB[1:0] control the direction of the GPIO[1:0] pins. A value of '1' sets the corresponding GPIO pin to an input, and a value of '0' sets the corresponding pin to a non-inverting output. The level at the output depends on the value of the corresponding bit GPIOL[1:0].

Input Data Format Register   **Symbol:**   **IDF**

                                                                  Address: **1Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	DES	Reserved	VSP	HSP	IDF2	IDF1	IDF0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

Bits 2-0 of register IDF select the input data format. See Input Interface on section 3.3 on page 8 for a listing of available formats.

HSP (bit 3) of register IDF controls the horizontal sync polarity. A value of '0' defines the horizontal sync to be active low, and a value of '1' defines the horizontal sync to be active high.

VSP (bit 4) of register IDF controls the vertical sync polarity. A value of '0' defines the vertical sync to be active low, and a value of '1' defines the vertical sync to be active high.

DES (bit 6) of register IDF signifies when the CH7301C is to decode embedded sync signals present in the input data stream instead of using the H and V pins. This feature is only available for input data format #4. A value of '0' selects the H and V pins to be used as the sync inputs, and a value of '1' selects the embedded sync signal.

Connection Detect Register   **Symbol:**   **CD**

                                                                  Address: **20h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HPIE	Reserved	DVIT	Reserved	DACT2	DACT1	DACT0	SENSE
TYPE:	R/W	R/W	R	R/W	R	R	R	R/W
DEFAULT:	0	0	0	0	X	X	X	0

The Connection Detect Register provides a means to determine the status of the DAC outputs and the DVI hot plug detect pin. The status bits, DACT[2:0] correspond to the termination of the three DAC outputs. However, the values

contained in these STATUS BITS ARE NOT VALID until a sensing procedure is performed. Use of this register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits. The detection sequence works as follows:

1) Set the power management register (Register 49h) to enable all DAC's, and set register 21h[0] = '0'.

2) Set the SENSE bit to a 1. This forces a constant output from the DAC's.

3) Reset the SENSE bit to 0. This triggers a comparison between the voltage present on these analog outputs and the reference value. During this step, each of the three status bits corresponding to individual DAC outputs will be set if they are CONNECTED.

4) Read the status bits. The status bits, DACT[2:0] now contain valid information which can be read to determine which outputs are connected to a display monitor. Again, a "1" indicates a valid connection, a "0" indicates an unconnected output.

Bit 5 of register CD can be read at any time to determine the level of the hot plug detection pin (HPDET). When the hot plug detect pin changes state, and the DVI output is selected, the HPINT output pin will be pulled low signifying a change in the DVI termination. At this point, the HPIR bit in register 1Eh should be set high, then low to reset the hot plug detect circuit.

Bit 7 of register CD enables the hot plug interrupt detection signal output from the GPIO[1]/HPINT pin. A value of '1' allows the hot plug detect circuit to pull the GPIO[1]/HPINT pin low when a change of state has taken place on the hot plug detect pin (HPDET). A value of '0' disables the interrupt signal. See also the description of the DVIT bit.

DAC Control Register

Symbol: **DC**

Address: **21h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	SYNCO0	DACG1	DACG0	DACBP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Bit 0 of register DC selects the DAC bypass mode. If the input data format is digital RGB, a value of '1' outputs the incoming data directly at the DAC[2:0] outputs for the VGA-Bypass RGB output. If the input data format is digital YCrCb, bit 0 of register 56h must be set to '1', together with bit 0 of register 21h set to '1', to output the analog RGB from the DACs.

Bits 2-1 of register DC control the DAC gain. DACG1 should be low when the input data format is RGB (IDF = 0-3), and high when the input data format is YCrCb (IDF = 4).

Bits 3 of register DC enables the HSYNC and VSYNC outputs.

Hot Plug Detection Register

Symbol: HPD

Address: 23h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	HPDD	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HPDD (bit 2) of register HPD disables the hardware hot plug detection function. This function (default on) tri-states the DVI outputs when the hot plug detect pin (HPDET) is pulled low in accordance with the DVI specification, revision 1.0. This function is independent of the hot plug interrupt function (HPIE, register 20h, bit 7) controlled via the SPP interface.

HPDD = 0 => hardware hot plug interrupt is enabled

= 1 => hardware hot plug interrupt is disabled

DVI Control Input Register

Symbol: TCTL

Address: 31h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPPD3	TPPD 2	TPPD 1	TPPD 0	CTL3	CTL2	CTL1	CTL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

Bits 3-0 of register TCTL set the DVI control inputs applied to the green and red channels during sync intervals. It is recommended to leave these controls at the default value.

Bits 7-4 of register TCTL control the DVI PLL phase detector. The default value is recommended.

DVI PLL Charge Pump Control Register

Symbol: **TPCP**

Address: **33h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DVID2	DVID1	DVID0	DVII	TPPSD1	TPPSD0	Reserved	TPCP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	0	0	1	0	0

Bit 0 of register TPCP control the DVI PLL charge pump.

Bits 3-2 of register TPCP control the DVI PLL post scale divider. The value should be set as shown in Table 10 depending on the input frequency range.

Bit 4 of register TPCP inverts the DVI outputs. A value of 1 inverts the output. A value of 0 is recommended.

Bits 7-5 of register TPCP control the DVI transmitter output drive level. The value should be set as shown in Table 10.

DVI PLL Divider Register

Symbol: **TPD**

Address: **34h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	TPFFD1	TPFFD0	TPFBD3	TPFBD2	TPFBD1	TPFBD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	1	1	0

Bits 3-0 of register TPD control the DVI PLL feedback divider. The default value is recommended.

Bits 5-4 of register TPD control the DVI PLL feed forward divider. The default value is recommended.

Please see **Table 10** for the default values in terms of the frequency ranges.

DVI PLL Supply Control Register

Symbol: **TPVT**

Address: **35h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	1	0	0	0	0

This register controls the voltage in the DVI PLL, use default settings for this register.

DVI PLL Filter Register

Symbol: **TPF**

Address: **36h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPLPF3	TPLPF2	TPLPF1	TPLPF0	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Bits 3-0 of register TPF are reserved bits, and should be left at the default value.

Bits 7-4 of register TPF control the DVI PLL low pass filter. The default value is recommended.

Please see **Table 10** for the default values in terms of the frequency ranges.

Table 10. The Registers Default Settings In Terms Of The Frequency Ranges

Register		<= 65MHz	> 65MHz
33h	TPCP	08h	06h
34h	TPD	16h	26h
36h	TPF	60h	A0h

DVI Clock Test Register

Symbol: **TCT**

Address: **37h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

This register is used for internal testing. The default value is recommended.

Test Pattern Register   Symbol: **TSTP**

                                                                 Address: **48h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	ResetIB	ResetDB	Reserved	TSTP1	TSTP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	0	0	0

Bits 1-0 of register TSTP control the test pattern generation block. This test pattern can be used for both the DVI output and the display monitor output. The pattern generated is determined by **Table 11** below.

Table 11. Test Pattern Control

TSTP[1:0]	Buffered Clock Output
00	No test pattern – Input data is used
01	Color Bars
1X	Horizontal Luminance Ramp

Bit 3 of register TSTP controls the datapath reset signal. A value of '0' holds the datapath in a reset condition, while a value of '1', places the datapath in normal mode. The datapath is also reset at power on by an internally generated power on reset signal.

Bit 4 of register TSTP controls the serial port reset signal. A value of '0' holds the serial port registers in a reset condition, while a value of '1', places the serial port registers in normal mode. The serial port registers are also reset at power on by an internally generated power on reset signal.

Power Management Register   Symbol: **PM**

                                                                 Address: **49h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DVIP	DVIL	Reserved	Reserved	DACPD2	DACPD1	DACPD0	FPD
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

Register PM controls which circuitry within the CH7301C is operating, according to **Table 12** below.

Table 12. Power Management

49h[7]	49h[6]	56h[0]	21h[0]	49h[3:1]	49h[0]	Operating State	Functional Description
X	X	0	1	000	0	VGA to RGB Bypass On	Input is digital RGB
X	X	1	1	XXX	0	VGA to RGB Bypass On	Input is digital YCrCb
X	X	X	0	XXX	0	VGA to RGB Bypass Off	All DACs off
1	1	X	X	XXX	0	DVI Encode, Serialize, Transmitter, and PLL on	DVI is in normal function
X	X	X	X	XXX	1	Full Power Down	All circuitry is powered down except serial port

Version ID Register

Symbol: **VID**

Address: **4Ah**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	1	0	0	1	0	1	0	1

Register VID is a read only register containing the version ID number of the CH7301C.

Device ID Register

Symbol: **DID**

Address: **4Bh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	1	0	1	1	1

Register DID is a read only register containing the device ID number of the CH7301C.

DVI Sync Polarity Register

Symbol: **DSP**

Address: **56h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	TMSYO	Reserved	Reserved	Reserved	Reserved	T_RGB
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

T_RGB (bit 0) of register DSP enables the YCrCb to RGB color space conversion

    T_RGB   =   0 => Disable YCrCb to RGB conversion

               =   1 => Enable YCrCb to RGB conversion

TMSYO (bit 5) of register DSP determines the polarity of embedded sync for DVI, if 0, flip H, V for DVI.

5. ELECTRICAL SPECIFICATIONS

Table 13: Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All power supplies relative to GND	-0.5		5.0	V
	Input voltage of all digital pins	GND – 0.5		VDD + 0.5	V
T$_{SC}$	Analog output short circuit duration		Indefinite		Sec
T$_{AMB}$	Ambient operating temperature	0		85	°C
T$_{STOR}$	Storage temperature	-65		150	°C
T$_J$	Junction temperature			150	°C
T$_{VPS}$	Vapor phase soldering (1 minute)			220	°C

Note:

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latchup.

Table 14. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	PLL Power Supply Voltage	3.1	3.3	3.6	V
VDD	DAC Power Supply Voltage	3.1	3.3	3.6	V
DVDD, TVDD	Digital Power supply voltage	3.1	3.3	3.6	V
DVDDV	I/O Power supply voltage	1.1	1.8	3.6	V
R$_L$	Output load to DAC outputs		37.5		Ω

Table 15. Electrical Characteristics (Operating Conditions: $T_A = 0^oC$ - 70^oC, VDD = 3.3V ± 5%)

Symbol	Description	Min	Typ	Max	Units
	Video D/A resolution	10	10	10	Bits
	Full scale output current		33.9		mA
	Video level error			10	%
I$_{VDD}$	3 DACs Enabled		100	110	mA
I$_{DVDDV}$	DVDDV (1.8V) current (15pF load)		4		mA
I$_{PD}$	TOTAL		60		mA

Table 16. DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Inputs		0.25			V
V_{DATAIH}	D[0-11] Input High Voltage		Vref+0.25		DVDD+0.5	V
V_{DATAIL}	D[0-11] Input Low Voltage		GND-0.5		Vref-0.25	V
V_{MISCIH}	GPIOx, RESET*, AS, HPDET Input High Voltage	DVDD=3.3V	2.7		VDD + 0.5	V
V_{MISCIL}	GPIOx, RESET*, AS, HPDET Input Low Voltage	DVDD=3.3V	GND-0.5		0.6	V
I_{MISCPU}	Pull Up Current (GPIO, RESET*, AS)	V_{IN} = 0V	0.5		5.0	uA
I_{MISCPD}	Pull Down Current (HPDET)	V_{IN} = 3.3V	0.5		5.0	uA
V_{MISCOH}	GPIOx, VSYNC, HSYNC Output High Voltage	I_{OH} = -0.4mA	DVDD-0.2			V
V_{MISCOL}	GPIOx, VSYNC, HSYNC Output Low Voltage	I_{OL} = 3.2mA			0.2	V

Note:

VDATA - refers to all digital data (D[11:0]), clock (XCLK, XCLK*), sync (H, V) and DE inputs. VMISC - refers to GPIOx, RESET*, AS and HPDET inputs and GPIOx, VSYNC and HSYNC outputs.

Table 17. AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
f_{XCLK}	Input (XCLK) frequency		25		165	MHz
t_{PIXEL}	Pixel time period		6.06		40	ns
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{XJIT}	XCLK clock jitter tolerance			2		ns
t_{DVIR}	DVI Output Rise Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{DVIF}	DVI Output Fall Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{SKDIFF}	DVI Output intra-pair skew	f_{XCLK} = 165MHz			90	ps
t_{SKCC}	DVI Output inter-pair skew	f_{XCLK} = 165MHz			1.2	ns
t_{DVIJIT}	DVI Output Clock Jitter	f_{XCLK} = 165MHz			150	ps
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	XCLK = XCLK* to D[11:0], H, V, DE = Vref	0.50			ns
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	D[11:0], H, V, DE = Vref to XCLK = XCLK*	0.50			ns
t_R	H and V (when configured as outputs) Output Rise Time (20% - 80%)	15pF load VDDV = 3.3V			1.50	ns
t_F	H and V (when configured as outputs) Output Fall Time (20% - 80%)	15pF load VDDV = 3.3V			1.50	ns
t_{STEP}	De-skew time increment		50		80	ps

5.1 Timing Information

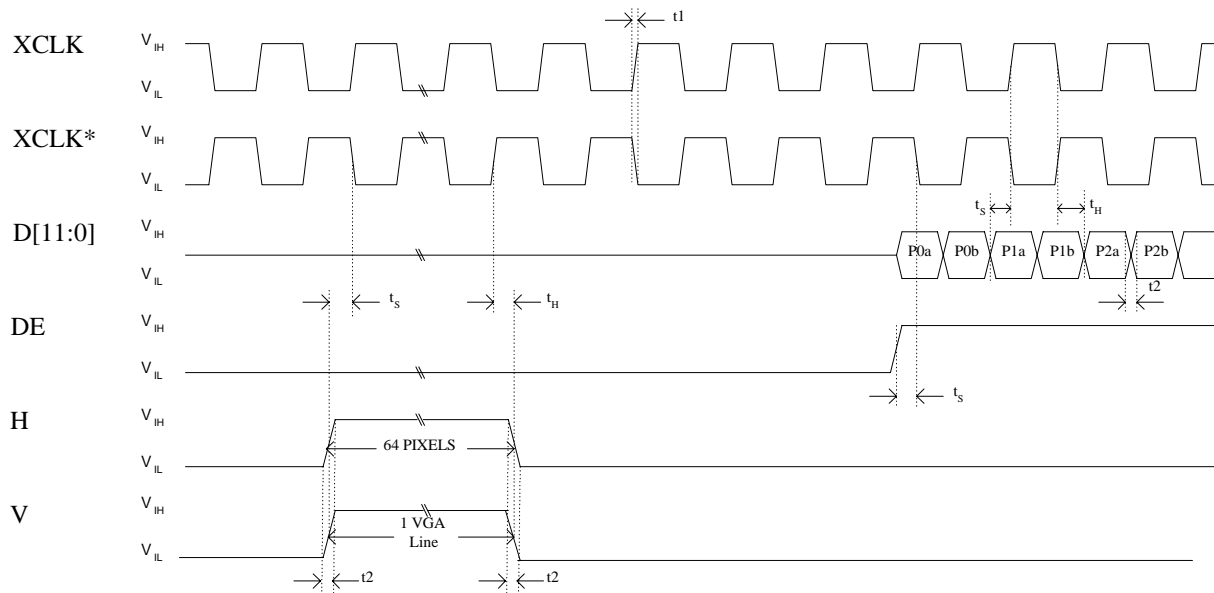### 5.1.1   Clock - Slave, Sync - Slave Mode

Figure 6: Timing for Clock - Slave, Sync - Slave Mode

Table 18: Timing for Clock - Slave, Sync - Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*		See **Table 17**		
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*		See **Table 17**		
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0], H, V & DE rise/fall time w/ 15pF load		1		ns

6. REVISION HISTORY

Rev. #	Date	Section	Description
1.0	03/07/03	All	First official release of CH7301C datasheet, rev. 1.0
1.1	09/08/03	Table 2	Edited Table 2 for DVI output resolutions
1.2	9/18/03	Figure 1	Added 'Color space conversion and sync decode' block.
		56h	Added register 56h, bit 0 for YCrCb to RGB color space conversion.
		56h	Added bit 5 for DVI embedded sync polarity control

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ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH7301C-T	LQFP	64	3.3V

Chrontel

**2210 O'Toole Avenue, Suite 100,
San Jose, CA 95131-1326
Tel: (408) 383-9328
Fax: (408) 383-9338
www.chrontel.com
E-mail: sales@chrontel.com**