Product Brief

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ZORAN®

Benefits Overview

Zoran's Frame-It-1 Video Deinterlacer is a silicon-efficient, high-performance Intellectual Property Core for video IC designs requiring progressive video output. Frame-It-1 is based on Zoran's extensive experience delivering high quality, high volume video ICs to major consumer products manufacturers worldwide. Frame-It-1 employs a robust motion detection and an intelligent interpolation algorithm in a easily implemented, fully synchronous design. 3:2 pulldown, 2:2 pulldown, and bad edit detection enable superior deinterlacing of source material orginally from film.

Proven in silicon, the Frame-It-1 Video Deinterlacer greatly reduces the risk and time involved when integrating the video deinterlacing

function into an IC. Expensive, discrete components can be eliminated from system designs. Frame-It-1 is designed into Zoran's Vaddis™ family of DVD decoders, which are in mass production and are used in brand name consumer products worldwide.

VIP-II Demonstration System

The VIP-II is an FPGA demonstration system for Zoran's IP Core products. The VIP-II accepts composite video, S-video and component video inputs and with its user friendly GUI, enables customers to thoroughly evaluate the performance of Zoran's IP Core products.

Features

- "I to P" converter
- Converts interlaced video to progressive output video
- Robust motion detection based algorithm
- Weaves still areas of the image
- Advanced interpolation for moving areas of the image
- 3:2 and 2:2 pulldown detection for film modes

- Bad edit detection
- Silicon efficient design
- Requires only a single clock input from 20 to 30 MHz
- Fully synchronous design
- Process technology independent "softcore"

Integrated Circuit Applications
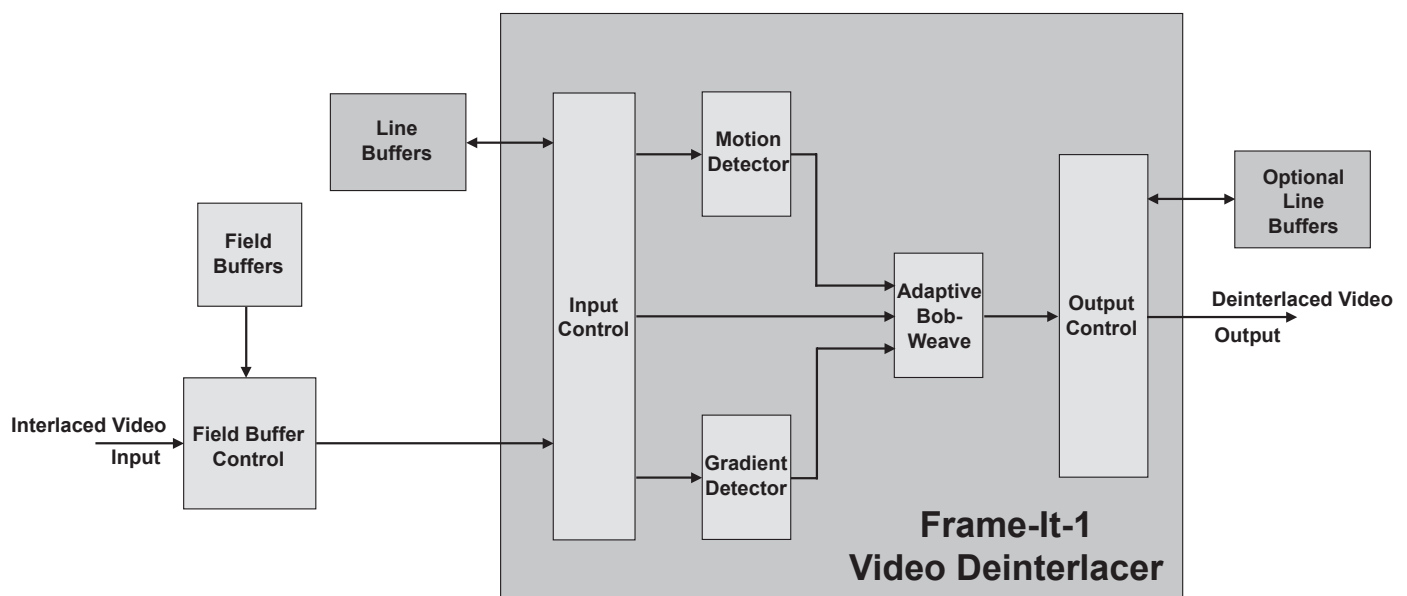
- LCD controllers
- LCD-TV
- PDP-TV

- Projector TV Systems
- Progressive output CRT-TV
- Any IC requiring progressive video output

Deliverables

- Compilable Verilog source code
- Bit-accurate, cycle-accurate C++ model
- Synopsis synthesis scripts

- Test input files
- Documentation
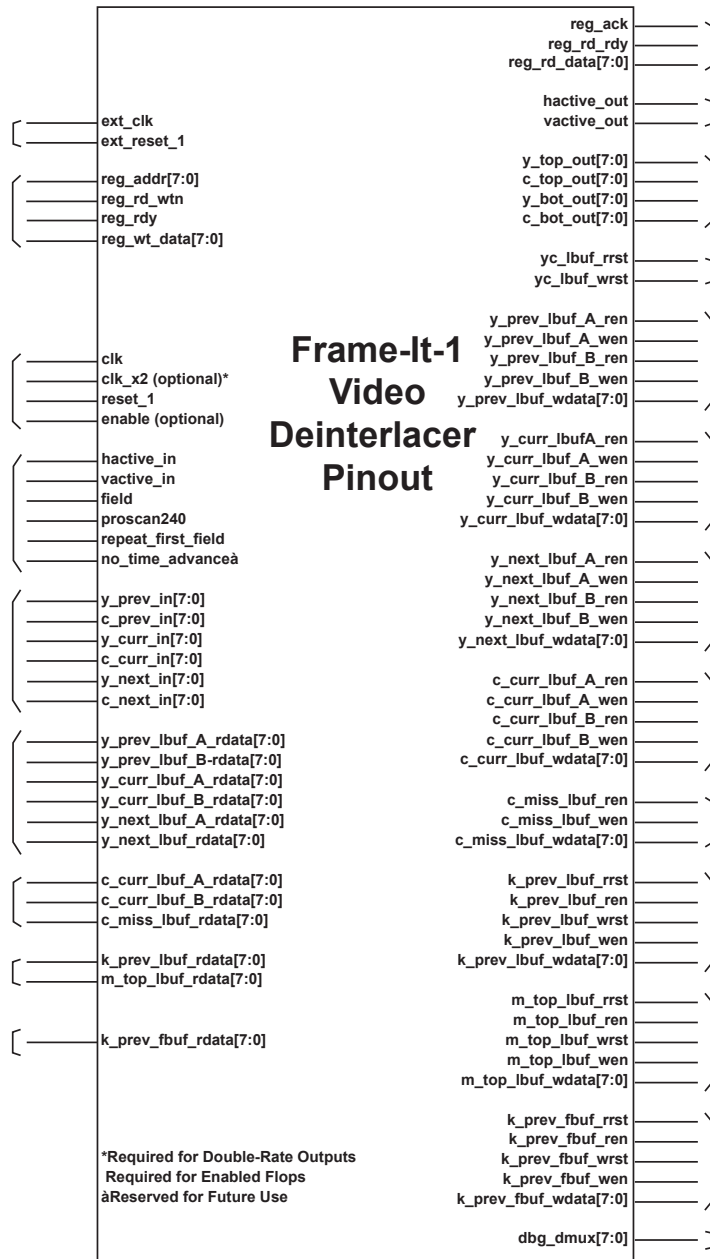- VIP-II FPGA demonstration system available

Frame-It-1 Video Deinterlacer Block Diagram

Video Deinterlacer

Product Brief

Frame-It-1 Video Deinterlacer Logical Pinout

Frame-It-1 Video Deinterlacer Pinout

Inputs:
- ext_clk
- ext_reset_1
- reg_addr[7:0]
- reg_rd_wtn
- reg_rdy
- reg_wt_data[7:0]
- clk
- clk_x2 (optional)*
- reset_1
- enable (optional)
- hactive_in
- vactive_in
- field
- proscan240
- repeat_first_field
- no_time_advanceà
- y_prev_in[7:0]
- c_prev_in[7:0]
- y_curr_in[7:0]
- c_curr_in[7:0]
- y_next_in[7:0]
- c_next_in[7:0]
- y_prev_lbuf_A_rdata[7:0]
- y_prev_lbuf_B-rdata[7:0]
- y_curr_lbuf_A_rdata[7:0]
- y_curr_lbuf_B_rdata[7:0]
- y_next_lbuf_A_rdata[7:0]
- y_next_lbuf_rdata[7:0]
- c_curr_lbuf_A_rdata[7:0]
- c_curr_lbuf_B_rdata[7:0]
- c_miss_lbuf_rdata[7:0]
- k_prev_lbuf_rdata[7:0]
- m_top_lbuf_rdata[7:0]
- k_prev_fbuf_rdata[7:0]

Outputs:
- reg_ack
- reg_rd_rdy
- reg_rd_data[7:0]
- hactive_out
- vactive_out
- y_top_out[7:0]
- c_top_out[7:0]
- y_bot_out[7:0]
- c_bot_out[7:0]
- yc_lbuf_rrst
- yc_lbuf_wrst
- y_prev_lbuf_A_ren
- y_prev_lbuf_A_wen
- y_prev_lbuf_B_ren
- y_prev_lbuf_B_wen
- y_prev_lbuf_wdata[7:0]
- y_curr_lbufA_ren
- y_curr_lbuf_A_wen
- y_curr_lbuf_B_ren
- y_curr_lbuf_B_wen
- y_curr_lbuf_wdata[7:0]
- y_next_lbuf_A_ren
- y_next_lbuf_A_wen
- y_next_lbuf_B_ren
- y_next_lbuf_B_wen
- y_next_lbuf_wdata[7:0]
- c_curr_lbuf_A_ren
- c_curr_lbuf_A_wen
- c_curr_lbuf_B_ren
- c_curr_lbuf_B_wen
- c_curr_lbuf_wdata[7:0]
- c_miss_lbuf_ren
- c_miss_lbuf_wen
- c_miss_lbuf_wdata[7:0]
- k_prev_lbuf_rrst
- k_prev_lbuf_ren
- k_prev_lbuf_wrst
- k_prev_lbuf_wen
- k_prev_lbuf_wdata[7:0]
- m_top_lbuf_rrst
- m_top_lbuf_ren
- m_top_lbuf_wrst
- m_top_lbuf_wen
- m_top_lbuf_wdata[7:0]
- k_prev_fbuf_rrst
- k_prev_fbuf_ren
- k_prev_fbuf_wrst
- k_prev_fbuf_wen
- k_prev_fbuf_wdata[7:0]
- dbg_dmux[7:0]

*Required for Double-Rate Outputs
 Required for Enabled Flops
àReserved for Future Use

For more information, contact Zoran's Sunnyvale office or the office nearest you:

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