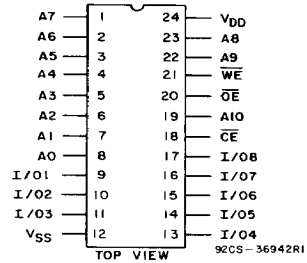
CDM6116AC/3

High-Reliability CMOS 2048-Word by 8-Bit LSI Static RAM

Features:
- *Fully static operation*
- *Single power supply: 4.5 to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *3-state outputs*
- *Industry standard 24-pin configuration*
- *Chip-enable gates address buffers for minimum standby current*
- *Tested to meet the electrical, mechanical and environmental /3 screening*



TERMINAL ASSIGNMENT
24-Lead Dual-In-Line Ceramic Package

Package Specifications

See Section 11, Fig. 6, b1

The RCA-CDM6116AC/3 is a CMOS 2048-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data inputs and data outputs and utilizes a single power supply of 4.5 to 5.5 V. A chip-enable input and an output-enable input are provided for memory expansion and output buffer control.

The chip enable (CE) gates the address and output buffers and powers down the chip to the low power standby mode. The output enable ($\overline{OE}$) controls the output buffers to eliminate bus contention.

The CDM6116AC/3 has an operating temperature range of -55° to +125°C.

The CDM6116AC/3 is supplied in a 24-lead dual-in-line side-brazed ceramic package (D suffix) and in a 28-terminal leadless chip carrier ceramic package (J suffix).

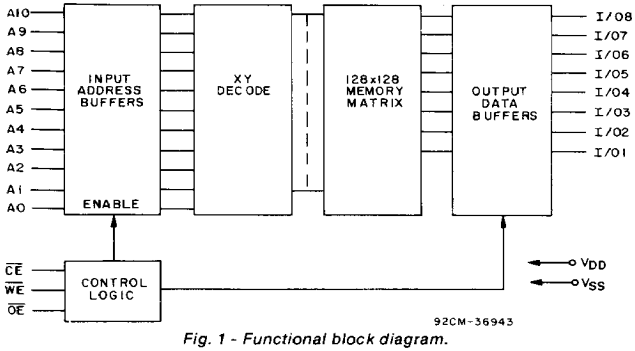


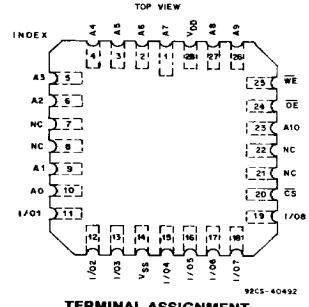
Fig. 1 - Functional block diagram.

	25/-55°C	+125°C
Access Time (max.)	150 ns	185 ns
Output Enable Time (max.)	60 ns	80 ns
Operating Temperature	-55° to +125°C	
Operating Current (max.)	45 mA	45 mA
Standby Current: TTL Level	1.7 mA	2 mA
CMOS Level	50 μA	500 μA

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 TO A10	MODE	I/01 TO I/08	DEVICE CURRENT
H	X	X	X	NOT SELECTED	HIGH Z	STANDBY
L	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	L	STABLE	WRITE	DATA IN	ACTIVE
L	L	L	STABLE	WRITE	DATA IN	ACTIVE

L = LOW H = HIGH X = H or L



TERMINAL ASSIGNMENT
28-Terminal Leadless Chip Carrier Package

Package Specifications

See Section 11, Fig. 39, c1

MAXIMUM RATINGS, *Absolute-Maximum Ratings*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(Voltage referenced to V_{SS} terminal) ..... -0.3 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.3 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C ..... 500 mW
For T_A = +100°C to +125°C ..... Derate linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE FOR D TYPE PACKAGE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS ALL TYPES		UNITS
		MIN.	MAX.	
DC Operating Voltage Range		4.5	5.5	V
Input Voltage Range	V_{IH}	2.2	V_{DD} + 0.3	
	V_{IL}	-0.3	0.8	

STATIC ELECTRICAL CHARACTERISTICS at T_A=-55°C to +125°C, V_{DD}=5 V ± 10%, except where noted

CHARACTERISTIC		TEST CONDITIONS	LIMITS +25/-55°C		LIMITS +125°C		UNITS
			Min.	Max.	Min.	Max.	
Standby Device Current	I_{DDS}	$\overline{CE}$ = V_{IH}, V_{IH} = 2.2 V, V_{IL} = 0.8 V	—	1.7	—	2	mA
	I_{DDS1}	$\overline{CE}$ = 5.5 V, V_{IH} = 5.5 V, V_{IL} = 0 V	—	50	—	500	µA
Output Voltage Low Level	V_{OL} Max.	I_{OL} = 2.1 mA	—	0.4	—	0.4	V
Output Voltage High Level	V_{OH} Min.	I_{OH} = -1 mA	2.4	—	2.4	—	
Input Leakage Current	I_{IN} Max.	V_{DD} = 5 V, V_{IN} = 0 V to V_{DD}	—	±1	—	±2	µA
3-State Output Leakage Current	I_{OUT}	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{DD}	—	±1	—	±2	
Operating Device Current	I_{OPER}#	V_{IN} = V_{IL}, V_{IH}, f = 1 MHz, (Where V_{IL} = 0.8 V, V_{IH} = 2.2 V)	—	45	—	45	mA

#Outputs open circuited.

SIGNAL DESCRIPTIONS

A0-A10 (Address Inputs): These inputs must be stable prior to a write operation, but may change asynchronously during read operations.
I/01-I/08: 8-bit tri-state data bus.
$\overline{CE}$ (Chip Enable): Powers down chip, disables Read and Write functions, and gates off address inputs.
$\overline{OE}$ (Output Enable): Enables tri-state outputs if $\overline{CE}$ is low and $\overline{WE}$ is high.
$\overline{WE}$ (Write Enable): Enables Write function, if $\overline{CE}$ is low. $\overline{WE}$ will dominate if both $\overline{WE}$ and $\overline{OE}$ are low (i.e., the bus will be tri-stated and a Write will occur).
V_{DD}, V_{SS}: Power supply connections.

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DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -55°C to +125°C, V_{DD} = 5 V ± 10%, Input $t_r, t_f \leq$ 10 ns; C_L = 50 pF, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC		LIMITS				UNITS
		+25°C/-55°C		+125°C		
Read Cycle Times, See Fig. 2		**Min.†**	**Max.**	**Min.†**	**Max.**	
Read Cycle Time	t_{RC}	150	—	185	—	ns
Address Access Time	t_{AA}	—	150*	—	185*	
Chip Enable Access Time	t_{ACE}	—	150*	—	185*	
Chip Enable to Output Active	t_{CX}	15	—	15	—	
Output Enable to Output Valid	t_{OEV}	—	60*	—	80*	
Output Enable to Output Active	t_{OEX}	15	—	15	—	
Chip Disable to Output "High Z"	t_{CHZ}	—	60	—	80	
Output Disable to Output "High Z"	t_{OHZ}	—	60	—	80	
Output Hold from Address Change	t_{OH}	15	—	15	—	

†Time required by a limit device to allow for the indicated function.
*Indicates 100% testing. Other parameters do not represent 100% testing.

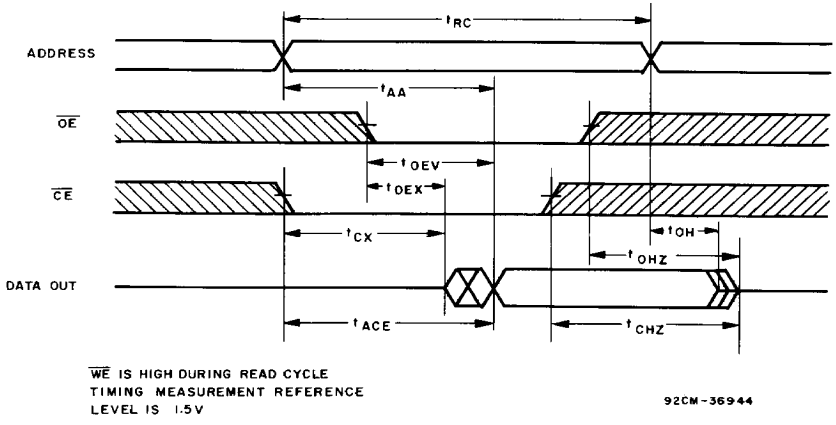


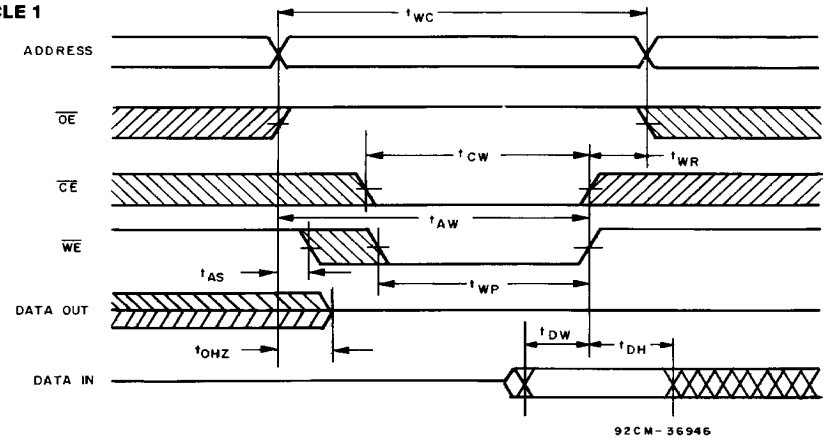
Fig. 2 - Read-cycle timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -55°C to +125°C, V_{DD} = 5 V ± 10%, Input $t_r, t_f \leq$ 10 ns; C_L = 50 pF, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC		LIMITS				UNITS
		+25°C/-55°C		+125°C		
Write Cycle Times, See Fig. 3		**Min.†**	**Max.**	**Min.†**	**Max.**	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable to End of WRITE	t_{CW}	90*	—	120*	—	
Address Valid to End of WRITE	t_{AW}	90*	—	120*	—	
Address Setup Time	t_{AS}	0*	—	0*	—	
Write Pulse Width	t_{WP}	90*	—	120*	—	
Write Recovery Time	t_{WR}	10	—	10	—	
Output Disable to Output "High Z"	t_{OHZ}	—	60	—	80	
Write to Output "High Z"	t_{WHZ}	—	60	—	80	
Input Data Setup Time	t_{DW}	50*	—	80*	—	
Input Data Hold Time	t_{DH}	5*	—	10*	—	
Output Active from End of Write	t_{OW}	10	—	10	—	

†Time required by a limit device to allow for the indicated function.
*Indicates 100% testing. Other parameters do not represent 100% testing.

WRITE CYCLE 1



WRITE CYCLE 2 - $\overline{OE}$ = LOW

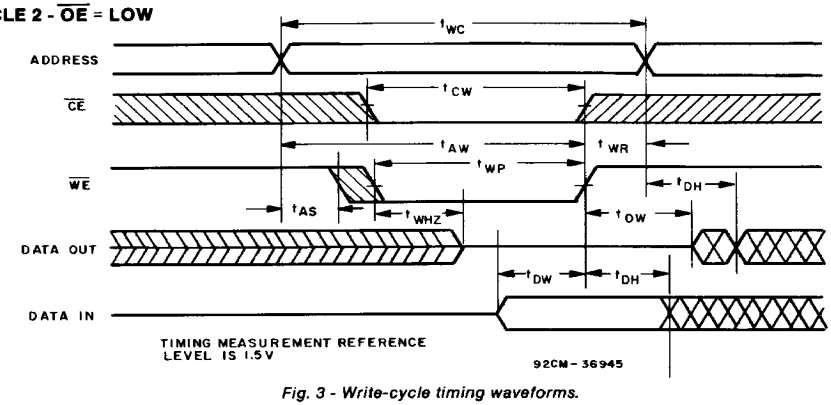


Fig. 3 - Write-cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at T_A = -55° C to +125° C

CHARACTERISTIC (See Fig. 4)		TEST CONDITIONS	LIMITS +25° C/-55° C Min.	LIMITS +25° C/-55° C Max.	LIMITS +125° C Min.	LIMITS +125° C Max.	UNITS
Data Retention Voltage	V_{DR}	$\overline{CE} \geq V_{DD}$ - 0.2 V	2	—	2	—	V
Data Retention Quiescent Current	$I_{DD}DR$	V_{DD} = 3 V, $\overline{CE} \geq$ 2.8 V	—	20	—	250	µA
Chip Disable to Data Retention Time	t_{CDR}	See Fig. 4	10	—	10	—	ns
Recovery to Normal Operation Time	t_R	See Fig. 4	*t_{RC}	—	*t_{RC}	—	ns

*t_{RC} = Read Cycle Time.
Power Down Time = 500 ms

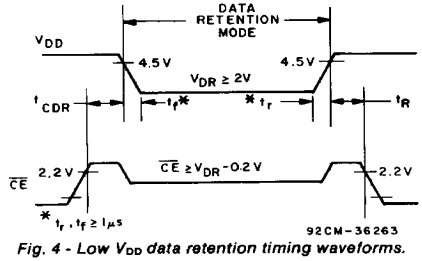


Fig. 4 - Low V_{DD} data retention timing waveforms.

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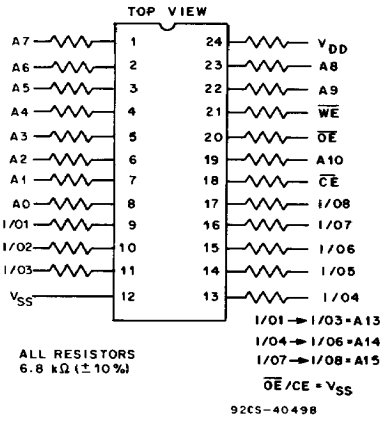
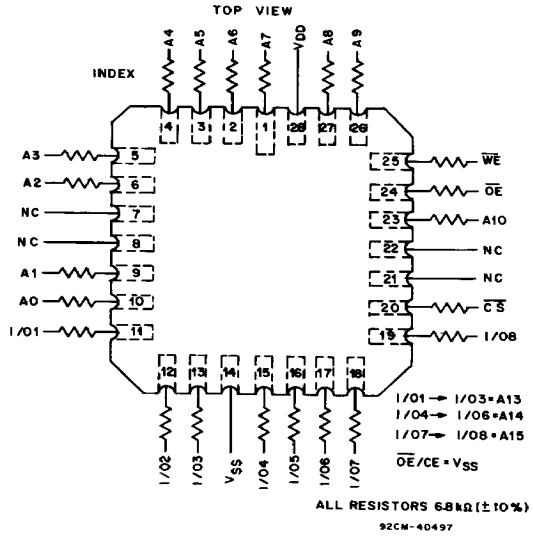
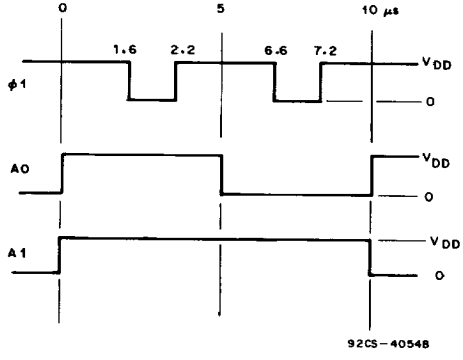


(a) Burn-in circuit for 24-lead D package.



(b) Burn-in circuit from 28-terminal leadless chip-carrier, (LCC), J package.



(c) Burn-in circuits timing waveforms.

TYPE NO.	V_{DD}	TEMP.	TIME
CDM6116ACD/3 CDM6116ACJ/3	7 V	+125°C	160 Hrs., Min.

Fig. 5 - Dynamic burn-in circuits and timing waveforms.