

# **Tone Ringer**

# S2561/S2561A

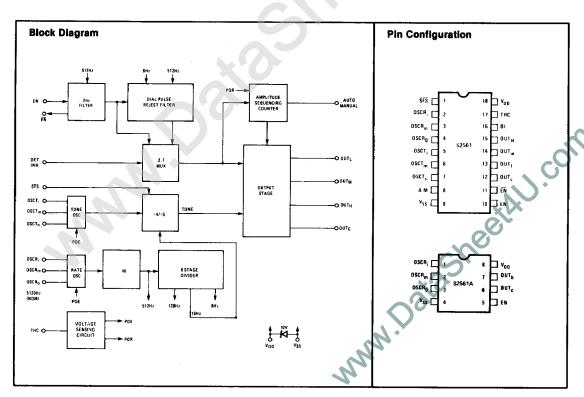
#### **Features**

- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased **Power Output**
- □ 50mW Output Drive Capability at 10V Operating Voltage

- Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- □ Single Frequency Tone Capability

#### General Description

The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.







#### **Absolute Maximum Ratings:**

Supply Voltage	+ 12.0V*
Operating Temperature Range	
Storage Temperature Range	
Voltage at any Pin	V <sub>SS</sub> 0.3V to V <sub>DD</sub> + 0.3V
Lead Temperature (Soldering, 10sec)	300°C

#### **Electrical Characteristics:**

Specifications apply over the operating temperature and 3.5V ≤ V<sub>DD</sub> to V<sub>SS</sub> <12.0V unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions	
V <sub>DS</sub>	Operating Voltage (V <sub>DD</sub> to V <sub>SS</sub> )	8.0	12.0	٧	Ringing, THC pin open	
V <sub>DS</sub>	Operating Voltage	4.2		٧	"Auto" mode, non-ringing	
1 <sub>DS</sub>	Operating Current		500	μΑ	Non-ringing, $V_{DD} = 10V$ , THC pin open, DI pin open or $V_{SS}$	
ОНС	Output Drive Output Source Current (OUT <sub>H</sub> , OUT <sub>C</sub> outputs)	5		mA	$V_{DD} = 10V, V_{OUT} = 8.75V$	
OLC	Output Sink Current (OUT <sub>H</sub> , OUT <sub>C</sub> outputs)	5		mA	$V_{DD} = 10V, V_{OUT} = 0.75V$	
Гонм	Output Source Current (Out <sub>M</sub> output)	2		mA	$V_{DD} = 10V$ , $V_{OUT} = 8.75V$	
IDLM	Output Sink Current (OUT <sub>M</sub> output)	2		mA	$V_{DD} = 10V, V_{OUT} = 0.75V$	
IOHL	Output Source Current (OUT <sub>L</sub> output)	1		mA	$V_{DD} = 10V, V_{OUT} = 8.75V$	
IDLL	Output Sink Current (OUT <sub>L</sub> output)	1		mA	$V_{DD} = 10V, V_{OUT} = 0.75V$	
	CMOS te CMOS					
V <sub>IH</sub>	Input Logic "1" Level	0.7 V <sub>DD</sub>	$V_{DD} + 0.3$	٧	All inputs	
V <sub>IL</sub> .	Input Logic "0" Level	V <sub>SS</sub> - 0.3	0.3 V <sub>DD</sub>	٧	All inputs	
V <sub>OHR</sub>	Output Logic "1" Level (Rate output)	0.9 V <sub>DD</sub>		٧	l <sub>0</sub> = 10μA (Source)	
V <sub>OLR</sub>	Output Logic "O" Level (Rate output)		0.5	٧	$I_0 = 10\mu A \text{ (Sink)}$	
V <sub>OZ</sub>	Output Leakage Current (OUT <sub>H</sub> . OUT <sub>M</sub> outputs in high impedance state)		1	μA μA	$V_{DD} = 10V$ , $V_{OUT} = 0V$ $V_{DD} = 10V$ , $V_{OUT} = 10V$	
CIN	Input Capacitance		7.5	pF	Any pin	
Δfo/fo	Oscillator Frequency Deviation	-5	+5	%	Fixed RC component values $1MQ \le R_{fi}$ , $R_{ti} \le 5MQ$ ; $100kQ \le R_{fm}$ , $R_{tm} \le 750kQ$ ; $150pF \le C_{fo}$ , $C_{to} \le 3000pF$ ; $330pF$ recommended value of $C_{fo}$ and $C_{to}$ , supply voltage varied from $9V \pm 2V$ (over temperature and unit-unit variations)	
R <sub>LOAD</sub>	Output Load Impedance Connected Across OUT <sub>H</sub> and OUT <sub>C</sub>	600		Q	Tone Frequency Range = 300Hz to 3400Hz	
կլլ, կլ	Leakage Current, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>		100	nA	Any input, except DI pin $V_{DD} = 10V$	
ν <sub>τΗ</sub>	POE Threshold Voltage	6.5	8	٧		
٧ <sub>z</sub>	Internal Zener Voltage	11	13	٧	1 <sub>Z</sub> = 5mA	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ( $V_{SS} \le v_1 \le V_{DD}$  as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

<sup>\*</sup>This device incorporates a 12V internal zener diode across the VDD to VSS pins. Do NOT connect a low impedance power supply directly across the device unless the supply voltage can be maintained below 12V or current limited to <25mA.



#### **Functional Description**

The S2561 is a CMOS device capable of simulating the effects of the telephone bell. This is achieved by producing a tone that shifts between two predetermined frequencies (512 and 640Hz) with a frequency ratio of 5:4 at a 16Hz rate.

Tone Generation: The output tone is derived from a tone oscillator that uses a 3 pin R-C oscillator design consisting of one capacitor and two resistors. The oscillator frequency is divided alternately by 4 or 5 at the shift rate. Thus, with the oscillator adjusted for 5120Hz, a tone signal is produced that alternates between 512Hz and 640Hz at the shift rate. The shift rate is derived from another 3 pin R-C oscillator which is adjusted for a nominal frequency of 5120Hz. It is divided down to 16Hz which is used to produce the shift in the tone frequency. It should be noted that in the special case where both oscillators are adjusted for 5120Hz, it is only necessary to have one external R-C network for one oscillator with the other oscillator driven from it. The oscillators are designed such that for fixed R-C component values an accuracy of ±5% can be obtained over the operating supply voltage, temperature and unit-unit variations. See Table 2 for component and frequency selections. In the single frequency mode, activated by connecting the SFS input to V<sub>SS</sub> only the higher frequency continuous tone is produced by using a fixed divider ratio of 4 and by disabling the shift operation.

Ring Signal Detection: In the following description it is assumed that both the tone and rate oscillators are adjusted for a frequency of 5120Hz. Ringing signal (nominally 42 to 105 VAC, 20Hz, 2 sec on/4 sec off duty cycle) applied by the central office between the telephone line pair is capacitively coupled to the tone ringer circuitry as shown in Figure 2. Power for the device is derived from the ringing signal itself by rectification (diodes D1 thru D4) and zener diode clamping (Z2). The signal is also applied to the EN input after limiting and clamping by a resistor (R2) and internal diodes to VDD and VSS supplies. Internally the signal is first squared up and then processed thru a 2ms filter followed by a dial pulse reject filter. The 2ns filter is a two-stage register clocked by a 512Hz signal derived from the rate oscillator by a divide by 10 circuit. The squared ring signal (typically a square wave) is applied to the D input of the first stage and also to reset inputs of both stages. This provides for rejection of spurious noise spikes. Signals exceeding a duration of 2ms only can pass through the filter.

The dial pulse reject filter is clocked at 8Hz derived from the rate oscillator by divide by 640 circuit. This circuit is designed to pass any signal that has at least two transitions in a given 125ms time period. This insures that signals below 8Hz will be rejected with certainty. Signals over 16Hz will be passed with certainty and between 8Hz and 16Hz there is a region of uncertainty. By adjusting the rate oscillator to a different frequency the break points of 10Hz and 20Hz the rate oscillator can be adjusted to 6400Hz. Of course this also increases the tone shift rate to 20Hz. The action of the dial pulse reject filter minimizes the dial pulse interference during dialing although it does not completely eliminate it due to the rather large region of uncertainty associated with this type of discrimination circuitry. The dial pulse filter also has the characteristic that an input signal is not detected unless its duration exceeds 125ms. This insures that the tone ringer will not respond to momentary bursts of ringing less than 125 milliseconds in duration (Ref. 1).

In logic interface applications, the 2ms filter and the dial pulse reject filter can be inhibited by wiring the Det. INHIBIT pin to  $V_{DD}$ . This allows the tone ringer to be enabled by a logic '1' level applied at the "ENABLE" input without the necessity of a 20Hz ring signal.

Voltage Sensing: The S2561 contains a voltage sensing circuit that enables the output stage and the rate and tone oscillators, only when the supply voltage exceeds a predetermined value. Typical value of this threshold is 7.3 volts. This prduces two benefits. First, it insures that the audible intensity of the output tone is fairly constant throughout the ringing period; and secondly, it insures proper circuit operation during the "auto" mode operation by reducing the power consumption to a minimum when the supply voltage drops below 7.3 volts. This extends the supply voltage decay time beyond 4 seconds (off period of the ring signal) with an adequate filter capacitor and insures the proper functioning of the "amplitude sequencing" counter. It is important to note that the operating supply voltage should be well above the threshold value during the ringing period and that the filter capacitor should be large enough so that the ripple on the supply voltage does not fall below the threshold value. A supply voltage of 10 to 12 volts is recommended.

In applications where the tone ringer is continuously powered and below the threshold level, the internal threshold can be bypassed by connecting the THC pin to  $V_{DD}$ . The internal threshold can also be reduced by





connecting an external zener diode between the THC and  $\ensuremath{V_{DD}}$  pins.

**Auto Mode:** In the "auto" mode, activated by wiring the "auto/manual" input to  $V_{SS}$ , an amplitude sequencing of the output tone can be achieved. Resistors  $R_L$  and  $R_M$  are inserted in series with the  $Out_L$  and  $Out_M$  outputs, respectively, and paralleled with the  $Out_H$  output (Figure 1). Load is connected across  $Out_H$  and  $Out_C$  pins.  $R_L$  is chosen to be higher than  $R_M$ . In this manner the first ring is of the lowest amplitude, second ring is of medium amplitude and the third and consecutive

Figure 1-A. Output Stage Connected for Auto Mode Operation

EN OUTL RL

OUTH RN

OUTH RL

OUTH RL

AUTO. "R3"

EN OUTH

TONE

TONE

TONE

TONE

TONE

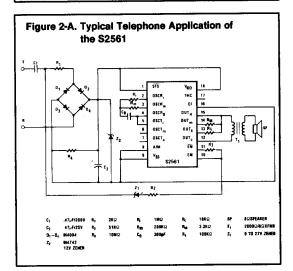
TONE

TONE

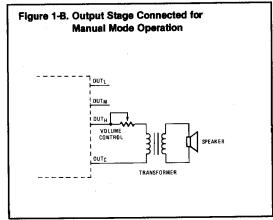
TONE

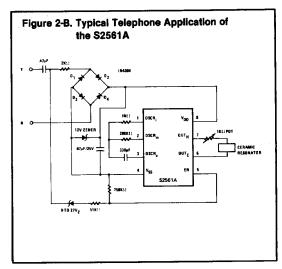
TONE

TRANSFORMER



rings thereafter are at maximum amplitude. For the proper functioning of the "amplitude sequencing" counter the device must have at least 4.2 volts across it throughout the ring sequence. The filter capacitor is so chosen that the supply voltage will not drop below 4.0 volts during the off period. At the end of a ring sequence when the off period substantially exceeds the 4 second duration, the counter will be reset. This will insure that the amplitude sequencing will start correctly beginning a new ring sequence. The counter is held in reset during the "manual" mode operation. This produces a maximum ring amplitude at all times.







Output Stage: The output stage is of push-pull type consisting of buffers L, M, H and C. The load is connected across pins  $\operatorname{Out}_H$  and  $\operatorname{Out}_C$  (Figure 2). During ringing, the  $\operatorname{Out}_H$  and  $\operatorname{Out}_C$  outputs are out of phase with each other and pulse at the tone rate. During a non-ringing state, all outputs are forced to a known level such as ground which insures that there is no DC component in the load. Thus, direct coupling can be used for driving the load. The major benefit of the push-pull arrangement is increased power output. Four times as much power can be delivered to the load for the same operating voltage. Buffers M and H are three-state. In the "auto" mode buffer M is active only during the second

ring and in the "high impedance" state at all other times. Buffer H is active beginning the third ring. In the "manual" mode buffers H, L and C are active at all times while buffer M is in a high impedance state. The output buffers are so designed that they can source or sink 5mA at a V<sub>DD</sub> of 10 volts without appreciable voltage drop. Care has been taken to make them symmetrical in both source and sink configurations. Diode clamping is provided on all outputs to limit the voltage spikes associated with transformer drive in both directions V<sub>DD</sub> and V<sub>SS</sub>.

Normal protection circuits are present on all inputs.

Table 1. S2561 (S2561A) Pin/Function Descriptions

Pin	Number	Function			
Power (V <sub>DD</sub> *, V <sub>SS</sub> *)	18, 9 (8, 4)	These are the power supply pins. The device is designed to operate over the range of 3.5 to 12.0 volts. A range of 10 to 12 volts is recommend for the telephone application.			
Ring Enable (EN*, EN)	10, 11, (5)	These pins are for the 20Hz ring enable input. They can also be used for DC level enabling by wiring the DI pin to V <sub>DD</sub> . EN is available for the S2561 only.			
Auto/Manual (A/M)	8	''Auto'' mode for amplitude sequencing is implemented by wiring this pin to $V_{SS}$ . ''Manual'' mode results when connected to $V_{DD}$ . The amplitude sequencing counter is held in reset during the ''manual'' mode.			
Outputs (Out <sub>L</sub> , Out <sub>M</sub> , Out <sub>H</sub> , Out <sub>C</sub> )	13, 14, 15, (7, 6)	These are the push-pull outputs. Load is directly connected across $\operatorname{Out}_H$ and $\operatorname{Out}_C$ outputs. In the ''auto'' mode, resistors $R_L$ and $R_M$ can be inserted in series with the $\operatorname{Out}_L$ and $\operatorname{Out}_M$ outputs for amplitude sequencing (see Figure 1).			
Oscillators Rate Oscillator (OSCRi, OSCRm, OSCRo)	2, 3, 4, (1, 2, 3)	These pins are provided to connect external resistors RRi, RRm and capacitor CR <sub>0</sub> to form an R-C oscillator with a nominal frequency of 5120Hz. See Table 2 for components selection.			
<b>Tone Oscillator</b> (OSCT <sub>i</sub> , OSCT <sub>m</sub> , OSCT <sub>o</sub> )	5, 6, 7	These pins are provided to connect external resistors RT <sub>i</sub> , RT <sub>m</sub> and capacitor $\text{CT}_0$ to form an R-C oscillator from which the tone signal is derived. With the oscillator adjusted to 512Hz and 640Hz results. See Table 2 for components selection.			
Threshold Control (THC)	17	The internal threshold voltage is brought out to this pin for modification in non-telephone applications. It should be left open for telephone applications. For power supplies less than 9V connect to $V_{DD}$ .			





Table 1. (Continued)

Pin	Number	Function
Detector Inhibit (DI)	16	When this pin is connected to $V_{DD}$ , the dial pulse reject filter is disabled to allow DC level enabling of the tone ringer. This pin should be hardwired to $V_{SS}$ in normal telephone-type applications.
Single Frequency Select (SFS)	1	When this pin is connected to $V_{SS}$ , only a single frequency continuous tone is produced as long as the tone ringer is enabled. In normal applications this pin should be hardwired to $V_{DD}$ .

<sup>\*</sup>Pinouts of 8 pin S2561A package.

Table 2. Selection Chart for Oscillator Components and Output Frequencies

Tone/Rate Oscillator Frequency (Hz)		Oscillator Components	1		
	R <sub>I</sub> (kΩ)	R <sub>M</sub> (kΩ)	C <sub>O</sub> (pF)	Rate (Hz)	Tone (Hz)
5120	1000	200	330	16	512/640
6400				20	640/800
3200	Select compor	nents in the ranges ind	icated in the	10	320/400
8000		of electrical characteris	25	800/1000	
				fo	fo fo
fo				320	10 8

#### **Applications**

Typical Telephone Application: Figure 2 shows the schematic diagram of a typical telephone application for the S2561 tone ringer. Circuit power is derived from the telephone lines by the network formed by capacitor  $C_1$ , resistor  $R_1$ , diode bridge  $D_1$  through  $D_4$ , and filter capacitor  $C_2$ .  $C_2$  is chosen to be large enough so as to insure that the power supply ripple during ringing does not fall below the internal threshold level (typ. 7.3 volts) and to provide large enough decay time during the off period. A typical value of  $C_2$  may be  $.47\mu$ F.  $C_1$  and  $R_1$  are chosen to satisfy the Ringer Equivalence Number (REN) specification (Ref. 1). For REN = 1 the resistor should be a minimum of  $8.2k\Omega$ . It must be noted that the amount of power that can be delivered to the load depends upon the selection of  $C_1$  and  $R_1$ .

The device is enabled by limiting the incoming ring signal through resistors  $\rm R_2$ ,  $\rm R_3$  and diodes  $\rm d_5$  and  $\rm d_6$ . Zener diode  $\rm Z_1$  (typ. 9–27 volts) may be required in certain applications where large voltage transients may occur on the line during dial pulsing. The internal 2ms filter and the dial pulse reject filter will suppress any undesirable components of the signal and will only respond to the normal 20Hz ring signal. Ring signals with frequencies above 16Hz will be detected.

The configuration shown will produce a tone with frequency components of 512Hz and 540 Hz with a shift rate of approximately 16 Hz and deliver at least 25mW to an  $8\Omega$  speaker through a 2000 $\Omega$ :8 $\Omega$  transformer. If "manual" mode is used, a potentiometer may be inserted in series with the transformer primary to provide volume control. If "automatic" mode is used, resistors  $R_L$  and  $R_M$  can be chosen to provide desired amplitude sequencing. Typically, signal power

will be down 20 log 
$$\frac{R_{LOAD}}{R_L + R_{LOAD}}$$
 dB during the

first ring, and down 20 log 
$$\frac{R_{LOAD}}{R_M + R_{LOAD}}$$
 dB during the

second ring with maximum power delivered to the load beginning the third and consecutive rings.

In applications where dial pulse rejection is not necessary, such as in DTMF telephone systems, the ENABLE pin may be connected directly to  $V_{DD}$ . Det. Inh pin must be connected to  $V_{DD}$  to allow DC level enabling of the ringer.

Reference 1. Bell system communications technical reference: PUB 47001 of August 1976. "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment"—2.6.1. and 2.6.3