T-45-23-21

February 1991
Edition 1.0

FUJITSU

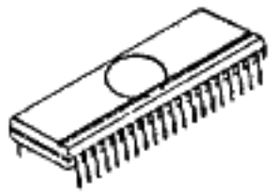
DATA SHEET

MB86040

CMOS PIPELINED DIVIDER WITH 10-BIT DIVIDEND, 8-BIT DIVISOR, AND 10-BIT QUOTIENT

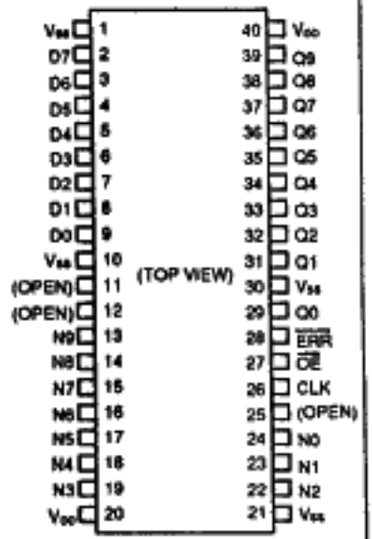
The MB86040 is a high-speed CMOS pipe-lined divider designed for high-speed image signal processing.
The MB86040 operates at up 10MHz and 10-bit quotient is generated with 10-bit dividend and 8-bit divisor.

- Single supply voltage: +5V ±5%
- Clock cycle time: 100ns min.
- Data format: Positive fixed point decimal number
- Pipeline configuration
- Divided by zero error detection function



PLASTIC PACKAGE
DIP-40P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE) V_{SS} = 0V

Ratings	Symbol	Conditions	Value	Unit
Supply voltage	V_{DD}	-	V_{SS} −0.5 to +6.0	V
Input voltage	V_I	-	V_{SS} −0.5 to V_{DD}+0.5	V
Output voltage	V_O	-	V_{SS} −0.5 to V_{DD}+0.5	V
Operating temperature	T_A	-	−25 to +85	°C
Storage temperature	T_{STG}	-	−40 to +125	°C
Output current *1)	I_O	V_O = V_{DD}	+70 (Maximum)	mA
		V_O = 0V	−40 (Maximum)	

*1) This is the output current per pin for V_{DD} = 5V and for a maximum of 1 second.

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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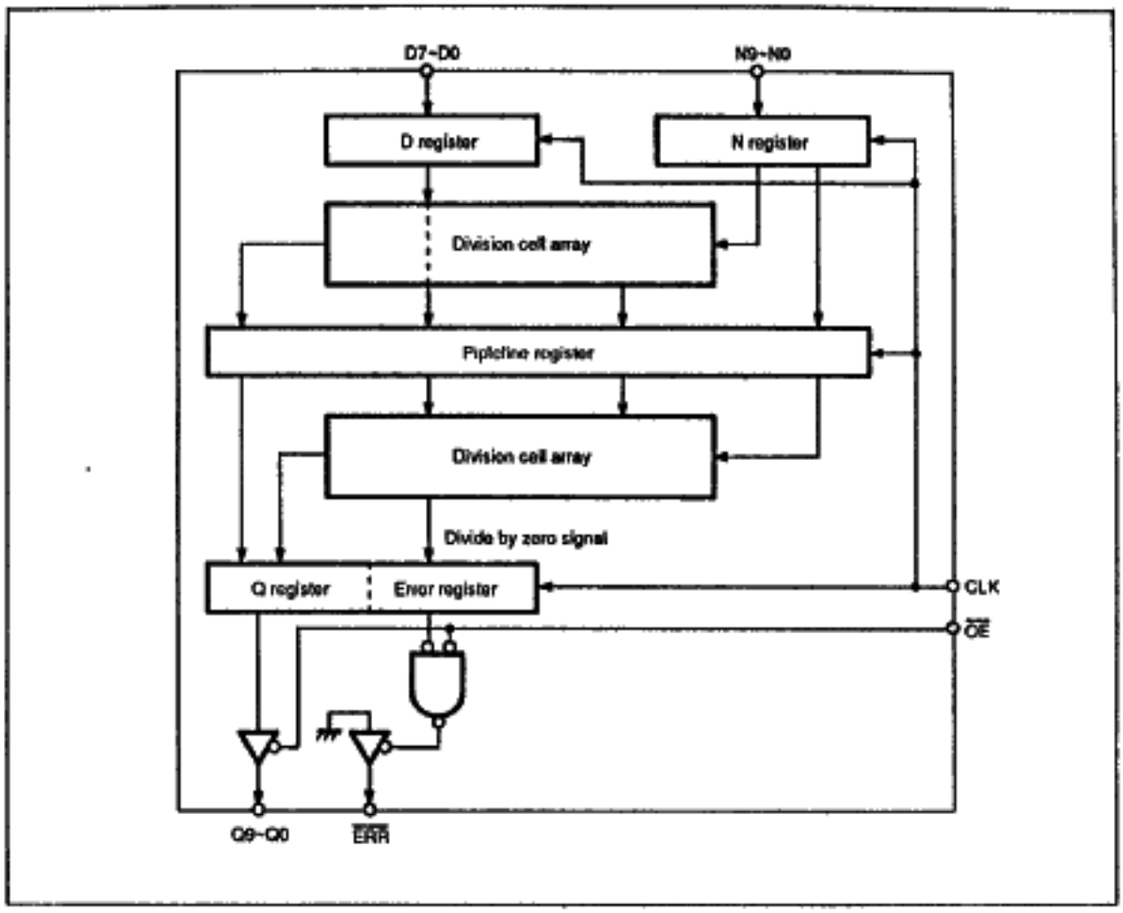
BLOCK DIAGRAM



DATA FORMAT

Dividend: N	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Divisor: D	D7	D6	D5	D4	D3	D2	D1	D0
	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Quotient: Q	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

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PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Descriptions
13~19 22~24	N9~N0	I	Dividend input pins. (Positive fixed point decimal number: 10-bit) MSB: N9 LSB: N0
2~9	D7~D0	I	Divisor input pins. (Positive fixed point decimal number: 8-bit) MSB: D7 LSB: D0
39~31 29	Q9~Q0	O	Quotient output pins. (Positive fixed point decimal number: 10-bit) MSB: Q9 (Three-state output) LSB: Q0
26	CLK	I	Clock input pin for the pipeline register. Data is latched on the rising edge of clock.
27	$\overline{OE}$	I	Q0 to Q9, $\overline{ERR}$ pins output enable signal input pin. When low, output pins are enabled. When high, output pins are set to high impedance.
28	$\overline{ERR}$	O	Error flag output pin. Goes low on detection of divide by zero when $\overline{OE}$ pin is low. The others case, goes to high impedance. (Open drain output)
20 40	V_{DD}	–	Supply voltage input (+5V) Connect all V_{DD} pins to the power supply line.
1, 10 21, 30	V_{SS}	–	Ground Connect all V_{SS} pins to network ground.
11, 12, 25	(OPEN)	–	No connection

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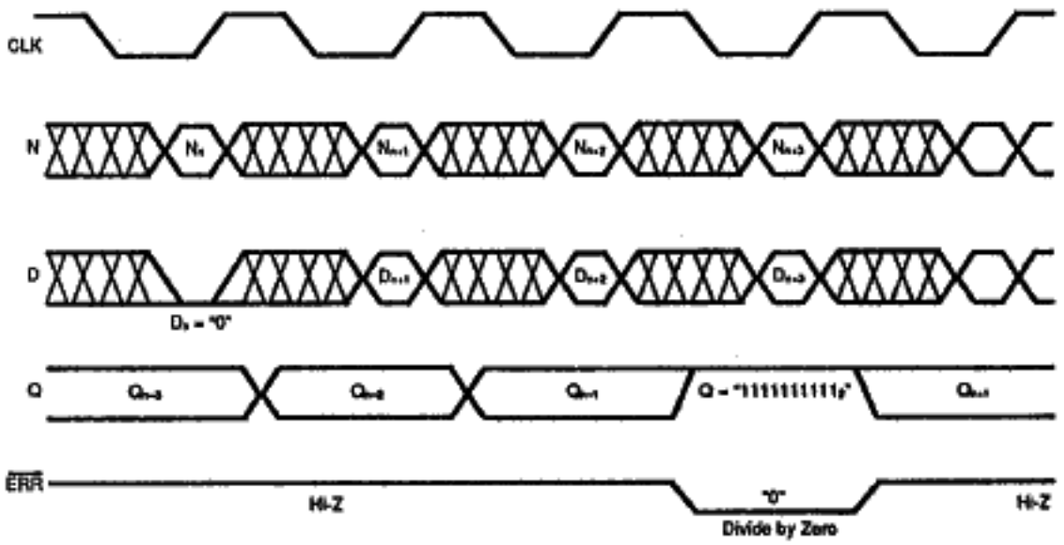
OPERATION DESCRIPTIONS

- The high speed operation technique and pipeline method enable 10MHz max operation speed.
- The MB86040 uses 2-stage pipeline method. The output delayed 3 cycles after input. The min output delay is 100ns. (See Figure-1)
- Input/output data is positive fixed point decimal number.
- When operation divided by zero is done (D_n = "0"), all bit of quotient (Q_n) becomes "1". $\overline{ERR}$ signal becomes low while this cycle.
- The residue is not output, the residue is omitted.

Fig. 1 – TIMING CHART



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply voltage	V_{DD}	–	4.75	5.00	5.25	V
Operating temperature	T_A	–	0	–	70	°C
High-level output current	I_{OH}	–	–	–	–2	mA
Low-level output current	I_{OL}	–	–	–	3.2	mA

DC CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply current	I_{DDS}	Static $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	–	–	0.1	mA
High-level input voltage	V_{IH}	–	2.2	–	–	V
Low-level input voltage	V_{IL}	–	–	–	0.8	V
High-level output voltage	V_{OH}	$I_{OH} = -2mA$	4.0	–	V_{DD}	V
Low-level output voltage	V_{OL}	$I_{OL} = 3.2mA$	V_{SS}	–	0.4	V
Input leakage current	I_{LI}	$V_I = 0V$ to V_{DD}	–10	–	10	µA

AC CHARACTERISTICS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
CLK cycle	t_{CC}	100	–	–	ns
CLK pulse width	t_{CW}	15	–	–	ns
N9~N0, D7~D0 set-up time	t_{SD}	15	–	–	ns
N9~N0, D7~D0 hold time	t_{HD}	15	–	–	ns
Q9~Q0, $\overline{ERR}$ hold time	t_{OH}	3	–	–	ns
Q9~Q0, $\overline{ERR}$ data valid delay time	t_{DV}	–	–	45	ns
Q9~Q0, $\overline{ERR}$ data valid delay time (from $\overline{OE}$)	t_{OVE}	0	–	40	ns
Q9~Q0, $\overline{ERR}$ data float delay time	t_{OZE}	0	–	40	ns

Note: The AC Chracteristics are guaranteed under the signal waveform shown on page 6.

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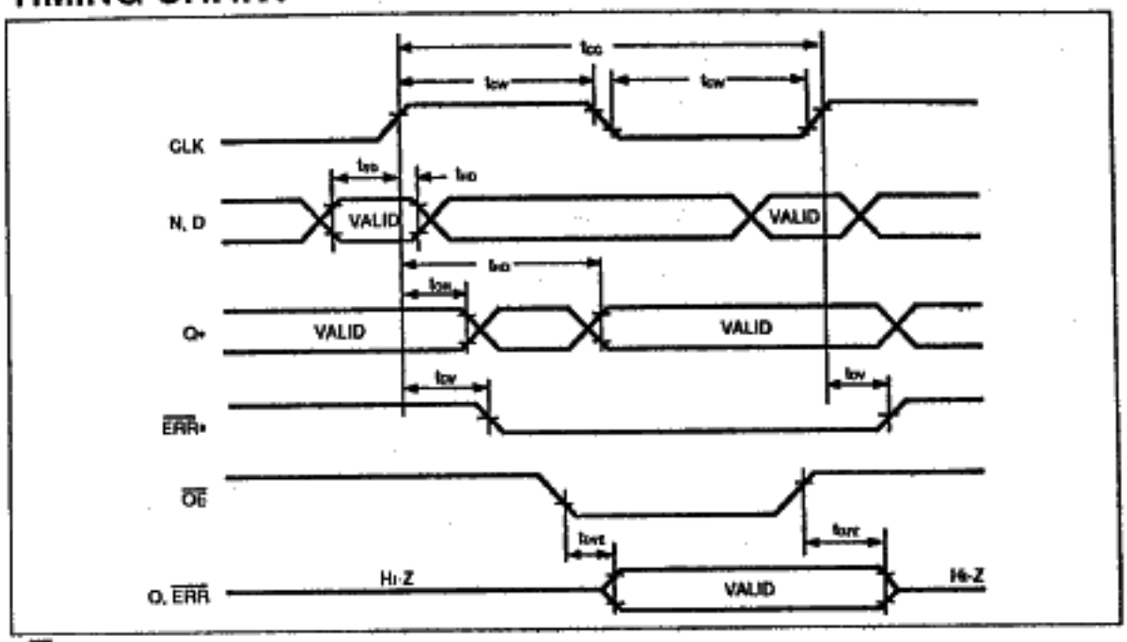
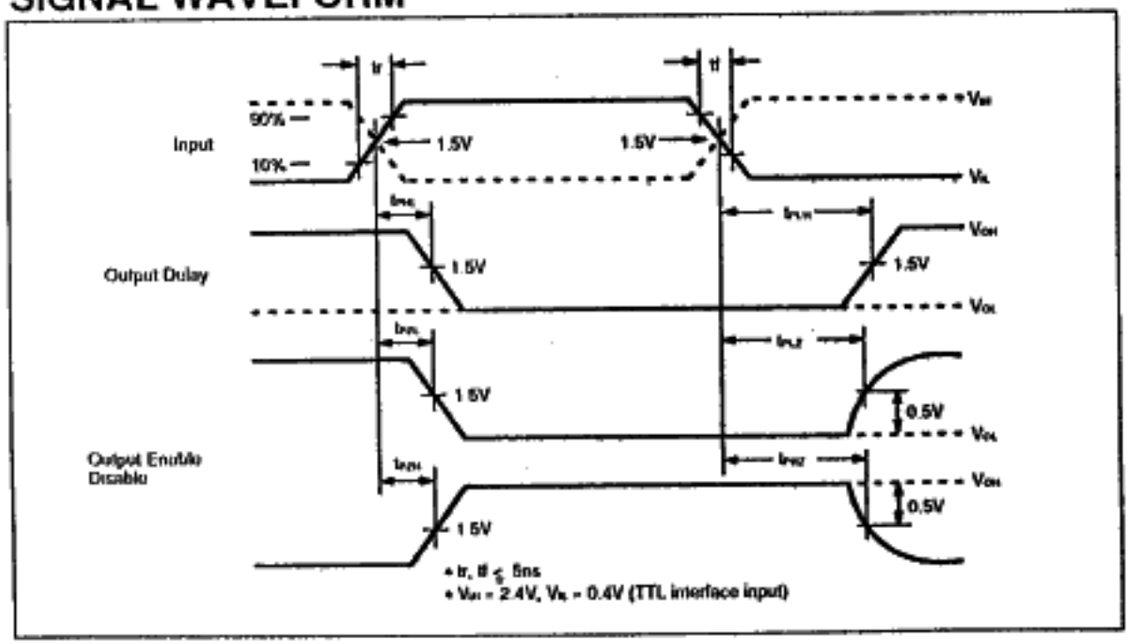
TIMING CHART



* $\overline{OE}$ = "L"

SIGNAL WAVEFORM



* tr, tf ≤ 5ns
* V_{IH} = 2.4V, V_{IL} = 0.4V (TTL interface input)

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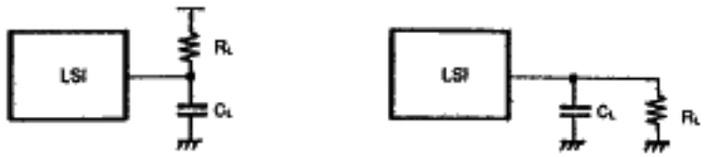
AC CHARACTERISTICS TEST CONDITION



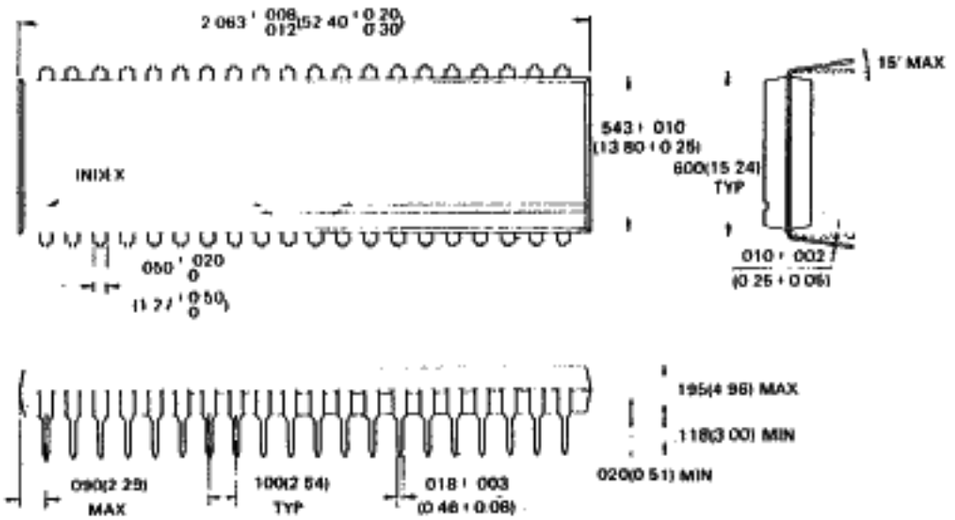
(a) $\begin{pmatrix} L \rightarrow Z \\ Z \rightarrow L \end{pmatrix}$ Delay test circuit

(b) $\begin{pmatrix} H \rightarrow Z \\ Z \rightarrow H \end{pmatrix}$ Delay test circuit

- Output load capacitance C_L = 65pF
- Output load resistance R_L = 2kΩ

PACKAGE DIMENSIONS

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40P-M01)



Dimensions in inches (millimeters)