

**STRUCTURE** 

Silicon Monolithic Integrated Circuits

**PRODUCT SERIES** 

3 in 1 Motor Driver for Digital Video Camera

**TYPE** 

**BD6300KU** 

**FUNCTIONS** 

· 3-phase motor driver for capstan , 3-phase sensor-less motor driver for cylinder,

Reversible motor driver for loading

#### OABSOLUTE MAXIMAM RATINGS (Ta=25°C)

Parameter	Symbol	Limit	Unit
Supply voltage	VCC	7	٧
	UNREG	15	٧
	C_VM	10	٧
	D_VM	10	٧
	L_VM	7	٧
Power dissipation	Pd	1750*	mW
Operate temperature	Topr	-25~+75	°C
Storage temperature	Tstg	-40~+150	°C
Output max current	IOMAX	800 * *	mA
Junction temperature	Tjmax	150	°C

<sup>\* 70</sup>mm × 70mm × 1.6mm glass epoxy board. Derating in done at 14mW/℃ for operating above Ta=25℃

#### **OOPERATING CONDITIONS**

Parameter	Symbol	Limit	Unit
Supply voltage	VCC	2.7~4.5	V
	UNREG	5~12*	٧
	C_VM	0~8*	٧
	D_VM	0~8*	V
	L_VM	4.5~5.5	V

<sup>\*</sup> UNREG≧C\_VM,UNREG≧D\_VM, L\_VM≧VCC

#### Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

#### Application example

- ROHM cannot provide adequate confirmation of patents.
- The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
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<sup>\* \*</sup> However, do not exceed Pd, ASO and Tj=150°C (Common to 3 drivers)

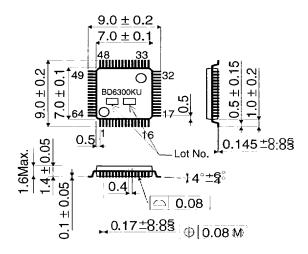


 $OELECTRICAL\ CHARACTERISTICS\ (Unless otherwise\ specified\ Ta=25°C, VCC=3V,\ C\_VM=D\_VM=L\_VM=5V,\ UNREG=7.2V)$ 

ļ	Parameter	Symbol	Min,	Limit	Max.	Unit	Conditions
TOTAL	VCC Circuit current 1	ICC1	5	Typ. 11	17		Power save OFF
TOTAL	VCC Circuit current 2	ICC2	1	4	<del>'</del> /	mA mA	Power save OFF
	VG voltage	VG	9.5	11	12.5		rower save ON
CAPSTAN	Output H voltage1	C VOH1	-	0.1	0.16	·	IOUT=-200mA
OUTPUT	Output H voltage2	C_VOH2		0.2	0.32	v	IOUT=-400mA
	Output L voltage	C_VOL		0.2	0.32	·······································	IOUT=200mA,C_RNF=0.33Ω
CAPSTAN	In-phase input voltage range	C_VCM	1.2		VCC-1.1	v	
HALL AMP	Hall input offset voltage	C_VHOFS	-15	_	+15	mV	
CAPSTAN	EC input bias current	C_IEC		3.0	7.5	μА	C_EC=VCC
TORQUE CONTROL	Torque control input/output gain	C_GIO	0.42	0.60	0.78	A/V	C_RNF=0.33 Ω, C_RCC=3.3k Ω
	Torque control start voltage	C_VECOFS	1.05	1.2	1.35	٧	
	Current limit voltage	C_CLIMIT	0.25	0.330	0.410	V	C_RNF=0.33Ω
	Ripple Cancel Ratio	C_VRCC	22	45	68	%	IOUT=100mA, C_RCC=3.3kΩ C_RNF=0.33Ω
CAPSTAN	Voltage gain	C_GVS	7	8	9	TIMES	
	vonage gain	C_GV3	·		J	IIMES	1010
VS	Output H voltage	C_VVSOH	_	0.5	0.8	٧	IOVS=-1mA, between VCC and output
0.007	Output L voltage	C_VVSOL	-	0.13	0.2	٧	IOVS=50 μ A
CAPSTAN FGSMT	In-phase input voltage range	C_VFGCM C_IFG	0.35	_	VCC-1.1	V	
FGSMT	Input bias current	C_VFGSOH			1	μA V	
	Output H voltage Output L voltage	C_VFGSOL	2.8	0.1	0.3	<u>v</u>	101 1-4
DRUM	Output H voltage	D_VOH	_	0.3	0.48	V	IOL=1mA IOUT=-400mA
OUTPUT	Output L voltage	D_VOL		0.28	0.40	<del>v</del>	IOUT=100mA
0011 01	D PS input	<u></u>					1001=100mA
	switching level	D_PS	0.7	1.4	2	V	
DRUM	EC input bias current	D IEC		2.0	5.0	μА	D_EC=VCC
TORQUE CONTROL	Torque control				· · · · · · · · · · · · · · · · · · ·		
	input/output gain	D_GIO	0.45	0.66	0.87	A/V	D_RNF=0.33 Ω
	Torque control start voltage	D VECOFS	1.05	1.2	1.35	V	
	Current limit voltage	D_CLIMIT	0.217	0.274	0.332	V	D_RNF=0.33Ω
DRUM STARTIING/ DETECTION	DETECT terminal charge current	D_IDETO	2	5	10	μА	
	DETECT terminal discharge current	D_IDETI	2	5	10	μΑ	
	DETECT terminal H voltage	D_VDETH	1.1	1.3	1.5	٧	
	DETECT terminal L voltage	D_VDETL	0.5	0.65	0.8	V	
DRUM	ISET voltage	D_VISET	0.32	0.4	0.48	V	RISET=18kΩ
SLOPE	SL1,2 charge current	D_ISLO	16	22	28	μΑ	RISET=18kΩ
	SL1,2 discharge current	D_ISLI	17	24	31	μА	RISET=18kΩ
	SL1,2 H voltage	D_VSLH	2.5	2.8		V	
	SL1,2 L voltage	D_VSLL	0.85	1	1.15	V	
	SL1,2 charge and discharge current ratio	D_RSL	0.82	0.89	0.96	٧	
DRUM	Voltage gain	D_GVS	7	8	9	TIMES	
VS	Output H voltage	D_VVSOH	_	0.5	0.8	V	IOVS=-1mA, between VCC and output
	Output L voltage	D_VVSOL	_	0.13	0.2	V	IOVS=50 μ A
DRUM	DC bias voltage	D_VFG+	1/2 VCC-0.2	1/2 VCC	1/2 VCC+0.2	٧	
FGAMP/SMT	In-phase input voltage range	D_VFGCM	0.35		VCC-1.1	٧	
	Input bias current	D_IFG	_	_	1	μΑ	
	Output H voltage	D_VFGSOH	2.8	_		V	
	Output L voltage	D_VFGSOL	_	0.1	0.3	٧	IOL=1mA
DRUM PGAMP	DC bias voltage	D_VPG+	1/2 VCC-0.2	1/2 VCC	1/2 VCC+0.2	V	
	In-phase input voltage range	D_VPGCM	0.35		VCC-1.1	V	
	Output H voltage	D_VPGSOH D_VPGSOL	2.8			V	100 1-4
LOADING	Output L voltage Output saturation voltage	L_VSAT	-	0.14	0.3	v v	IOL=1mA  IOUT=200mA, L_REF=L_VM  Total saturation voltage of low
	I DEC sis is a second	L_IIREF		0.0	2	ļ	and high side output transistor
	L_REF pin input current	L_UNEF		0.3		μA	L_REF=L_VM
DEAL AMP	V_out-L_REF offset Input bias current	R_IIN	_	100	200	mV	
REAL AMP	Input offset voltage	R_VOFS	-8		1 8	μA mV	
	In-phase input voltage	R_VINCM	0.35		VCC-1.1	mv	
	Output L voltage	R_VSOL	- 0.35	0.1	0.3	ŀ∵v⊤	IOL=1mA

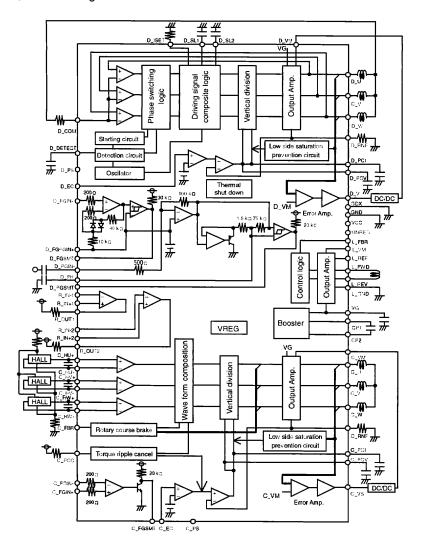


# OPackage outline (Plastic Mold)



UQFP64 (Unit:mm)

# O Block Diagram



# OTerminal function table

PIN NO.	PIN Name	PIN NO.	PIN Name
1	D_PH_	33	R_IN+2
2	D_FGIN-	34	R_IN-2
3	D_FGPGIN	35	R_OUT2
4	D_PGIN-	36	VG
5	D_FGSMT	37	CP2
6	vcc	38	CP1
7	D_DETECT	39	GND
8	D_ISET	40	GDX
9	D_SL1	41	D_PS
10	D_SL2	42	C_PS
11	UNREG	43	C_FBR
12	D_VM	44	C_VM
13	D_VS	45	C_VS
14	D_EC	46	C_EC
15	D_PCI	47	C_PCI
16	D_PCV	48	C_PCV
17	D_COM	49	FGND1
18	D_U	50	C_U
19	D_V	51	C_V
20	D_RNF	52	C_RNF
21	D_W	53	C_W
22	N.C.	54	C_RCC
23	FGND2	55	C_HV-
24	L_FBR	56	C_HV+
25	L_REF	57	C_HU-
26	L_FWD	58	C_HU+
27	L_GND	59	C_HW+
28	L_REV	60	C_HW-
29	L_VM	61	C_FGIN+
30	R_IN+1	62	C_FGIN-
31	R_IN-1	63	C_FGSMT
32	R_OUT1	64	D_PGSMT



## O NOTES FOR USE

#### 1) Absolute maximum ratings

When the absolute maximum rating of applied voltage, operation temperature range, etc is exceeded, destruction is possible. In case of destruction, short-circuit mode or open mode cannot be identified; therefore when special mode is envisioned where absolute maximum rating may be exceeded, please take a physical safety measure such as use of fuse.

## 2) Power supply line

Return of regenerated current is caused by back electromotive force of motor, therefore take a measure such as placing a capacitor between power supply and GND for routing regenerated current, and fully ensure that various characteristics of electric field capacitor have no problem such as pull-out capacity at a low temperature before determining a capacity value.

#### 3) GND potential

Ensure that the potential of GND terminal is the minimum potential in any operating condition. Also ensure that all terminals except GND terminal do not fall below GND voltage including transient phenomenon. However, it is possible that the motor output terminal may deflect below GND because of influence by back electromotive force of motor. Trouble such as malfunction may possibly occur depending on use condition, environment, and property of individual motor. Fully make sure that no problem is found on operation of IC etc.

#### 4) Thermal design

Consider the permissible loss (Pd) under actual use condition and apply thermal design with sufficient margin.

#### 5) Operation in strong electromagnetic field

Use in strong electromagnetic field may cause malfunction. Be careful.

#### 6) ASO

In using this IC, perform setting so that the output Tr does not exceed the absolute maximum rating and ASO.

#### 7) Thermal shut down circuit

BD6300KU is built in the protection of IC and power supply circuit and so on, and Thermal shut down circuit for safety. Operation temperature is to 175°C(Typ) and hysteresis width is 25°C(Typ). The condition of Output terminal is OPEN when chip temperature of IC rise and TSD circuit operate. Please be careful as this is effective against being due to output current like exceeding power dissipation and short of output, but is not effective in case of flowing large current into IC generating heat by internal destruction of IC and short during terminal.

#### 8) GND wiring pattern

When there are small signal GND and large current GND, separate the large current GND pattern from small signal GND pattern. It is recommended to apply one-point grounding at the reference point of the set in order that resistance of wiring pattern and large current do not cause change of voltage of small signal GND. Please be cautious not to fluctuate the wiring pattern of GND of external mounted parts.

## 9) Capacitor between output and GND

When a large capacitor is connected between output and GND, if Vcc is shorted with 0V or GND for some cause, it is possible that the current charged in the capacitor may flow into the output resulting in destruction. Keep the capacitor between output and GND below 100uF.

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