

## 150 MHz PIXEL VIDEO CONTROLLER FOR MONITORS IN DC-COUPLING MODE

### FEATURES

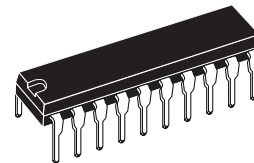
- 150 MHz Pixel Rate
- 2.7 ns Rise and Fall Time
- I<sup>2</sup>C Bus Controlled
- Support DC Coupling Application only
- Brightness Selection (after or before Drive)
- Grey Scale Tracking Versus Brightness
- InfraBlack Range Selection 1.3 or 1.8V (i.e: 26 or 36V in kit with STV95xx amplifier)
- InfraBlack Offset Selection 0.4 to 2.2V (i.e: 115 to 80V in kit with STV95xx amplifiers)
- OSD Mixing
- Beam Current Attenuation (ABL)
- Pedestal Clamping on Output Stage
- Possibility of Light or Dark Grey OSD Background
- OSD Contrast Control
- Input Black Level Clamping with Built-in Clamping Pulse
- 5 V to 8 V Power Supply
- Perfectly matched with the STV95xx ST Amplifier Family
- Pre-amplifier Control (bandwidth and stand-by)
- Amplifier Control (bandwidth and stand-by), only applicable to amplifiers with CTL pin or STDBY pins.

### DESCRIPTION

The STV9211 is an I<sup>2</sup>C Bus controlled RGB pre-amplifier designed for Monitor applications, able to mix the RGB signals coming from any OSD device. The usual Contrast, Brightness, Drive and Cut-Off (InfraBlack) Controls are provided.

In addition, it includes the following features:

- High resolution cut-off (InfraBlack) adjustment,
- OSD contrast,
- Bandwidth and stand-by control,
- Brightness before/after Drive Selection.



**DIP20**  
(Plastic Package)

**ORDER CODE:** STV9211

The RGB incoming signals are amplified and shaped to drive in DC coupling the video amplifier without intermediate follower stages.

One of the main advantages of ST devices is their ability to sink and source currents.

These driving capabilities combined with an original output stage structure suppress any static current on the output pins and therefore reduce dramatically the power dissipation of the device.

Extensive integration combined with high performance and advanced features make the STV9211 one of the best choice for any CRT monitor.

Perfectly matched with the ST video amplifiers STV95xx, they offer a complete solution for high performance and cost-optimized Video Board Application.

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## Revision follow-up

### Target specification

December 2000	version 1.0	document created
January 2001	version 1.1	reformatted with ST new corporate template
January 2001	version 1.2	General update - replacement of some figures , - correction and addition of registers First ADCS release
April 2001	version 1.3	General update - replacement of some figures , - correction of text, - addition of sections
June 2001	version 1.4	General update and addition of: - chapter 10: Application hints, - chapter 11: Internal, schematics, - chapter 12: application boards

### Product preview

October 2001	version 2.0	General update: - replacement of some figures, - addition of sections : cut-off adjustment..., - addition of figures (I2C, Cut-off adjustment) - TDA95xx salestype replaced with STV95xx
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### Preliminary data

December 2001	version 3.0	General update - figures replaced - Cut-off replaced with Infra-Black
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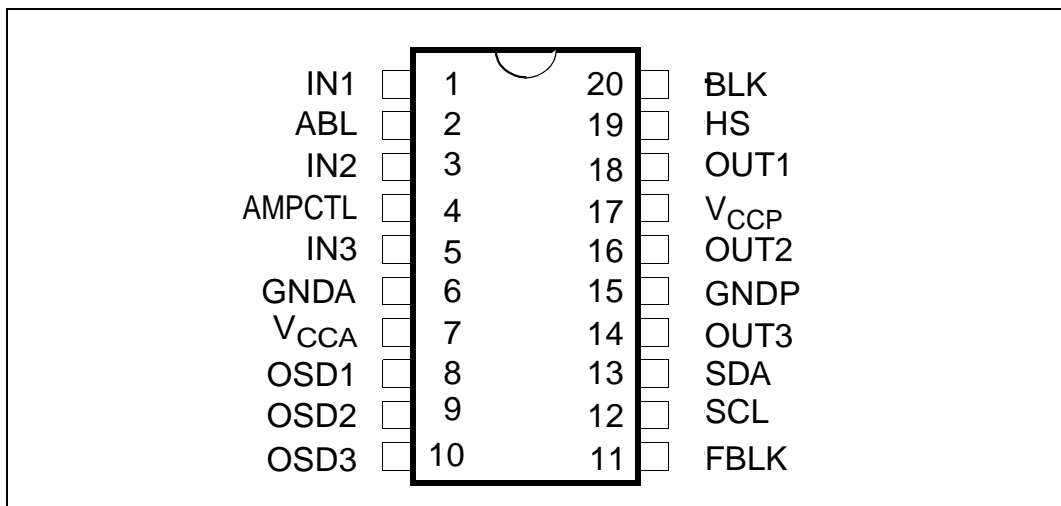
### Datasheet

January 2002	version 4.0	<u>section 1.2</u> : pin description modified for IN1, IN2, IN3, OSD1, OSD2, OSD3 and OUT1, OUT2, OUT3: replaced with video input, OSD input, Video output (channel 1, red), (channel 2, green), (channel 3, blue) respectively <u>Block diagram</u> replaced <u>section 2.3</u> Blanking input added <u>Section 2.8</u> - Cut-off adjustment: Tables 1 and 2 gathered into table 1 <u>Section 2.12</u> - preamplifier bandwidth adjustment (4 bits) instead of 3 bits previously <u>Chapter 10 - Application hints</u> tables 9 and 10 replaced with table 1 Cross reference to AN1445 replaced with AN1510
February 2003	version 4.1	Text changed in section 2.2. Text changed and figure removed in section 2.3.

# 1 PIN CONNECTION, PIN DESCRIPTION

## 1.1 Pin connection

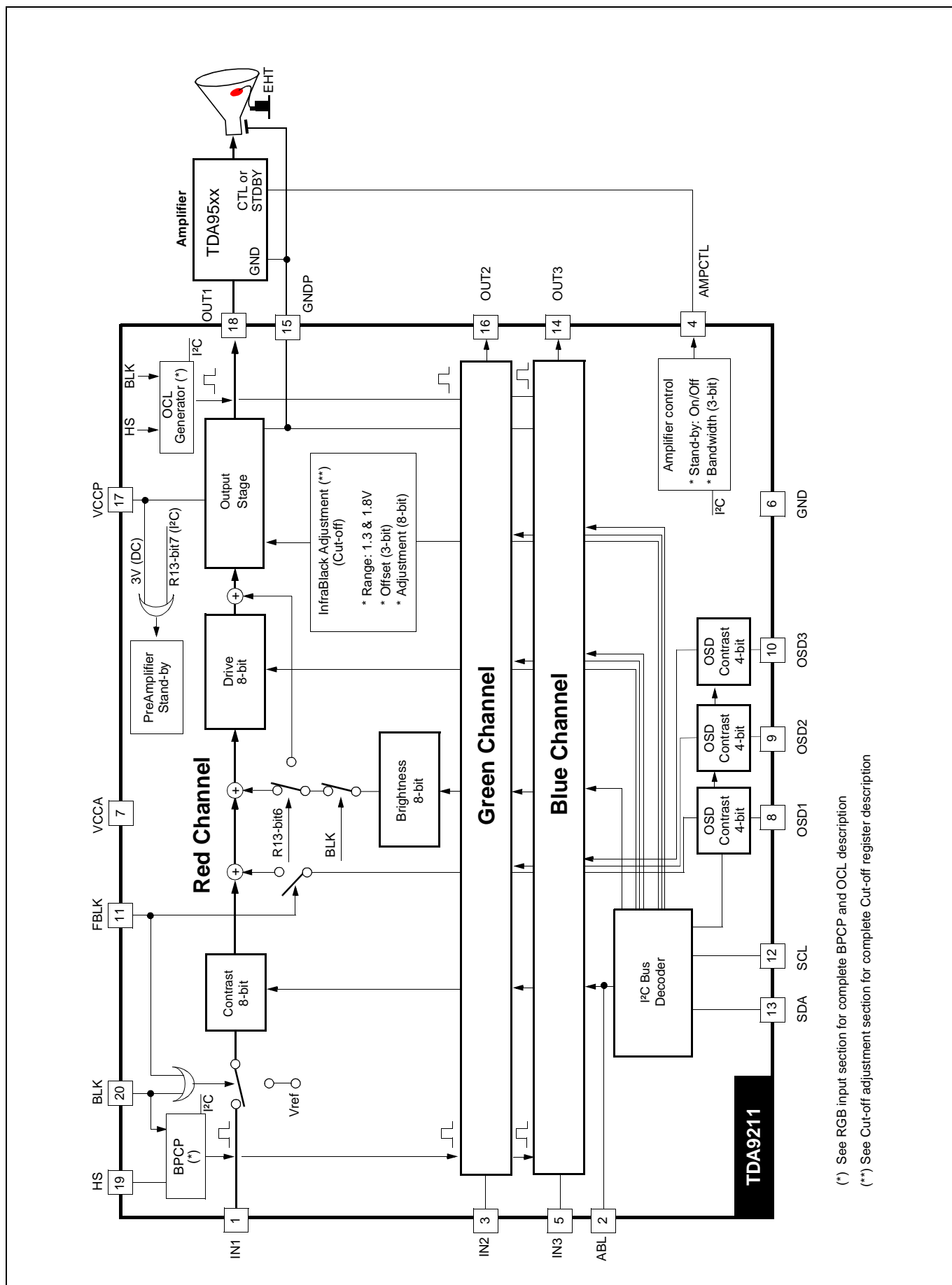
Figure 1: STV9211 pin connection



## 1.2 Pin description

Pin number	symbol	description
1	IN1	Video input (channel 1, red)
2	ABL	ABL input
3	IN2	Video input (channel 2, green)
4	AMPCTL	Amplifier control (bandwidth and stand-by). Only applicable with amplifiers with the CTL or STDBY pins. To be connected to ground if not used.
5	IN3	Video input (channel 3, blue)
6	GNDA	Analog ground
7	V <sub>CCA</sub>	Analog supply (5V)
8	OSD1	OSD input (channel 1, red)
9	OSD2	OSD input (channel 2, green)
10	OSD3	OSD input (channel 3, blue)
11	FBLK	Fast blanking
12	SCL	SCL
13	SDA	SDA
14	OUT3	Video output (channel 3, blue)
15	GNDP	Power ground
16	OUT2	Video output (channel 2, green)
17	V <sub>CCP</sub>	Output stage supply (5 V to 8 V)
18	OUT1	Video output (channel 1, red)
19	HS	Horizontal synchro or BPCP pulse
20	BLK	Blanking input

Figure 2: Block diagram



(\*) See RGB input section for complete BPCP and OCL description

(\*\*) See Cut-off adjustment section for complete Cut-off register description

## 2 FUNCTIONAL DESCRIPTION

### 2.1 RGB input, clamping function

The three RGB inputs have to be supplied with a video signal (maximum peak-to-peak value = 1V) through coupling capacitors (100 nF typ.).

The RGB inputs include a clamping function using the input serial capacitor as “memory capacitor”. To avoid the discharge of this capacitor during the line (due to leakage current), the input voltage is referenced to the ground.

This clamping function is gated by the BPCP pulse (Black Porch Clamping Pulse) which is internally generated (see [Figure 4](#)). The Register 8 allows to choose the way to generate this BPCP (see [Figure 3](#) and [Figure 4](#)).

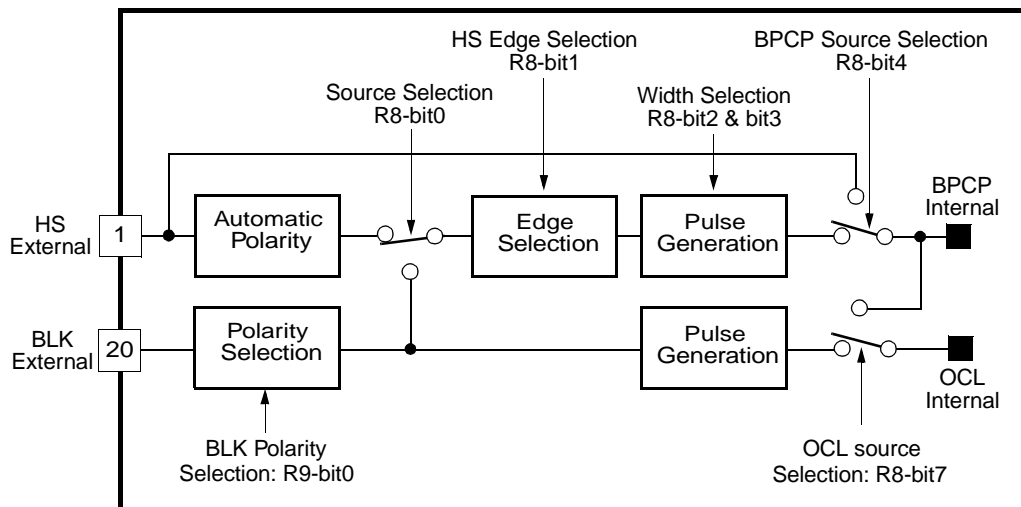
- Synchronization: HS or BLK signal (Register 8, bit0)
- Polarity: Positive or negative (Automatic detection) when synchronized by HS  
Positive or negative ( programmed via Register 9, bit 0) when synchronized by BLK - see [Note 1](#)
- Edge: Trailing or Leading (Register 8, bit1)
- Width: From 0.33 $\mu$ s to 1.33 $\mu$ s (Register 8, bit2 and bit3)
- Direct BPCP: If the application provides the BPCP, one can program the direct connection between Pin 19 and the internal BPCP (Register 8, bit4)

*Note 1: When BPCP is synchronized by BLK, the leading edge of the BLK must be selected to get a proper synchronization.*

**Figure 3: BPCP selection of synchronization edge**

Synchronization source	Edge selection	BPCP generation	
HS (R8, bit 0=0)	Trailing (R8, bit 1=0)	HS (Pin 19)	
	Leading (R8, bit 1=1)	HS (Pin 19)	
BLK (R8, bit 0=1)	Leading (R8, bit 1=0)	BLK (Pin 20)	
HS (R8, bit 4=1)	–	HS (Pin 19)	

Figure 4: BPCP and OCL generation



## 2.2 Fast blanking input

The fast blanking pin (FBLK) is TTL compatible. When it is at high level, the input signal is blanked and replaced by OSD insets defined by binary levels on three OSD inputs and a dedicated OSD contrast adjustment stage.

## 2.3 Blanking input

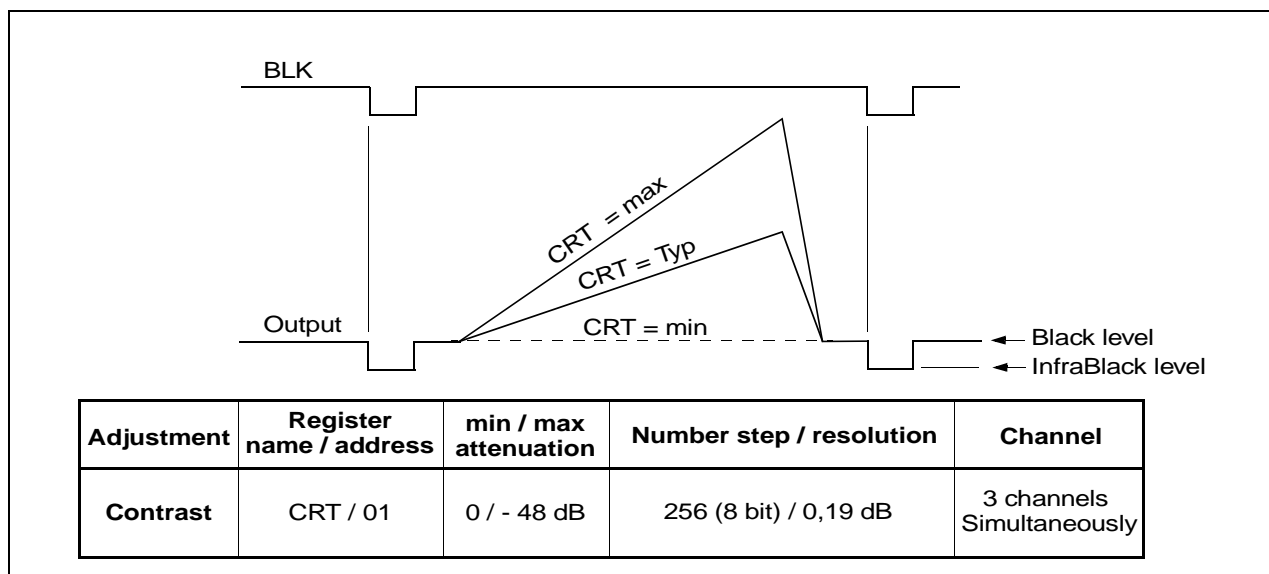
The blanking input BLK is TTL compatible. The active level is either high (positive pulse polarity) or low (negative pulse polarity). When the level is active, the RGB outputs are at infra-black level, regardless of the input level. The pulse on the BLK input defines the timing of the internal OCL signal and it can also define the timing of the internal BPCP pulse. See [Figure 4](#), [Figure 11](#) and [Chapter 9: I2C register description](#).



## 2.4 Contrast adjustment (8 bits)

The contrast is adjusted simultaneously on, the 3 RGB channels via three internal amplifiers delivering a 48dB attenuation range (see Register 1, I<sup>2</sup>C table 1 and [Figure 5](#)). .

Figure 5: Contrast adjustment



## 2.5 Brightness/Drive selection (1 bit)

The brightness position is selectable by I<sup>2</sup>C (Register 13, bit6. See I<sup>2</sup>C table 4).

There are 2 cases:

- bit6=0            The brightness is located before the Drive (as for the TDA9210).  
The advantage is to keep the “White balance” tracking when changing the brightness level.
- bit6=1            The brightness is located after the Drive.  
The advantage is to perform the “White balance” tracking faster (typically one adjustment less than in the previous case)

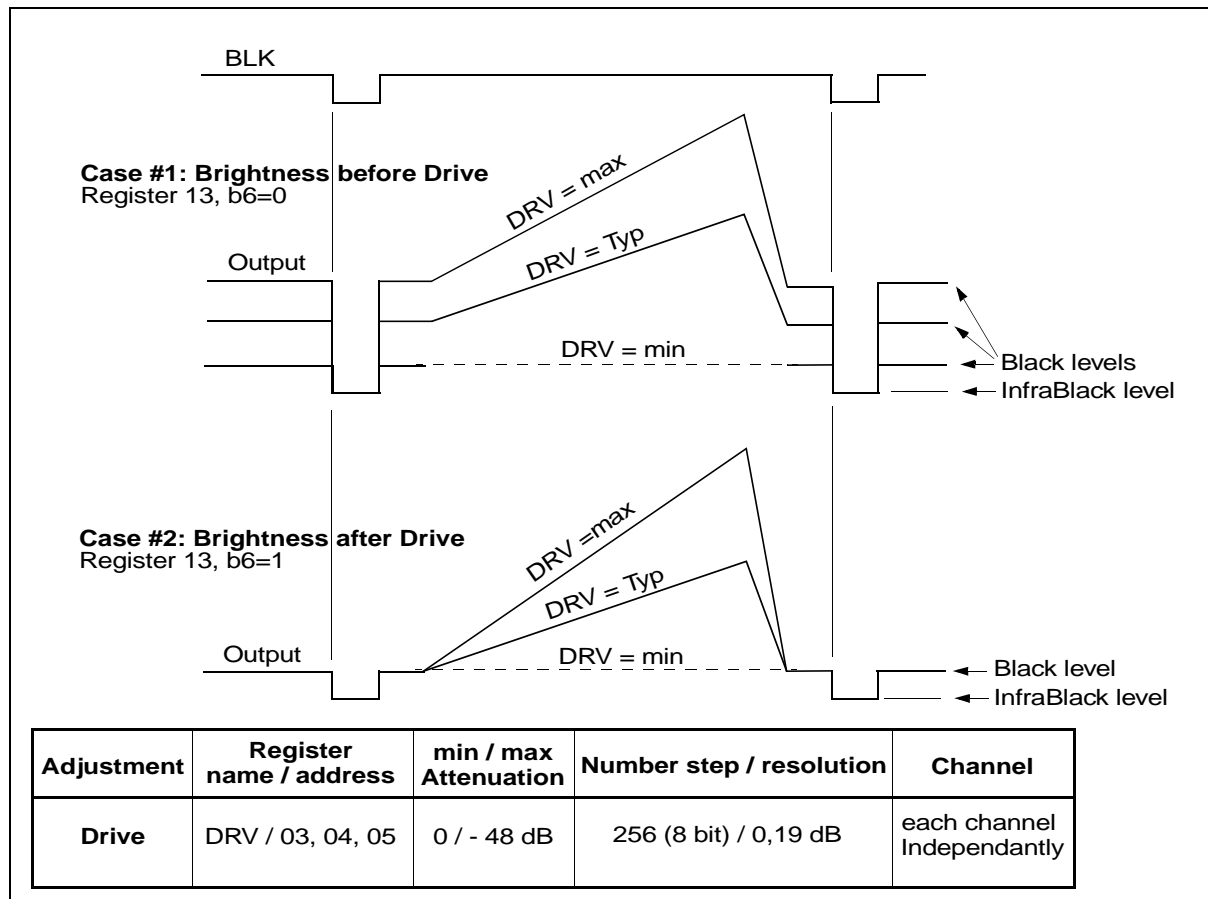
## 2.6 Drive adjustment (3 x 8 bits)

In order to perform the “White balance” adjustment, the gain of the three RGB signals are adjustable separately via the three Drive amplifiers (Registers 3, 4 and 5, I<sup>2</sup>C table 1).

The very large range of the Drives (48 dB) allows different standards or custom color temperatures.

It can also be used to adjust the output voltages at the optimum amplitude to drive the CRT drivers, keeping the whole contrast control for the end-user only.

Figure 6: Drive adjustment

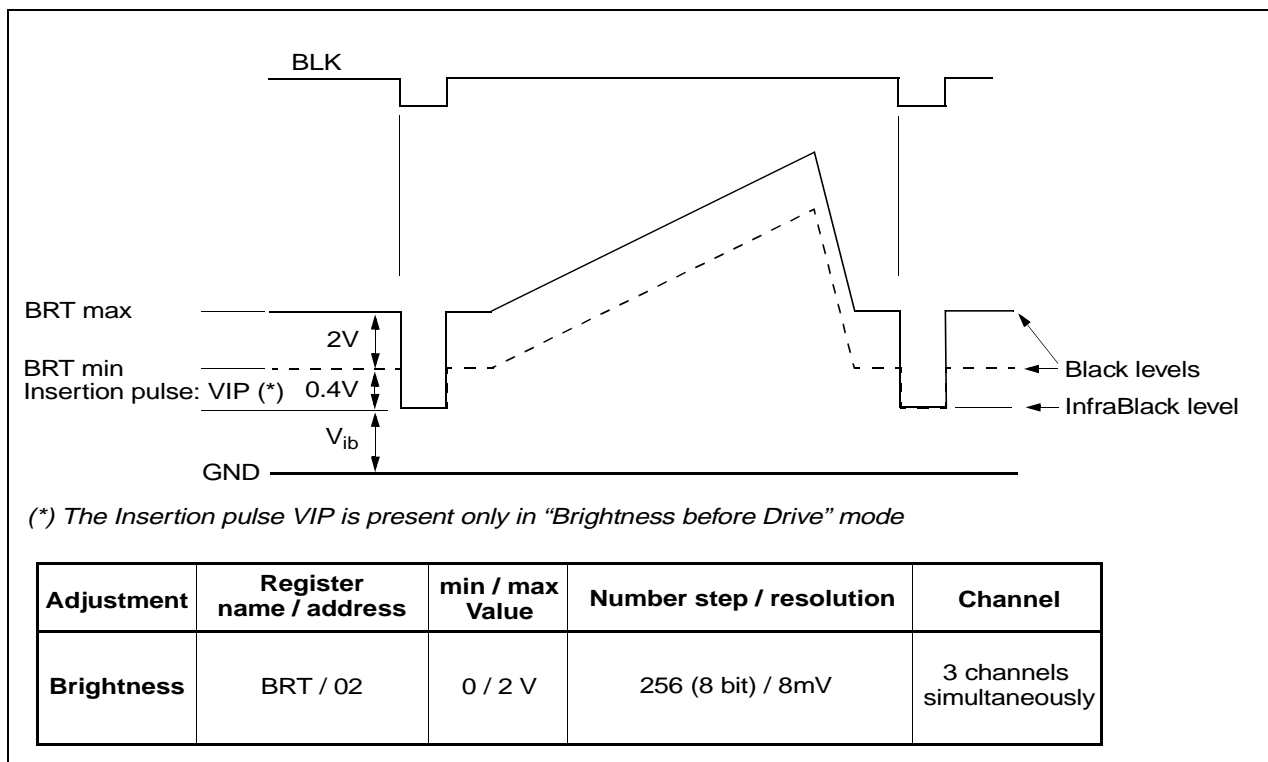


## 2.7 Brightness adjustment (8 bits)

Brightness adjustment is controlled by Register 2 (I<sup>2</sup>C table 1). It consists of adding the same DC voltage (BRT) to the three RGB signals. This DC voltage can be adjusted between 0 and 2V, outside the blanking pulse with 8mV adjustment steps (see [Figure 7](#)).

Inside the blanking pulse the DC output level is forced to the “Infra Black” level ( $V_{ib}$ ).

Figure 7: Brightness adjustment



## 2.8 Cut-off adjustment, Infra-black level (Vib) (3x8 bits)

The Infra-black level (Vib) is the output voltage during the blanking time (BLK). This level is sampled after each line (sample - and - hold block) during an internal pulse (OCL) which is generated during the blanking pulse (see [Figure 4](#)).

The STV9211 allows to adjust independantly the cut-off levels of the 3 video outputs with a high resolution. This is done via 3 registers (IBR, IBO and IBL) programming respectively:

- the range: 1.3 or 1.8V (i.e: 26 or 36V in kit with the STV95xx amplifiers)
- the offset (to keep the video signal inside the linear area)
- the level.

**Infra-black range register (IBR:** Register 14, bit 0. See I<sup>2</sup>C table 6)

This register must be selected first, either to 1.3V to get a 26V Cut-off adjustment range with the STV95xx amplifier or to 1.8V to get a 36V range (see [Figure 8](#))

**Infra-black offset register (IBO:** Register 14, bit 1, 2 & 3. See I<sup>2</sup>C table 6)

This register select the Vib offset. It allows to keep the video signal inside the linearity area of the amplifier.

The value of this register depends on the amplifier high voltage supply (Vdd).

In kit with the STV95xx amplifier family, we recommend the following programming:

**Table 1: Setting of the infra-black offset register (IBO)**

Vdd ( $\pm 5\%$ )	Case 1: Brightness before Drive		Case 2: Brightness after Drive	
	Binary	Decimal	Binary	Decimal
112 to 115V	001	1	011	3
107 to 111V	010	2	100	4
102 to 106V	011	3	101	5
97 to 101V	100	4	110	6
92 to 96V	101	5	111	7
88 to 91	110	6	111	7
87 and below	111	7	111	7

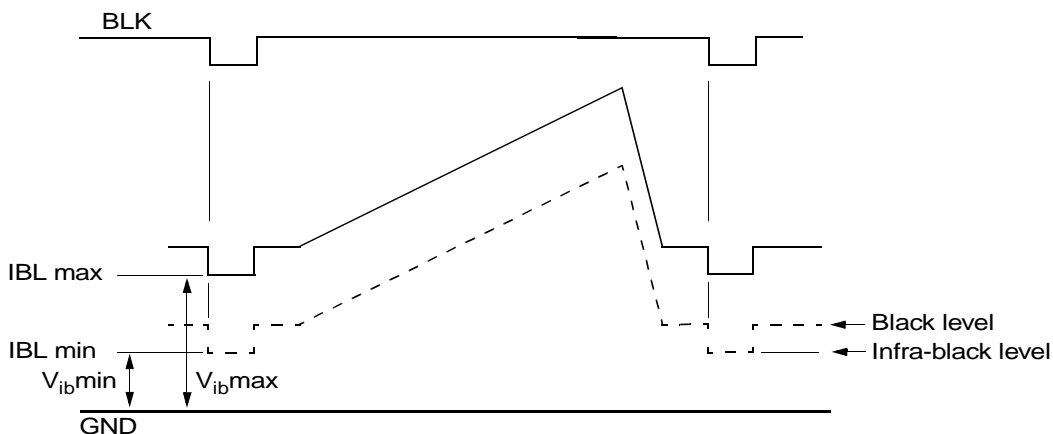
### Example:

For Vdd=101V +/-5% and Brightness before Drive, IBO must be set to 100.

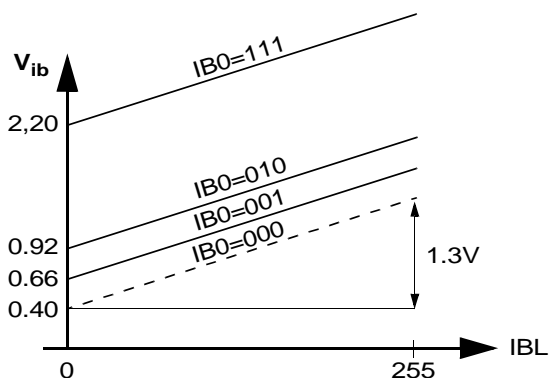
**Infra-black level register (IBL:** Register 10, 11, 12. See I<sup>2</sup>C table 1)

These three 8 bit- registers adjust independantly the infra-black level of the 3 outputs with a high resolution (typically 100mV at 26V range or 140mV at 36V range).

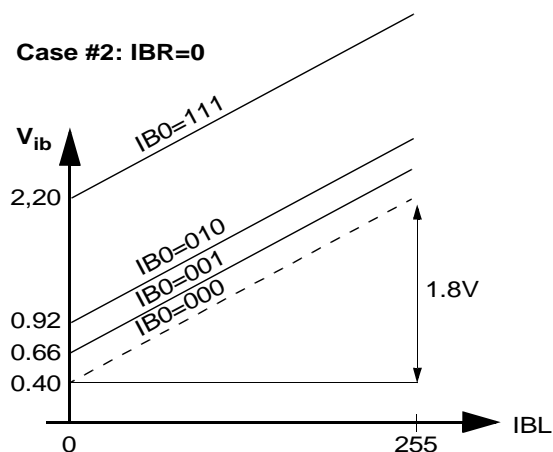
Figure 8: Infra-black level adjustment



Case #1: IBR=1



Case #2: IBR=0



Adjustment	Register name & address	Selection	min / max value	Number step / resolution	Channel
InfraBlack Range	IBR / 14	-	1.3 or 1.8 V	2 selections	3 channels Simultaneously
InfraBlack Offset	IBO / 14	-	0.4 to 2.2 V (@ IBL=0)	16 (3 bit) / 0.26V	3 channels Simultaneously
InfraBlack Level	IBL / 10, 11, 12	Examples #1 IBR=1 IBO=000	0.40 to 1.70V	256 (8 bit) / 5 mV	each channel Independantly
		Examples #2 IBR=0 IBO=010	0.92 to 2.72 V	256 (8 bit) / 7mV	

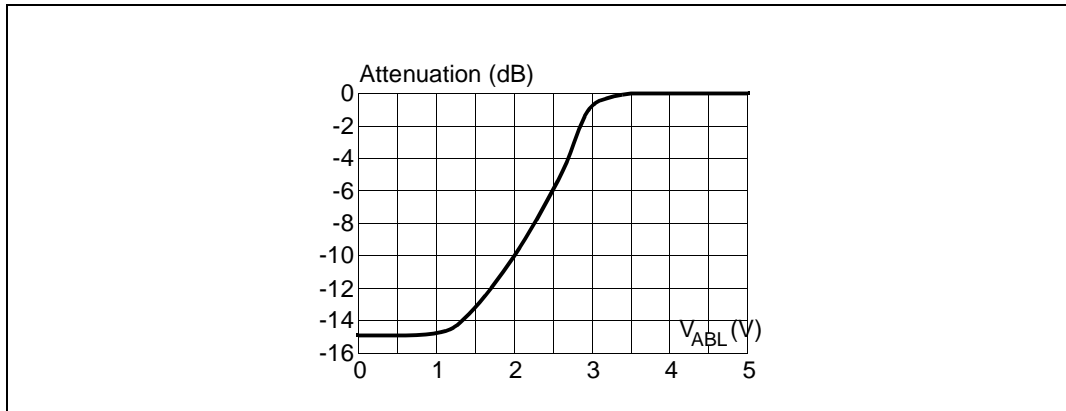
## 2.9 ABL Control

The STV9211 includes an ABL (automatic beam limitation) input to attenuate the RGB Video signals depending on the beam intensity.

The operating range is 2 V (from 3 V to 1 V). A typical 15 dB maximum attenuation is applied to the output signal whatever the contrast adjustment is. (See [Figure 9](#)).

When not used, the ABL input (Pin 2) must be connected to a 5 V supply voltage.

**Figure 9: ABL attenuation range**



## 2.10 OSD

### Principle

The STV9211 allows to mix the OSD signals into the RGB main picture. The four pins dedicated to this function are the following:

- Three TTL RGB inputs (Pins 8, 9, 10) connected to the three outputs of the corresponding OSD processor.
- One TTL fast blanking input (Pin 11) also connected to the FBLK output of the OSD processor.

When a high level is present on the FBLK, the IC acts as follows:

- The three main picture RGB input signals (IN1, IN2, IN3) are internally switched to an internal clamp reference voltage.
- The three output signals (OUT1, OUT2, OUT3) are set to the voltage corresponding to the three OSD input logic states (0 or 1). (See [Figure 2](#): Block diagram).

### Output level

If the OSD input is set to 0, the output is set to the black level (see [Figure 10](#)).

If the OSD input is at high level, the output voltage is set to: black-level +  $V_{OSD}$ , where  $V_{OSD}$  is the I<sup>2</sup>C bus-controlled voltage, adjustable between 0 V to 4.9 V by 306 mV steps via Register 7 (4 bits).

The same variation is applied simultaneously to the three channels providing the OSD contrast.

### Grey OSD

The STV9211 allows the display of grey OSD by programming the following conditions:

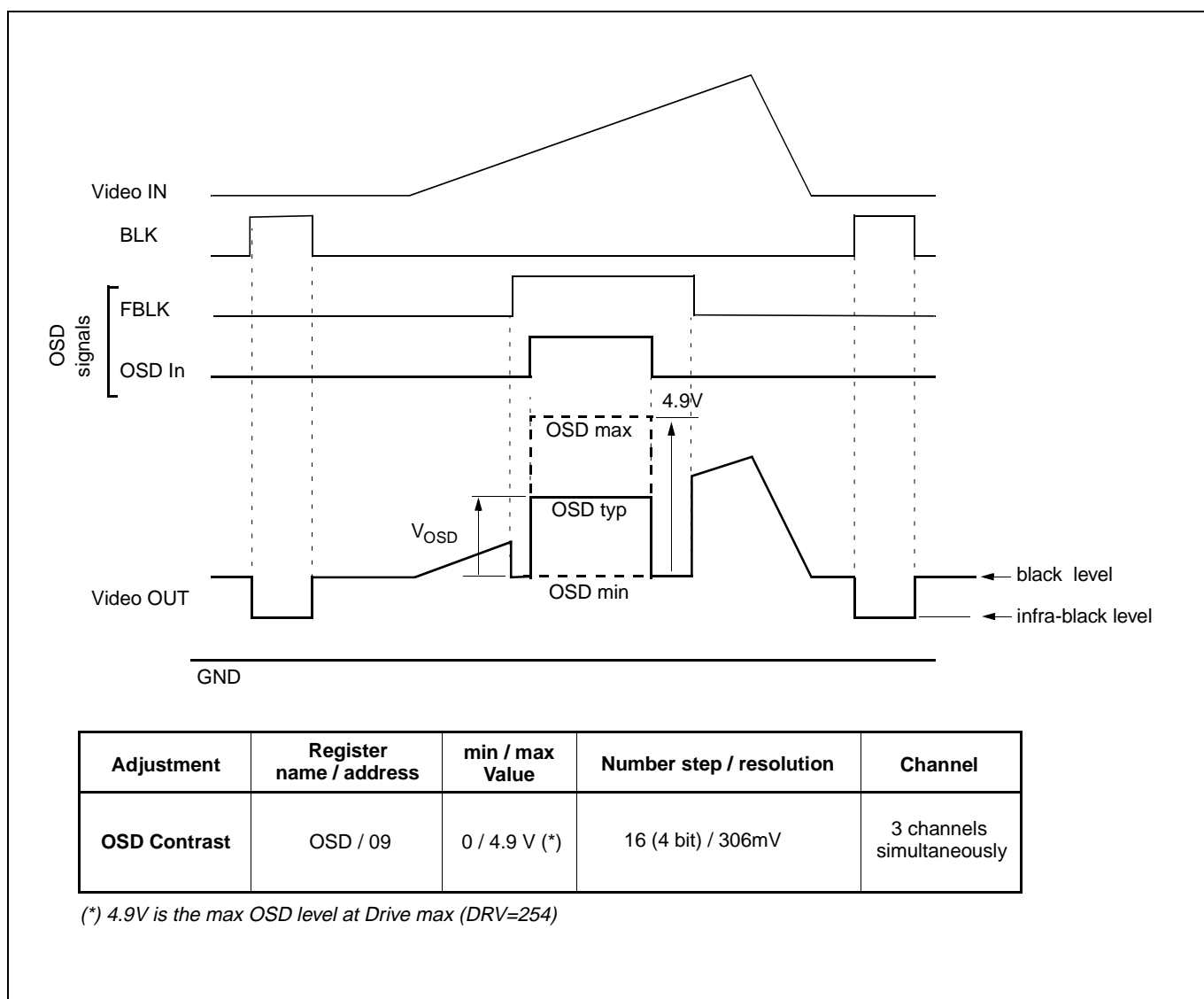
- OSD1 = 1, OSD2 = 0 and OSD3 = 1,
- Register 9, bit 5 or 6 = 1.

If Register 9, bit 5 =1: a light grey OSD is displayed.

If Register 9, bit 6 = 1: a dark grey OSD is displayed.

If Register 9, bit 5=0 and bit 6=0: a standard OSD is displayed.

Figure 10: OSD



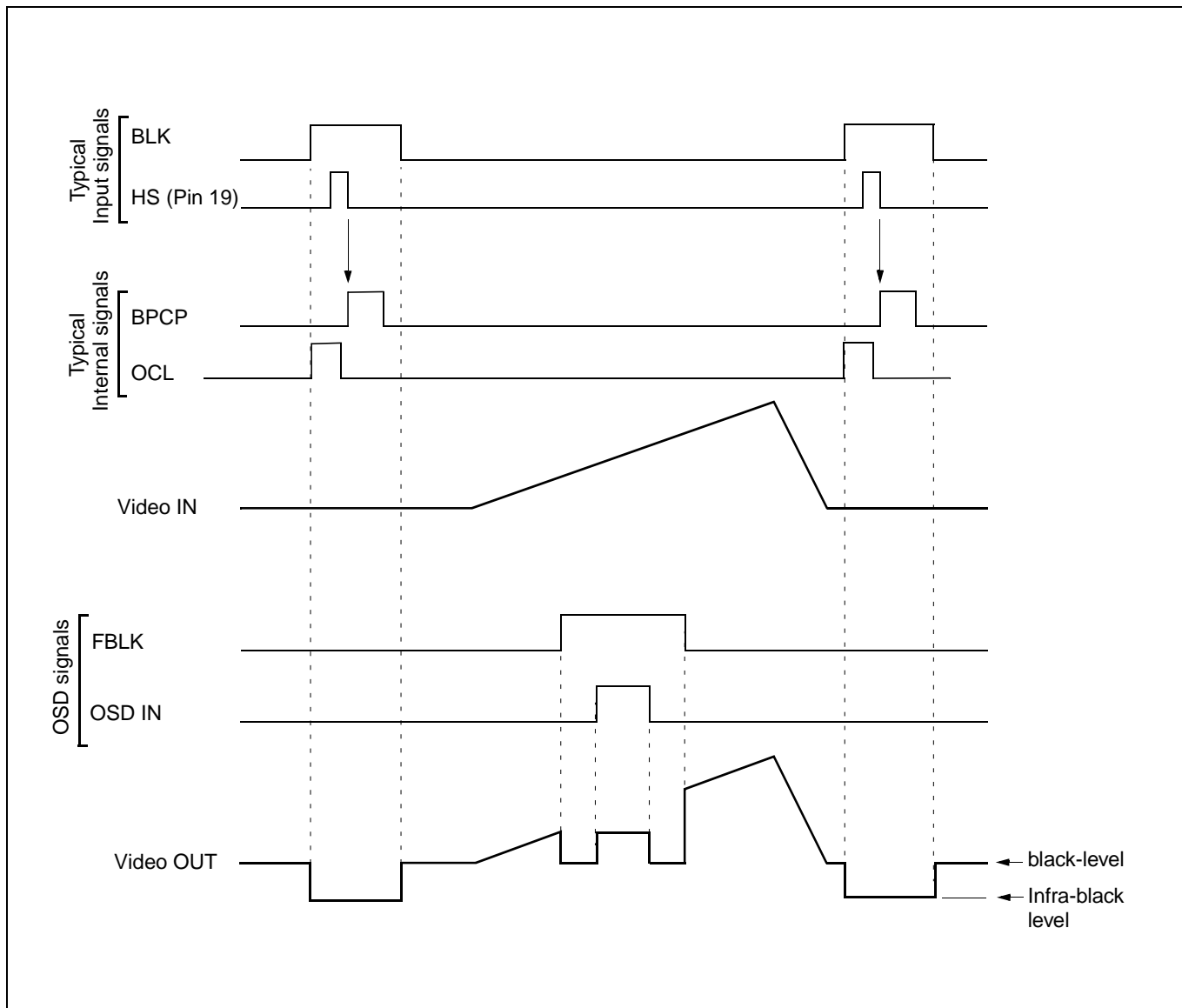
## 2.11 Output stage

The overall waveforms of the output signal are shown in *Figure 11*. The three output stages are large bandwidth output amplifiers able to deliver up to  $4.4 V_{PP}$  for  $0.7 V_{PP}$  video signal.

When a high level is applied on the BLK input (Pin 20), the three outputs are forced to “Infra Black” level (Vib) thanks to a sample and hold circuit (described below).

The black level is the output voltage outside the blanking pulse when no video input signal is available (see *Figure 11*).

Figure 11: Signal waveforms





## 2.12 Preamplifier bandwidth adjustment (4 bits)

An advanced feature: preamplifier bandwidth adjustment (BW: Register 13, see I<sup>2</sup>C table 5), is implemented on the STV9211.

The programming of this BW register is very important to get good video performances.

It must not be set its maximum value. With the following values, the optimum performances are obtained.

$t_R/t_F$	Preamplifier bandwidth register: BW	
	Binary	Decimal
$5.5 \pm 1$ ns	1000	8
$7.5 \pm 1$ ns	0101	5
$9.5 \pm 1$ ns	0010	2
10 ns and below	0000	0

For applications where rise/fall time <5.5ns, this feature offers several advantages:

- Slew-rate: depending on the external capacitive load and on the peak-to-peak output voltage, this adjustment avoids getting any slew-rate phenomenon.
- Electromagnetic radiation (EMI): slowing down the signal of rise/fall time will decrease the EMI without significantly deteriorating the rise/fall time of the CRT driver.
- Video signal response: using this adjustment will allow to optimize the high frequency transient phenomenons.
- Picture boost mode: when displaying still pictures or moving video, having high video swing can be of greater interest than rise/fall time. The preamplifier bandwidth adjustment can be used to avoid any slew-rate phenomenon at the CRT driver output.

## 2.13 Amplifier bandwidth adjustment (7 bits)

The STV9211 can adjust the bandwidth of any ST video amplifier having a dedicated control pin (CTL). The adjustment is done by I<sup>2</sup>C via Register 6 (see I<sup>2</sup>C table 2).

If not used, the AMPCTL pin must be connected to ground.

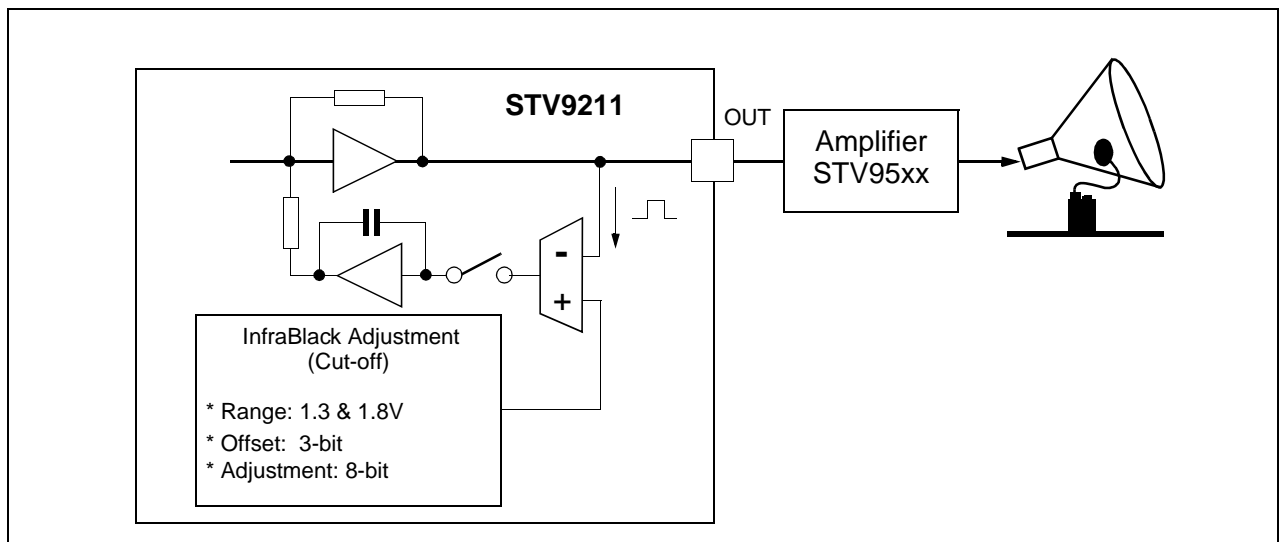
## 2.14 CRT cathode, DC-coupling mode (Figure 12)

The STV9211 can be used in DC coupling mode only.

The cut-off (InfraBlack) adjustment is done by the preamplifier.

The infra-black level ( $V_{ib}$ ) is adjusted independently for each channel via the Registers 10, 11 and 12 (see the complete description in [Section 2.10](#)).

Figure 12: DC-coupling mode



## 2.15 Preamplifier stand-by mode

The STV9211 is set in stand-by mode either by  $I^2C$  or by decreasing the  $V_{CCP}$  supply voltage.

- $I^2C$ : the STV9211 is in stand-by mode when Register 13, bit 7=1
- $V_{CCP}$ : the STV9211 is in stand-by mode when  $V_{CCP} < 3$  V

In stand-by mode, the analog blocks are internally switched-off while the logic parts ( $I^2C$  bus and power-on reset) are still supplied.

The power consumption is below 20mW.

## 2.16 Amplifier stand-by mode

The STV9211 can set in stand-by mode any ST video amplifier with the CTL control pin.

When Register 9, bit 7=1, the AMPCTL pin is switched to low level ( $< 0.3V$ ). The amplifier is set in stand-by mode when  $CTL < 0.3V$ .

If not used, the AMPCTL pin must be connected to ground.

## 2.17 Serial interface

The 2-wire serial interface is an I<sup>2</sup>C interface. The slave address of the STV9211 is DC hex.

A6	A5	A4	A3	A2	A1	A0	W
1	1	0	1	1	1	0	0

The host MCU can write into the STV9211 Registers. Read mode is not available.

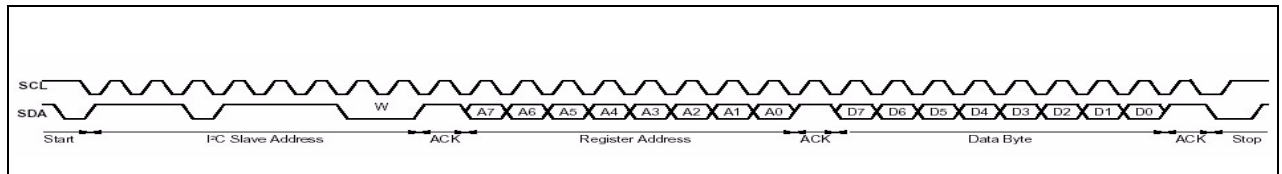
In order to write data into the STV9211, after the “start” message, the MCU must send the following data (see [Figure 13](#)):

- the I<sup>2</sup>C address slave byte with a low level for the R/W bit,
- the byte to the internal Register address where the MCU wants to write data,
- the data.

All bytes are sent with MSB bit first. The transfer of written data is ended with a “stop” message.

When transmitting several data, the Register addresses and data can be written with no need to repeat the start and slave addresses.

**Figure 13: I<sup>2</sup>C write operation**



## 2.18 Power-on reset

A power-on reset function is implemented on the STV9211 so that the I<sup>2</sup>C registers have a determined status after power-on. The Power-on reset threshold for a rising supply on V<sub>CCA</sub> (Pin 7) is 3.8 V (typ.) and 3.2V when the V<sub>CC</sub> decreases.

## 2.19 Specific application conditions

- **Functioning with  $V_{CCP}$  below 8 V**

To simplify the application, it is possible to supply the power  $V_{CCP}$  with 5 V (instead of 8 V nominal) at the expense of output swing voltage. The CRT Heater voltage (6.2V Typ.) is used very often to supply  $V_{CCP}$ .

- **Functioning without blanking pulse**

If no blanking pulse is applied to the STV9211, it is necessary to ensure the OCL pulse generation (which sets the infra-black level) by setting the Register 8, bit7=1 (OCL = BPCP).

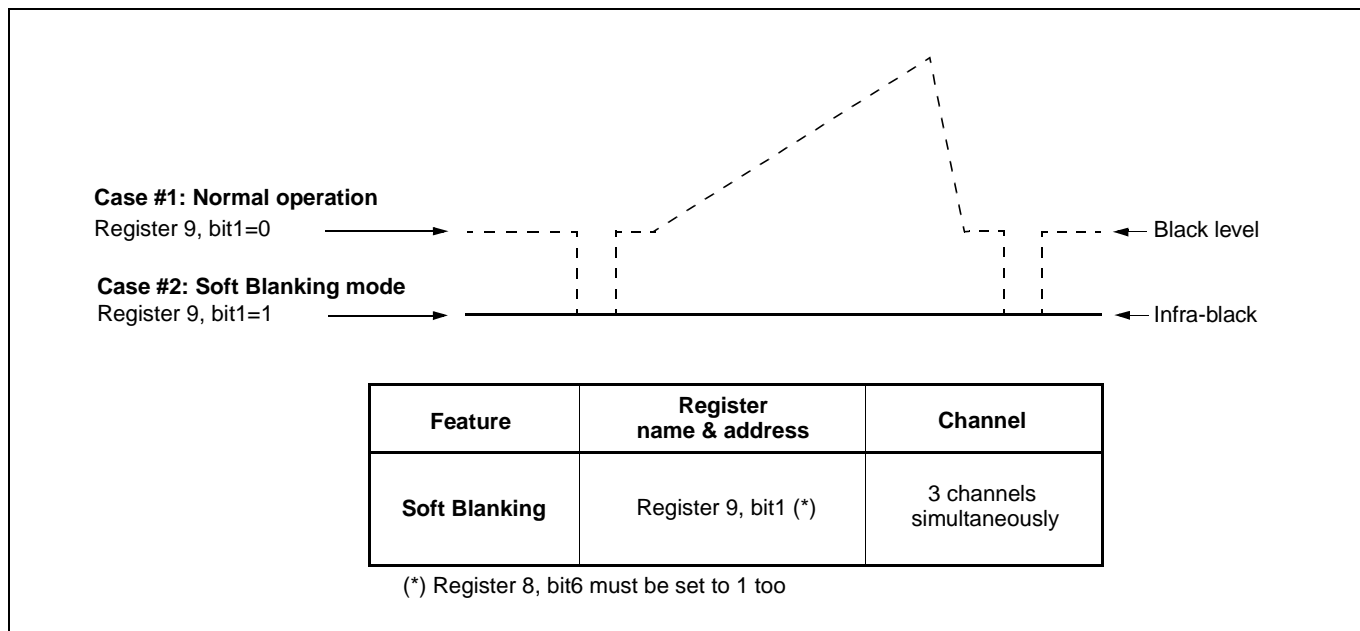
To ensure the device correct behavior in the worst possible conditions, the brightness Register must be set to 0.

- **Soft blanking**

It is possible to blank the video signal by setting the Register 9, bit1=1 and Register 8, bit6=1.

In this mode the output voltage is set to  $V_{ib}$  (see [Figure 14](#)). This mode is used for example when changing the timing resolution of the video, in order to suppress the video during this transient period.

Figure 14: Soft blanking



### 3 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Pin	Value	Units
$V_{CCA}$	Supply Voltage on Analog $V_{CC}$	7	5.5	V
$V_{CCP}$	Supply Voltage on Power $V_{CC}$	20	8.8	V
$V_{in}$	Voltage at any Input Pins (except Video inputs) and Input/Output Pins	-	5.5	V
$V_I$	Voltage at Video Inputs	1, 3, 5	1.4	V
$V_{ESD}$	ESD susceptibility Human Body Model (100pF discharge through 1.5k $\Omega$ )	All	2	kV
$T_{stg}$	Storage Temperature	-	-	$^{\circ}\text{C}$
$T_{oper}$	Operating Junction Temperature	-	+150	$^{\circ}\text{C}$

### 4 THERMAL DATA

Symbol	Parameter	Value	Units
$R_{th(j-a)}$	Max. Junction-ambient Thermal Resistance	69	$^{\circ}\text{C}/\text{W}$
$T_j$	Typ. Junction Temperature at $T_{amb} = 25^{\circ}\text{C}$	80	$^{\circ}\text{C}$

## 5 DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CCA} = 5\text{V}$ ,  $V_{CCP} = 8\text{V}$ , unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
<b>SUPPLY</b>						
$V_{CCA}$	Analog Supply Voltage	Pin 7	4.5	5	5.5	V
$V_{CCP}$	Power Supply Voltage	Pin 17	4.5	8	8.8	V
$V_{CCPS}$	Power Supply Voltage stand-by threshold	Pin 17	2.5	3.0	3.5	V
$I_{CCA}$	Analog Supply Current	$V_{CCA} = 5\text{V}$		70		mA
$I_{CCP}$	Power Supply Current	$V_{CCP} = 8\text{V}$		55		mA
$I_S$	Total Supply Current in stand-by mode	Pin 17 and pin 7	-	-	5	mA
<b>INPUTS, OUTPUTS</b>						
$V_I$	Video Input Voltage Amplitude			0.7	1	V
$V_O$	Output Voltage Range		0.5 <i>Note 1</i>		$V_{CCP}$ -0.5V	V
$V_{IL}$ $V_{IH}$	Low Level Input Voltage High Level Input Voltage	OSD, FBLK, BLK, HS	2.4		0.8	V V
$I_{IN}$	Input Current	OSD, FBLK, BLK	-1		1	$\mu\text{A}$
$R_{HS}$	Input Resistor	HS		40		$\text{k}\Omega$
AMPCTL1	Amplifier standby threshold	Pin 4 @ Register 9, bit 7 = 1 and $I_{4\text{sink}} = 200\mu\text{A}$		80	300	mV
AMPCTL2	Amplifier operating range	Pin 4 @ Register 9, bit 7 = 0 and $I_{4\text{sink}} = 200\mu\text{A}$  Register 6, bit 4 to bit 7=0000  Register 6, bit 4 to bit 7=1111		0.7 4.5		V V

## 6 AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CCA} = 5\text{V}$ ,  $V_{CCP} = 8\text{V}$ ,  $V_i = 0.7 V_{PP}$ ,  $C_{LOAD} = 5\text{pF}$

$R_S = 100\Omega$ , serial between output pin and  $C_{LOAD}$ , unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
<b>VIDEO OUTPUT SIGNAL (pins 14, 16, 18) - CONTRAST AND DRIVE</b>						
G	Maximum gain	Max Contrast and Drive (CRT = DRV = 254 dec)		16		dB
VOM	Maximum video output voltage (Note 1)	Max Contrast and Drive (CRT = DRV = 254 dec)		4.4		V
VON	Nominal video output voltage	Contrast and Drive at POR (CRT = DRV = 180 dec)		2.2		V
CAR	Contrast attenuation range	From max. Contrast (CRT=254 dec) to min. Contrast (CRT = 1 dec)		48		dB
DAR	Drive attenuation range	From Max. Drive (DRV = 254 dec) to min. Drive (DRV = 1 dec)		48		dB
GM	Gain matching (Note 3)	Contrast and Drive at POR		±0.1		dB
<b>VIDEO OUTPUT SIGNAL (pins 14, 16, 18) - BRIGHTNESS</b>						
BRTmax	Maximum brightness level	Max. Brightness (BRT = 255 dec) and Max. Drive (DRV = 254 dec)		2		V
BRT min	Minimum brightness level	Min. Brightness (BRT = 0 dec) and Max. Drive (DRV = 254 dec)		0		V
VIP	Insertion pulse	(Note 4)		0.4		V
BRTM	Brightness matching (Note 3)	Brightness and Drive at POR		±10		mV
<b>VIDEO OUTPUT SIGNAL - OSD</b>						
VOSDmax	Maximum OSD output level	Max. Drive (DRV = 254 dec) Max. OSD (OSD = 15 dec)		4.9		V
VOSD min	Minimum OSD output level	Min. OSD (OSD = 0 dec)		0		V
<b>VIDEO OUTPUT SIGNAL - INFRA BLACK LEVEL (Figure 8)</b>						
Vib0 max	Maximum infrablack level	IBR=0 and IBL=0 Max. Vib (IBL = 255 dec)		2.2		V
Vib0 min	Minimum infrablack level	Min. Vib (IBL = 0 dec)		0.4		V
Vib1 max	Maximum infrablack level	IBR=1 and IBL=0 Max. Vib (IBL = 255 dec)		1.7		V
Vib1 min.	Minimum infrablack level	Min. Vib (IBL = 0 dec)		0.4		V
Vib step 0	Infrablack level step	IBR=0 (Note 5)		7		mV
Vib step 1	Infrablack level step	IBR=1 (Note 5)		5		mV
<b>ABL (Pin 2)</b>						
GABLmin	ABL mini attenuation	$V_{ABL} \geq 3.2\text{V}$			0	dB
GABL max	ABL maxi attenuation	$V_{ABL} = 1\text{V}$			15	dB
$V_{ABL}$	ABL threshold voltage	For output attenuation			3	V
IABL high	High ABL input current	$V_{ABL} = 3.2\text{V}$			0	µA
IABLI ow	Low ABL input current	$V_{ABL} = 1\text{V}$			-2	µA
<b>VIDEO OUTPUT SIGNAL - DYNAMIC PERFORMANCES (Figure 9)</b>						
$t_R, t_F$	Rise Time, Fall Time (Note 6)	$V_{OUT} = 2 V_{PP}$ (BW = 15 dec) $V_{OUT} = 2 V_{PP}$ (BW = 0 dec)		2.7 5		ns
BW	Large Signal Bandwidth	$V_{OUT} = 2 V_{PP}$		130		MHz
BW	Bandwidth Adjustment Range	$V_{OUT} = 2 V_{PP}$ Minimum bandwidth (BW = 0 dec) Maximum bandwidth (BW = 15 dec)		70 130		MHz MHz
CT	Crosstalk between Video Outputs	$V_{OUT} = 2 V_{PP}$ @ $f = 10\text{MHz}$ @ $f = 50\text{MHz}$		60 35		dB dB

## Notes about electrical characteristics

- Note: 1 The video on the preamplifier output must remain above 0.5V even for high frequency signals.
- 2 Assuming that the video output signal remains inside the linear area of the preamplifier output (between 0.5V and  $V_{CCP} - 0.5V$ )
- 3 Matching measured between the different outputs
- 4 The VIP insertion pulse is present only in "brightness before drive" mode (see [Figure 7](#))
- 5 In kit with the STV95xx amplifier, this 7/5 mV step resolution offers a 100/140mV resolution at the amplifier output
- 6  $t_R$ ,  $t_F$  are calculated values, assuming an ideal input signal with rise/fall time = 0ns



## 7 I<sup>2</sup>C ELECTRICAL CHARACTERISTICS

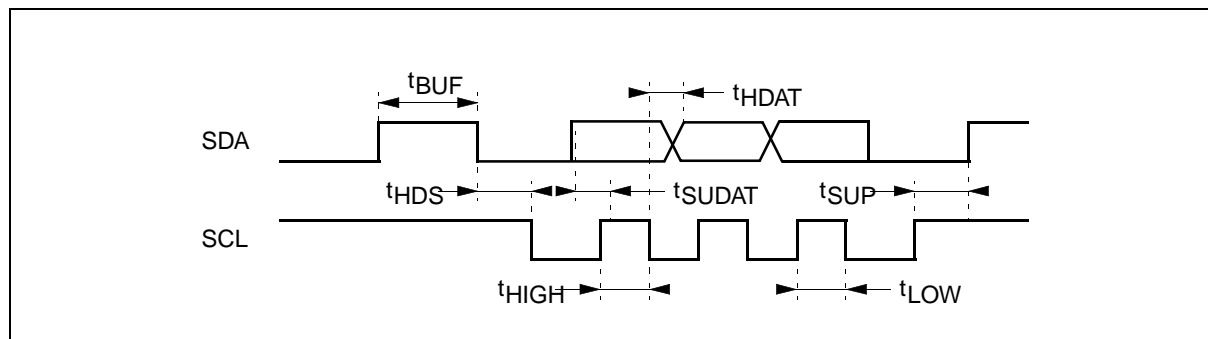
$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CCA} = 5\text{V}$ ,  $V_{CCP} = 8\text{V}$ ,  $V_i = 0.7 V_{PP}$ ,  $C_{LOAD} = 5\text{pF}$

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
$V_{IL}$	Low Level Input Voltage	On Pins SDA, SCL			1.5	V
$V_{IH}$	High Level Input Voltage		3			V
$I_{IN}$	Input Current (Pins SDA, SCL)	$0.4\text{ V} < V_{IN} < 4.5\text{ V}$	-10		+10	$\mu\text{A}$
$f_{SCL(\text{Max.})}$	SCL Maximum Clock Frequency		0.25		200	kHz
$V_{OL}$	Low Level Output Voltage	SDA Pin when ACK Sink Current = 6mA			0.6	V

## 8 I<sup>2</sup>C INTERFACE TIMING REQUIREMENTS

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{BUF}$	Time the bus must be free between two accesses			1300	ns
$t_{HDS}$	Hold Time for Start Condition			600	ns
$t_{SUP}$	Set-up Time for Stop Condition			600	ns
$t_{LOW}$	The Low Period of Clock			1300	ns
$t_{HIGH}$	The High Period of Clock			600	ns
$t_{HDAT}$	Hold Time Data			300	ns
$t_{SUDAT}$	Set-up Time Data			250	ns
$t_R, t_F$	Rise and Fall Time of both SDA and SCL			20	ns

Figure 15: I<sup>2</sup>C timing diagram



## 9 I<sup>2</sup>C REGISTER DESCRIPTION

Table 2: Register sub-addressed - I2C table 1

Sub-address		Register Names		POR Value		Max. Value	
Hex	Dec			Hex	Dec	Hex	Dec
01	01	Contrast (CRT) - <i>Note 1</i>	8-bit DAC	B4	180	FE	254
02	02	Brightness (BRT)	8-bit DAC	B4	180	FF	255
03	03	Drive 1 (DRV) - <i>Note 1</i>	8-bit DAC	B4	180	FE	254
04	04	Drive 2 (DRV) - <i>Note 1</i>	8-bit DAC	B4	180	FE	254
05	05	Drive 3 (DRV) - <i>Note 1</i>	8-bit DAC	B4	180	FE	254
06	06	Amplifier control	refer to I <sup>2</sup> C table 2	99	153	-	-
07	07	OSD Contrast (OSD)	4-bit DAC	09	09	0F	15
08	08	BPCP & OCL	Refer to I <sup>2</sup> C table 3	04	04		
09	09	Miscellaneous	Refer to I <sup>2</sup> C table 4	1C	28		
0A	10	Out 1- Infra-black level: IBL1	8-bit DAC	B4	180	FF	255
0B	11	Out 2- Infra-black level: IBL2	8-bit DAC	B4	180	FF	255
0C	12	Out 3- Infra-black level: IBL3	8-bit DAC	B4	180	FF	255
0D	13	Preamplifier Bandwidth Adjustment (BW) - <i>Note 2</i>	4-bit DAC - I <sup>2</sup> C table 5	07	07	0F	15
0E	14	InfraBlack range and offset selection	Refer to I <sup>2</sup> C table 6				

Table 3: Amplifier bandwidth adjustment register (R6) - I2C table 2

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR value
0	0	0	0	0	0	0	0	Min. amplifier bandwidth	
1	0	0	1	0	0	0	0	Typ. amplifier bandwidth	x
1	1	1	1	0	0	0	0	Max. amplifier bandwidth	

Table 4: BPCP &amp; OCL register (R8) - I2C table 3

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR value
			0			0	0	Internal BPCP triggered by HS (trailing edge)	x
			0			1	0	Internal BPCP triggered by HS (leading edge)	
			0			0	1	Internal BPCP synchronized by BLK (leading edge)	x
			0			1	1	Internal BPCP synchronized by BLK (trailing edge)	
			0	0	0			Internal BPCP Width = 0.33 $\mu$ s	
			0	0	1			Internal BPCP Width = 0.66 $\mu$ s	x
			0	1	0			Internal BPCP Width = 1 $\mu$ s	
			0	1	1			Internal BPCP Width = 1.33 $\mu$ s	
			1					Internal BPCP = BPCP input	
		0						Normal Operation	x
		1						Reserved (Force BPCP to 1 in test)	
	0							Normal Operation	x
	1							Reserved (Force OCL to 1 in test)	
0								Internal OCL pulse triggered by BLK	x
1								Internal OCL pulse = Internal BPCP	

Table 5: Miscellaneous register (R9) - I<sup>2</sup>C table 4

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR value
							0	Positive Blanking Polarity	x
							1	Negative Blanking Polarity	
						0		Soft Blanking = OFF	x
						1		Soft Blanking = ON ( <a href="#">Note 3</a> )	
			0					Reserved (Test mode, very low bandwidth)	
			1					Normal operation	x
	0	0						Light Grey on OSD Outputs = OFF	x
	0	1						Light Grey on OSD Outputs = ON	
	0	0						Dark Grey on OSD Outputs = OFF	x
	1	0						Dark Grey on OSD Outputs = ON	
0								Amplifier stand-by = OFF	x
1								Amplifier stand-by = ON	

Table 6: Pre-amplifier bandwidth adjustment (R13) - I<sup>2</sup>C table 5

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR value
				1	1	1	1	130 MHz (Note 2)	
				0	1	1	1	100 MHz (Note 2)	x
				0	0	0	0	70 MHz (Note 2)	
		0	0					Normal operation	x
		0	1					Reserved (test mode - BW DAC output connected to BLK input)	
		1	0					Reserved (test mode - BW DAC complementary output connected to BLK input)	
	0							Brightness before drive	x
	1							Brightness after drive	
0								Pre-amplifier stand-by = OFF	x
1								Pre-amplifier stand-by = ON	

Table 7: Cut-off range and offset selection (R14) - I<sup>2</sup>C table 6 - see Figure 8

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR value
-	-	-	-	-	-	-	0	Infra-black range (IBR) = 1.8V	
-	-	-	-	-	-	-	1	Infra-black range (IBR) = 1.3V	x
-	-	-	-	0	0	0	-	Infra-black offset (IB0)- Min. value = 0.4V @ IBL = 0	
-	-	-	-	1	0	0	-	Infra-black offset (IB0)- Typ. value = 1.3V @ IBL = 0	x
-	-	-	-	1	1	1	-	Infra-black offset (IB0)- Max. value = 2.2V @ IBL = 0	

## Notes about I<sup>2</sup>C register description

Note: 1 For contrast & drive adjustment, code 00 (dec) and 255 (dec) are not allowed.

2 This register has to be set with the following values:

t <sub>R</sub> /t <sub>F</sub>	Pre-amplifier bandwidth register: BW	
	Binary	Decimal
5.5 ± 1 ns	1000	8
7.5 ± 1ns	0101	5
9.5 ± 1ns	0010	2
10 ns and below	0000	0

3 to set the device in soft blanking mode, it is necessary to program also Register 8, bit 6 = 1

## 10 STV9211 + STV9556/55/53 APPLICATIONS HINTS

### 10.1 InfraBlack adjustment procedure (Cut-off)

The STV9211 allows to adjust independantly the InfraBlack levels of the 3 video outputs with a high resolution. This ajustment is done via the **3 infra-black level registers (IBL1, IBL2 and IBL3)**. In order to have the optimum resolution, it is necessary, first, to set the video signal inside the linear area of the amplifier, by programing the **infra-black range register IBR** (26 or 36V) and the **infra-black offset register IBO**.

#### Step 1

Setting of the **infra-black range register IBR** (Register 14, bit 0. See I<sup>2</sup>C table 6). This register must be selected, either to 1.3V to get a 26V Cut-off adjustment range with the STV95xx amplifier or to 1.8V to get a 36V range (see [Figure 16](#))

#### Step 2

Setting of the **Infra-black offset register IBO** (Register 14, bit 1, 2 & 3. See I<sup>2</sup>C table 6). This register selects the Vib Offset. It allows to keep the video signal inside the linearity area of the amplifier.

The register value depends on the amplifier high voltage supply (Vdd).

In kit with the STV95xx amplifier family, we recommend the following programming:

**Table 8: Setting of the infra-black offset register (IBO)**

Vdd ( $\pm 5\%$ )	Case 1: Brightness before Drive		Case 2: Brightness after Drive	
	Binary	Decimal	Binary	Decimal
112 to 115V	001	1	011	3
107 to 111V	010	2	100	4
102 to 106V	011	3	101	5
97 to 101V	100	4	110	6
92 to 96V	101	5	111	7
88 to 91	110	6	111	7
87 and below	111	7	111	7

Example:

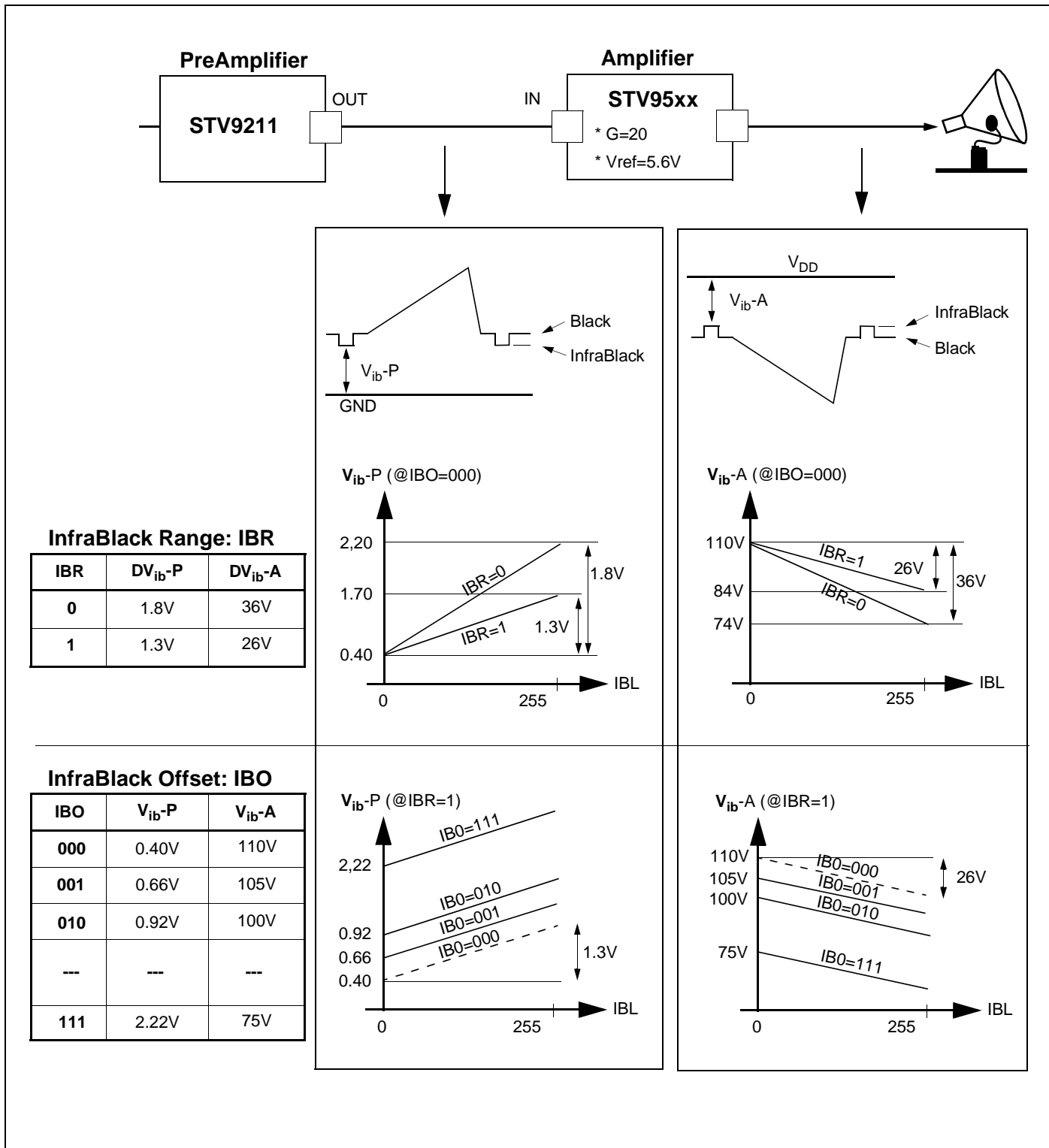
For Vdd=101V +/-5% and Brightness before Drive, IBO must be set to 100.

**Step 3**

Adjustment of the **InfraBlack level register IBL** (Register 10, 11, 12. See I<sup>2</sup>C table 1).

These three 8 bit- registers adjust separately the infra-black level of the 3 outputs with a high resolution (100mV at 26V range or 140mV at 36V range).

**Figure 16: STV9211 and STV95xx - Cut-off adjustment**



## 10.2 Preamplifier bandwidth register

The preamplifier bandwidth must not be set to maximum.

To get the optimum video performances and reduce the EMI, we recommend to use the values from [Section 2.12](#).

## 10.3 Preamplifier output network

The choice of the network between the STV9211 video outputs and the STV95XX amplifier is important. We recommend to use the network described in the application note AN1510.

## 10.4 White balance adjustment

The white balance adjustment on a DC-coupling video system and an AC-coupling video system differs.

Please, use our application note referenced AN1490 for the complete description of the white balance procedure.

# 11 INTERNAL SCHEMATICS

Figure 17:

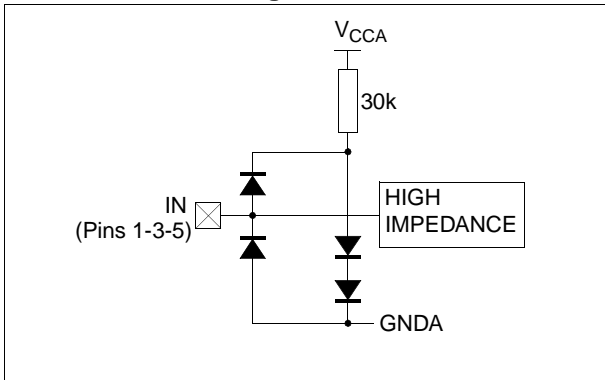


Figure 18:

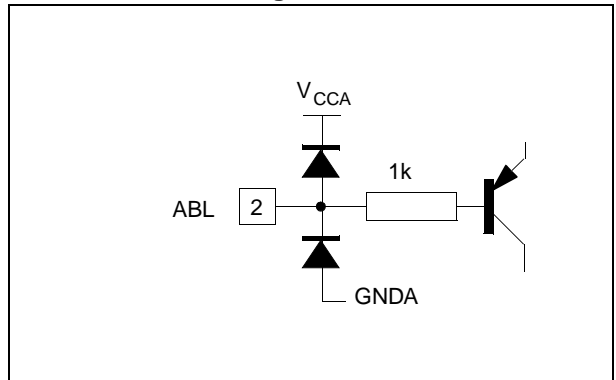


Figure 19: Pin 4

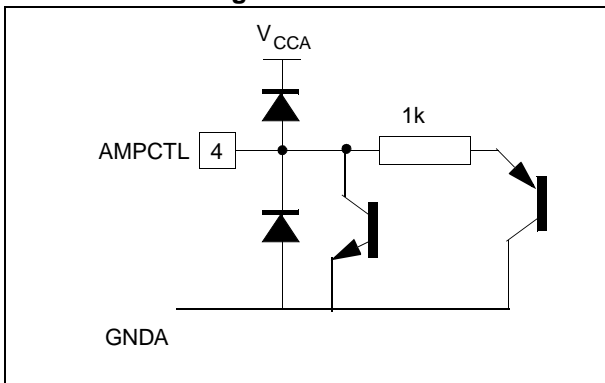


Figure 20:

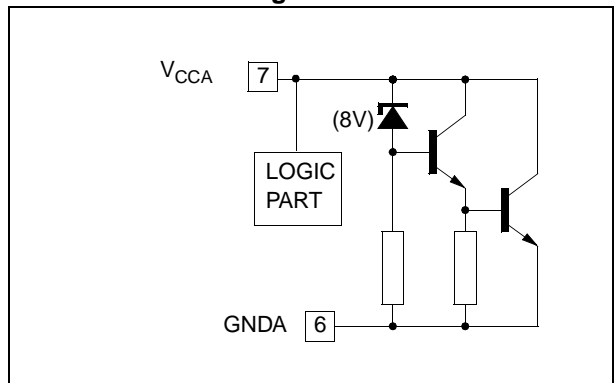


Figure 21:

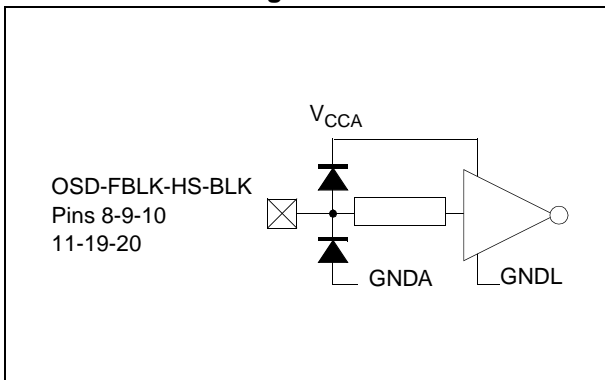


Figure 22:

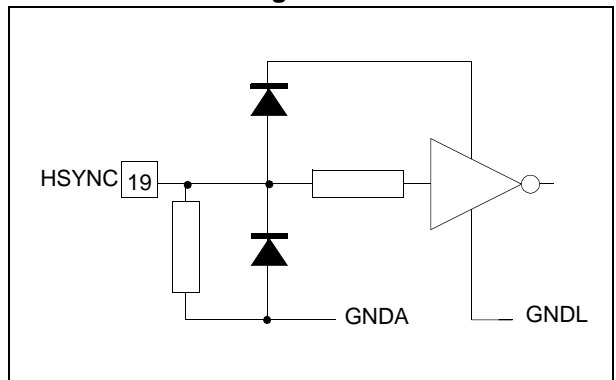


Figure 23:

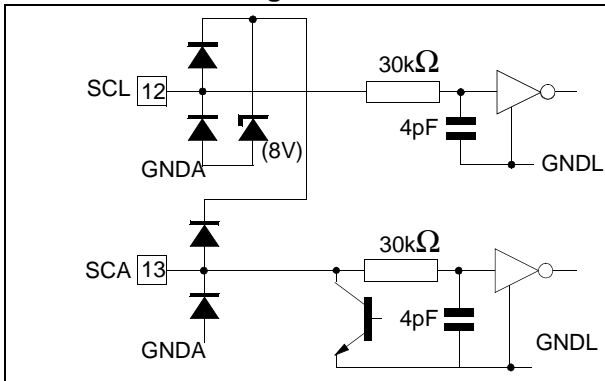


Figure 24:

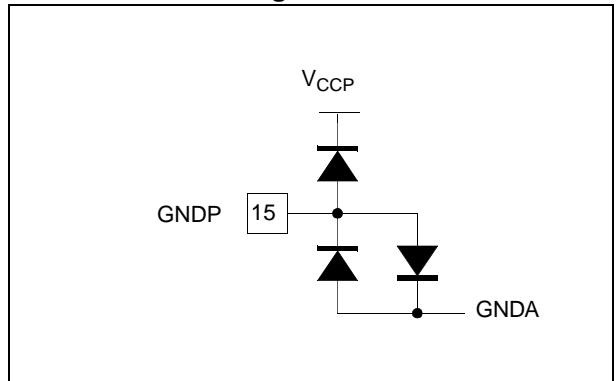
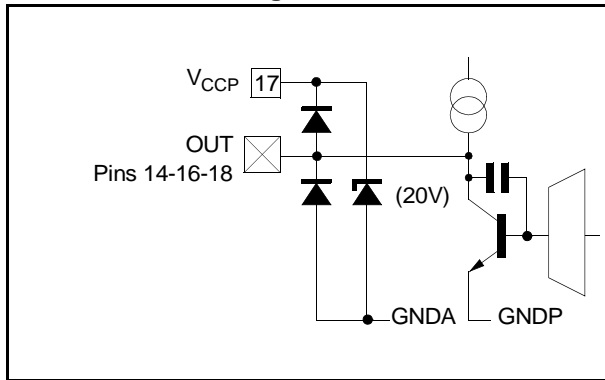




Figure 25:



## 12 DEMONSTRATION BOARDS

Figure 26: STV9211 + STV9556/55/53 + STV9936S/P demonstration board schematic

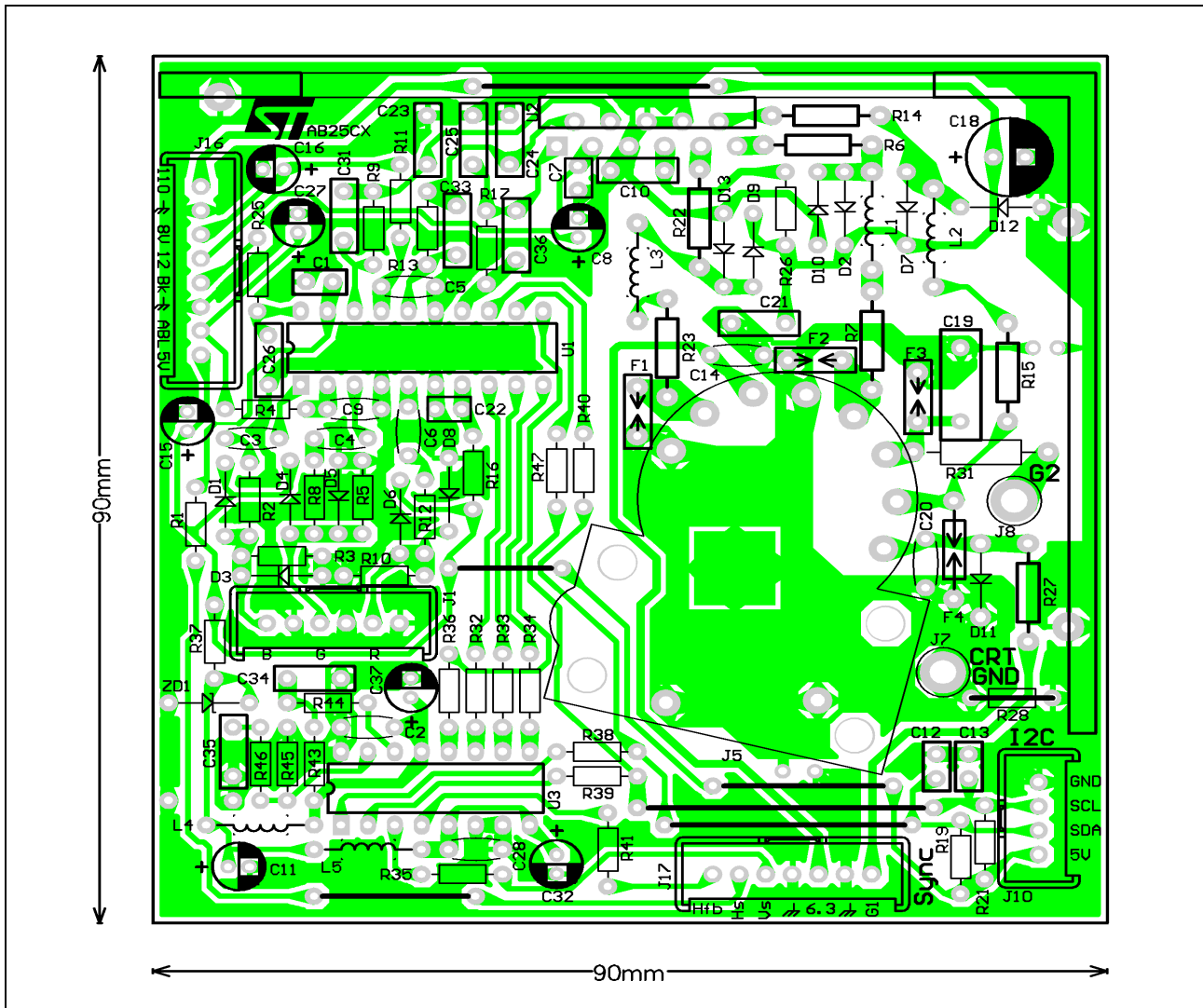
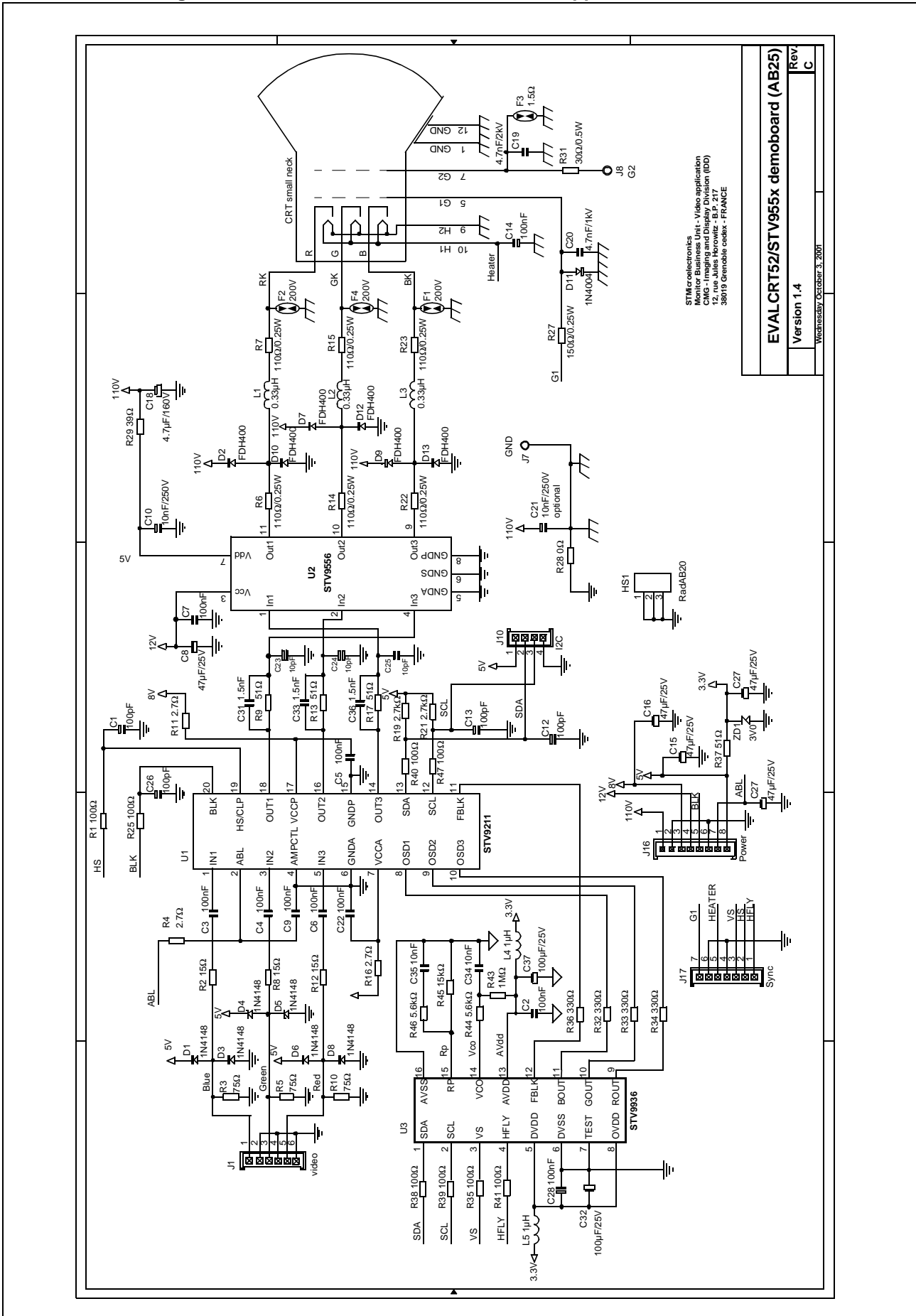


Figure 27: STV9211 - STV9556 - STV9936S/P application schematic

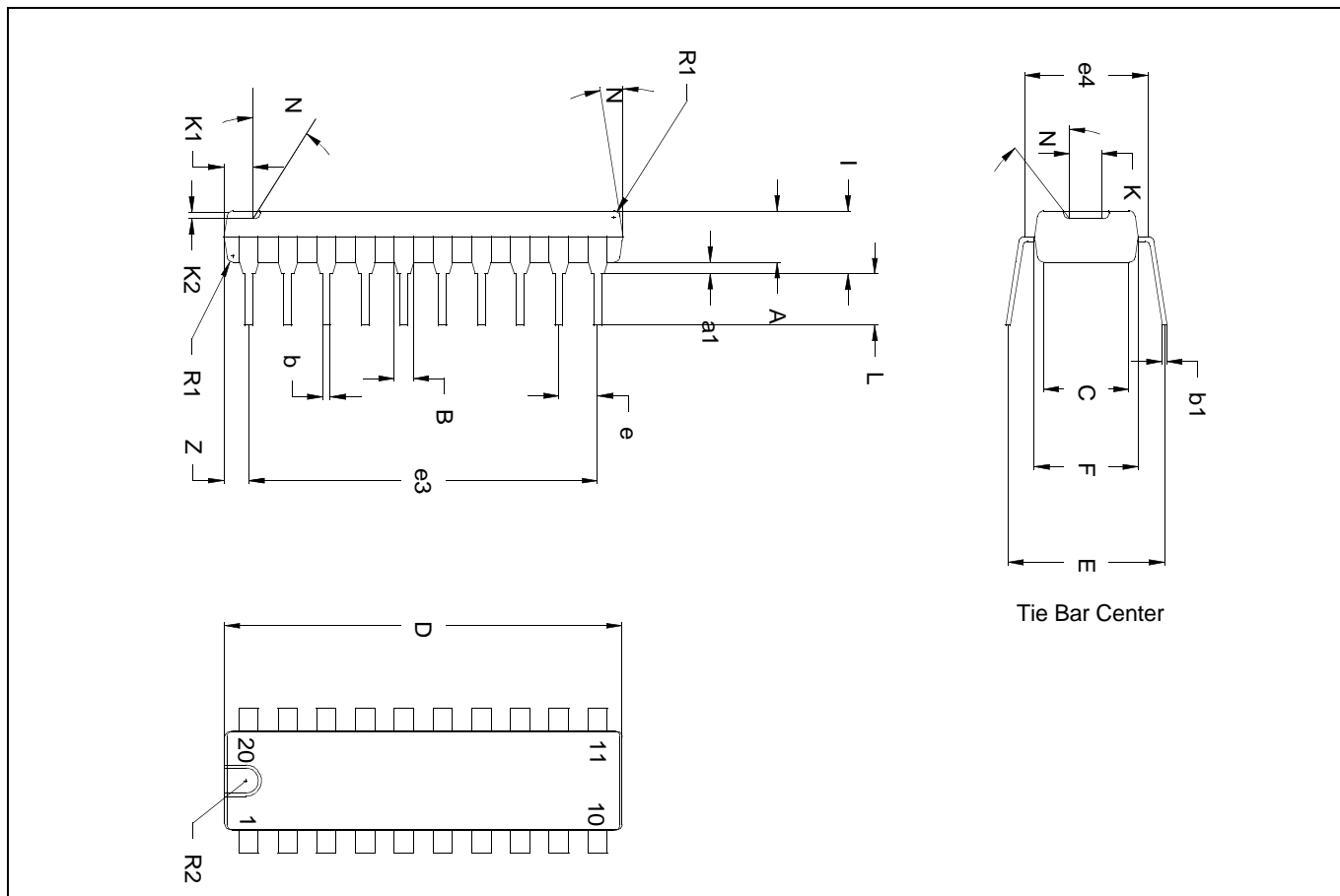


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<b>EVAL CRT52/STV955x demoboard (AB25)</b>	
Version 1.4	Rev C
Wednesday October 3, 2001	

# 13 PACKAGE MECHANICAL DATA

Figure 28: 20 pins - plastic dip



Dimensions	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.25	3.30	3.35	0.128	0.130	0.132
a1		0.508			0.020	
B	1.39		1.65	0.055		0.065
b	0.381	0.457	0.533	0.015	0.018	0.021
b1	0.20	0.254	0.30	0.008	0.010	0.012
C	5.20	5.33	5.46	0.205	0.210	0.215
D	24.9	25.15	25.4	0.980	0.990	1.000
E	7.8	8.5	9.1	0.307	0.335	0.358
e	2.29	2.54	2.79	0.090	0.100	0.110
e3	22.60	22.86	23.11	0.890	0.900	0.910
e4	7.36	7.62	7.87	0.290	0.300	0.310
F	6.22	6.35	6.50	0.245	0.250	0.255
I	3.42	3.68	3.93	0.135	0.145	0.155
L	3.17	3.30	3.42	0.125	0.130	0.135
N		7d			7d	
R1		0.152			0.006	
R2		0.762			0.030	
K		1.524			0.060	
K1		0.762			0.030	
K2		0.762			0.030	
Z		1.27	1.34		0.050	0.053

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