# **Triple Inverter with Open Drain Outputs**

The NL37WZ06 is a high performance triple inverter with open drain outputs operating from a 1.65 to 5.5 V supply.

The internal circuit is composed of multiple stages, including an open drain output which provides the capability to set output switching level. This allows the NL37WZ06 to be used to interface 5 V circuits to circuits of any voltage between  $V_{CC}$  and 7 V using an external resistor and power supply.

#### **Features**

- Extremely High Speed:  $t_{PD}$  2.5 ns (typical) at  $V_{CC} = 5 \text{ V}$
- Designed for 1.65 V to 5.5 V V<sub>CC</sub> Operation
- Over Voltage Tolerant Inputs
- LVTTL Compatible Interface Capability with 5 V TTL Logic with  $V_{CC} = 3 \text{ V}$
- LVCMOS Compatible
- 24 mA Output Sink Capability @ 3.0 V
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Chip Complexity: FET = 72
- Pb-Free Package is Available

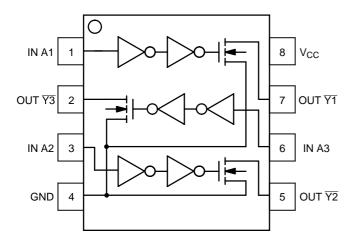


Figure 1. Pinout (Top View)

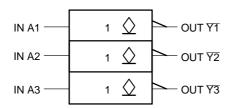
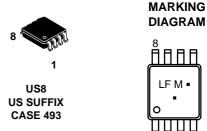


Figure 2. Logic Symbol



## ON Semiconductor®

http://onsemi.com



LF = Device Code
M = Date Code\*

Pb-Free Package

(Note: Microdot may be in either location)
\*Date Code orientation may vary depending upon manufacturing location.

#### **PIN ASSIGNMENT**

1	IN A1
2	OUT <del>Y</del> 3
3	IN A2
4	GND
5	OUT Y2
6	IN A3
7	OUT Y1
8	V <sub>CC</sub>
	- 00

#### **FUNCTION TABLE**

A Input	▼ Output
L	Z
Н	L

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

#### **MAXIMUM RATINGS**

Symbol	Parameter		Value	Unit
V <sub>CC</sub>	DC Supply Voltage	DC Supply Voltage		V
VI	DC Input Voltage		-0.5 to +7.0	V
Vo	DC Output Voltage		-0.5 to +7.0	V
I <sub>IK</sub>	DC Input Diode Current	V <sub>I</sub> < GND	-50	mA
I <sub>OK</sub>	DC Output Diode Current	V <sub>O</sub> < GND	-50	mA
Io	DC Output Sink Current		±50	mA
I <sub>CC</sub>	DC Supply Current per Supply F	Pin	±100	mA
I <sub>GND</sub>	DC Ground Current per Ground	Pin	±100	mA
T <sub>STG</sub>	Storage Temperature Range		-65 to +150	°C
TL	Lead Temperature, 1 mm from C	Case for 10 Seconds	260	°C
TJ	Junction Temperature under Bia	s	+150	°C
$\theta_{JA}$	Thermal Resistance	(Note 1)	250	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 8	85°C	250	mW
MSL	Moisture Sensitivity		Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.

- Tested to EIA/JESD22-A114-A.
   Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.

## **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parame	Min	Max	Unit	
V <sub>CC</sub>	Supply Voltage	Operating Data Retention Only	1.65 1.5	5.5 5.5	V
VI	Input Voltage	(Note 5)	0	5.5	V
Vo	Output Voltage	(HIGH or LOW State)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Free-Air Temperature		-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate	$V_{CC} = 2.5 \text{ V } \pm 0.2 \text{ V}$ $V_{CC} = 3.0 \text{ V } \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V } \pm 0.5 \text{ V}$	0 0 0	20 10 5	ns/V

<sup>5.</sup> Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

## DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	٦	T <sub>A</sub> = 25°C		-40°C ≤	Γ <sub>A</sub> ≤ 85°C	
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Unit
V <sub>IH</sub>	High-Level Input Voltage		1.65 2.3 to 5.5	0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub>			0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub>		V
V <sub>IL</sub>	Low-Level Input Voltage		1.65 2.3 to 5.5			0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub>		0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub>	V
I <sub>LKG</sub>	Z–State Output Leakage Current	$V_{IN} = V_{IL}$ $V_{OUT} = V_{CC}$ or GND	1.65 to 5.5			±5.0		±10.0	μΑ
V <sub>OL</sub>	Low-Level Output Volt-	I <sub>OL</sub> = 100 μA	1.65 to 5.5			0.1		0.1	V
	age V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 4 mA	1.65			0.45		0.45	]
		I <sub>OL</sub> = 8 mA	2.3		0.22	0.3		0.3	]
		I <sub>OL</sub> = 12 mA	2.7		0.22	0.4		0.4	]
		I <sub>OL</sub> = 16 mA	3.0		0.28	0.4		0.4	
		I <sub>OL</sub> = 24 mA	3.0		0.38	0.55		0.55	]
		I <sub>OL</sub> = 32 mA	4.5		0.42	0.55		0.55	]
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> or V <sub>OUT</sub> = V <sub>CC</sub> or GND	0 to 5.5			±0.1		±1.0	μΑ
I <sub>OFF</sub>	Power Off–Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0			1.0		10	μΑ
Icc	Quiescent Supply Cur- rent	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			1.0		10	μΑ

## AC ELECTRICAL CHARACTERISTICS $t_R$ = $t_F$ = 2.5 ns; $C_L$ = 50 pF; $R_L$ = 500 $\Omega$

				T <sub>A</sub> = 25°C		$-40^{\circ}C \leq T_{A} \leq 85^{\circ}C$			
Symbol	Parameter	Condition	V <sub>CC</sub> (V)	Min	Тур	Max	Min	Max	Unit
t <sub>PZL</sub>	Propagation Delay	$R_{L} = R_1 = 500 \Omega, C_L = 50 pF$	$1.8 \pm 0.15$			7.2		7.2	ns
	(Figure 3 and 4)	$R_{L} = R_1 = 500 \Omega, C_L = 50 pF$	$2.5 \pm 0.2$	0.8	3.0	4.0	0.8	4.1	
		$R_{L} = R_1 = 500 \Omega, C_L = 50 pF$	$3.3 \pm 0.3$	0.8	2.4	3.2	0.8	3.7	
		$R_{L} = R_1 = 500 \Omega, C_L = 50 pF$	$5.0 \pm 0.5$	0.5	2.4	3.0	0.5	3.5	
t <sub>PLZ</sub>	Propagation Delay	$R_{L} = R_1 = 500 \Omega, C_L = 50 pF$	$1.8 \pm 0.15$			7.2		7.2	ns
	(Figure 3 and 4)	$R_{L} = R_1 = 500 \Omega, C_L = 50 pF$	$2.5 \pm 0.2$	0.8	2.5	4.0	0.8	4.1	
		$R_{L} = R_1 = 500 \Omega, C_L = 50 pF$	$3.3 \pm 0.3$	0.8	2.1	3.2	0.8	3.7	
		$R_{L} = R_1 = 500 \Omega, C_L = 50 pF$	$5.0\pm0.5$	0.5	1.2	3.0	0.5	3.5	

## **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	$V_{CC} = 5.5 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	2.5	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC}$ = 5.5 V, $V_{I}$ = 0 V or $V_{CC}$	4.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)	10 MHz, $V_{CC}$ = 5.5 V, $V_{I}$ = 0 V or $V_{CC}$	4.0	pF

<sup>6.</sup>  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$ .  $C_{PD}$  is used to determine the no–load dynamic power consumption;  $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$ .

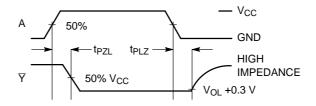
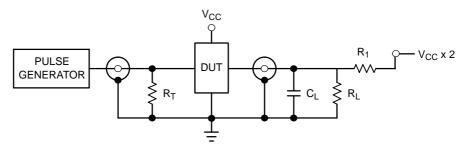


Figure 3. Switching Waveforms



 $R_T = Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )

Figure 4. Test Circuit

## **DEVICE ORDERING INFORMATION**

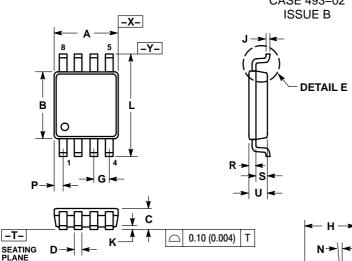
Device Order Number	Package Type	Tape and Reel Size <sup>†</sup>		
NL37WZ06US	US8	178 mm (7"), 3000 Units / Tape & Reel		
NL37WZ06USG	US8 (Pb-Free)	178 mm (7"), 3000 Units / Tape & Reel		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

## US8 **US SUFFIX**

CASE 493-02



#### NOTES:

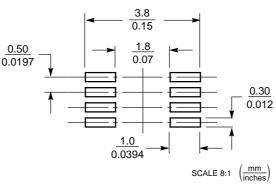
**R 0.10 TYP** 

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION "A" DOES NOT INCLUDE MOLD
- FLASH, PROTRUSION OR GATE BURR.
  MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM
- 0.0055") PER SIDE.
  DIMENSION "B" DOES NOT INCLUDE
  INTER-LEAD FLASH OR PROTRUSION.
  INTER-LEAD FLASH AND PROTRUSION SHALL NOT E3XCEED 0.140 (0.0055") PER SIDE
- LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300–800 °).
  ALL TOLERANCE UNLESS OTHERWISE
- SPECIFIED ±0.0508 (0.0002 ").

		MILLIMETERS		INC	HES	
	DIM	MIN	MAX	MIN	MAX	
	Α	1.90	2.10	0.075	0.083	
	В	2.20	2.40	0.087	0.094	
	C	0.60	0.90	0.024	0.035	
	D	0.17	0.25	0.007	0.010	
,	F	0.20	0.35	0.008	0.014	
	G	0.50	BSC	0.020	BSC	
	H	0.40	REF	0.016 REF		
	7	0.10	0.18	0.004	0.007	
	K	0.00	0.10	0.000	0.004	
	L	3.00	3.20	0.118	0.126	
	М	0 °	6 °	0 °	6 °	
	Ν	5 °	10 °	5 °	10 °	
	Ρ	0.23	0.34	0.010	0.013	
	R	0.23	0.33	0.009	0.013	
	S	0.37	0.47	0.015	0.019	
	U	0.60	0.80	0.024	0.031	
	٧	0.12 BSC		0.005	BSC	

#### F **DETAIL E**

**SOLDERING FOOTPRINT\*** 



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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