MOTOROLA

MC14406
MC14407

Advanced Information

CMOS LSI
(LOW POWER COMPLEMENTARY MOS)

FULL DUPLEX 8-BIT COMPANDED PCM CODEC

PULSE CODE MODULATION (PCM) CODEC

The MC14406 and MC14407 per channel PCM codecs are designed for 8000-samples-per-second, 8-bit-per-sample voice coding and decoding. These devices are full duplex and provide both Mu and A companding laws.

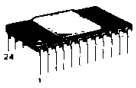
The transmit and receive data rates are independently selectable from 64 kHz to 3.088 MHz allowing direct interface to 24, 30, 32, and 48 channel digital frames.

Both codecs are fabricated using CMOS technology for reliable low power performance. The MC14406 is the full feature device in a 28-pin package. The MC14407 provides a 24-pin package without signaling capabilites.

- Per Channel Full Duplex Capability
- Low Power Operation – 80 mW Typ
- Power Down Input (1.0 mW Max in Power Down Mode)
- Pin Selection of A-law and Mu-law Companding (MC14407)
- Single Power Supply Operation – 10 to 16 volts
- Zero Code Suppression
- Transmit and Receive Signaling Available (MC14406)
- Independent Transmit and Receive Clocks to 3.088 MHz
- Externally Selectable Full Scale
- On-Chip Auto Zero

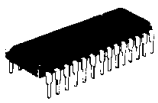
24-PIN PACKAGE

CASE 709 – PLASTIC

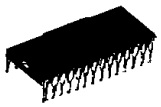


CASE 716 – CERAMIC

28-PIN PACKAGE



CASE 710 – PLASTIC

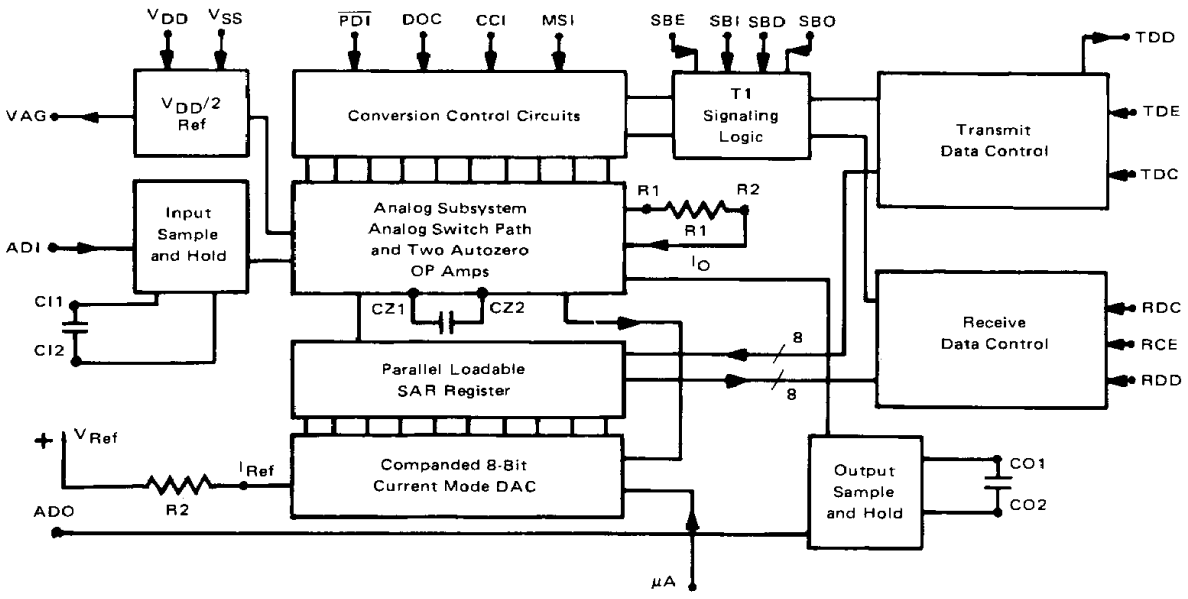


CASE 719 – CERAMIC

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

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MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to +18	Vdc
Voltage, Any Pin to V_{EE}	V	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin (Excluding V_{DD})	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	10	12	16	Vdc
Convert Clock Freqency	CCI	128	128	512	kHz
Transmit Data Clock Frequency	TDC	128	2048	3088	kHz
Receive Data Clock Frequency	RDC	128	2048	3088	kHz
Input Sample Capacitor	CI1, CI2	0.001	0.002	0.010	μF
Output Sample Capacitor	CO1, CO2	0.001	0.002	0.010	μF
Unit Step Size = Full Scale/4096	ADO	0.36	0.85	1.2	mV
Full Scale Voltage (V_{DD} = 15 V)	ADO	1.5	3.5	5.0	Vp
Load Bias Resistor	VAG	2.0	–	–	kΩ
Bypass Capacitor	VAG	–	0.1	–	μF
Auto Zero Capacitor	CZ1, CZ2	–	0.002	–	μF

SYSTEM PERFORMANCE A-to-D through D-to-A (R1 = 25 kΩ, R2 = 2.27 kΩ, T_A = 25°C)

Characteristic		Min	Typ	Max	Unit
Signal to Noise Ratio $\frac{S+N+D}{N+D}$	+3.0 to −30 dBm	33	36	–	dB
	−40 dBm	27	30	–	
C Message at f = 1020 Hz	−45 dBm	22	25	–	dB
Deviation from Level Linearity	+3.0 to −35 dBm	−0.5	–	+0.5	dB
	−35 to −45 dBm	−0.10	–	+1.0	dB
Idle Channel Noise (ADI = VAG)		–	0	12	dBmC
Quiet Code		–	–	–	

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This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DIGITAL ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Operating Current (R2 = 25 k)	I	12	–	–	–	8.0	–	–	–	mA
Power-Down Current ($\overline{PDI}$ = V_{SS})	I_{PD}	12	–	–	–	30	80	–	–	μA
Input Current										
CCI, RDD, RCE, RDC, TDC, $\overline{PDI}$	I_{in}	12	–	–	–	±0.00001	±0.3	–	–	μA
DOC, SBD, MSI, SBI, SBE	I_{inS}		–	–	–	+30	–	–	–	
(Internal Pull-Down Resistors)	I_{inD}		–	–	–	-0.00001	-0.3	–	–	
TDE, Mu/A-Law	I_{inS}		–	–	–	+0.00001	+0.3	–	–	
(Internal Pull-Up Resistors)	I_{inD}		–	–	–	-30	–	–	–	
Input Voltage "0" Level	V_{IL}	12	–	–	–	5.25	3.60	–	–	V
		15	–	–	–	6.75	4.0	–	–	
"1" Level	V_{IH}	12	–	–	8.4	6.75	–	–	–	V
		15	–	–	11	8.25	–	–	–	
Input Capacitance	C_{in}	12	–	–	–	5.0	7.5	–	–	pF
Output Drive Current SBO										
V_{OH} = 11	I_{OH}	12	–	–	-2.0	-4.0	–	–	–	mA
V_{OH} = 13.5		15	–	–	-3.0	-8.8	–	–	–	
V_{OL} = 1.0	I_{OL}	12	–	–	2.0	4.0	–	–	–	mA
V_{OL} = 1.5		15	–	–	3.0	8.8	–	–	–	
Output Drive Current TDD										
V_{OH} = 11	I_{OH}	12	–	–	-4.0	-8.0	–	–	–	mA
V_{OH} = 13.5		15	–	–	-6.0	-17.6	–	–	–	
V_{OL} = 1.0	I_{OL}	12	–	–	4.0	8.0	–	–	–	mA
V_{OL} = 15		15	–	–	6.0	17.6	–	–	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

Characteristic	Pin	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Analog Ground Voltage	VAG	–	–	6.0	6.05	6.1	–	–	V
Source Current		–	–	–	200	–	–	–	μA
Sink Current		–	–	–	5.0	–	–	–	mA
Output Impedance		–	–	–	50	–	–	–	Ω
Reference Input Current	I_{ref}	–	–	50	100	200	–	–	μA
Input Offset Voltage		–	–	–	±10	+25	–	–	mV
Offset Voltage Drift		–	–	–	30	100	–	–	μV/°C
Input Impedance dc	ADI	–	–	1.0	10	–	–	–	MΩ
AC (Ω) CI = 0.002 nF, 1 kHz		–	–	–	80	–	–	–	kΩ
Lower Common Mode Ring		–	–	–	2.0	2.5	–	–	V
Upper Common Mode Ring		–	–	9.5	10	–	–	–	V
Sample Duty Cycle	ADO	–	–	–	3/16	–	–	–	–
Neutral Duty Cycle		–	–	–	13/16	–	–	–	–
Neutral Offset (From VAG)		–	–	-25	+25	+25	–	–	mV
Neutral Offset Drift		–	–	–	30	100	–	–	μV/°C
Source Current		–	–	–	200	–	–	–	mA
Sink Current		–	–	–	5.0	–	–	–	mA
Lower Common Mode Ring		–	–	–	2.0	2.5	–	–	V
Upper Common Mode Ring		–	–	9.5	10	–	–	–	V
Output Impedance		–	–	–	100	–	–	–	Ω
Settling Time to 3.0 V R and F		–	–	–	0.3	–	–	–	μs

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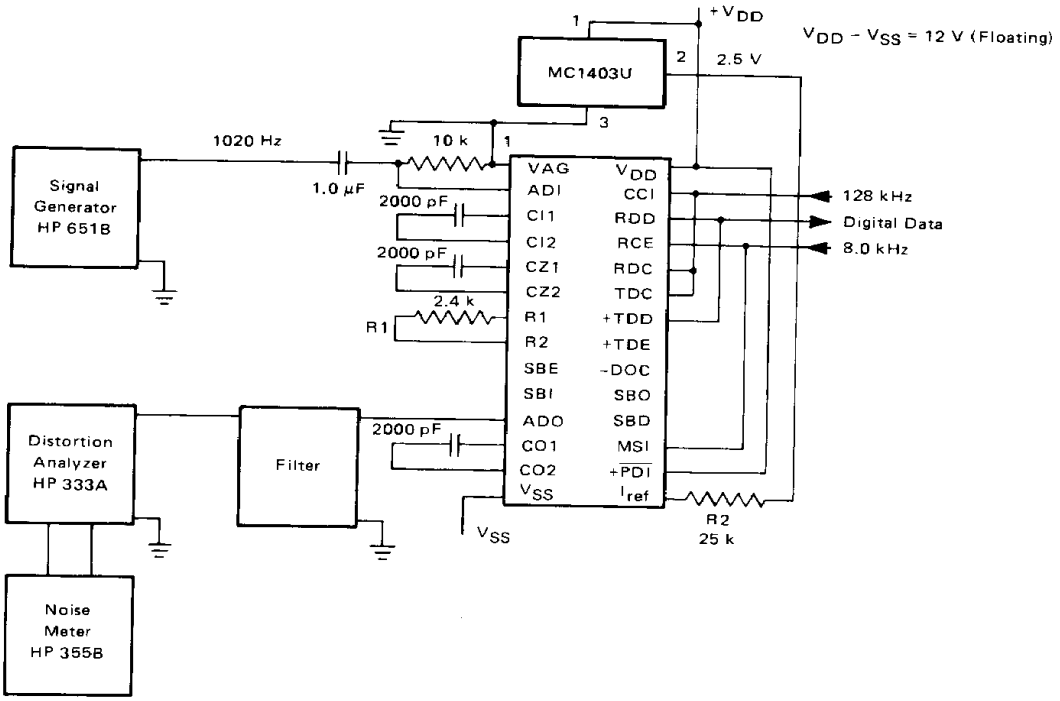
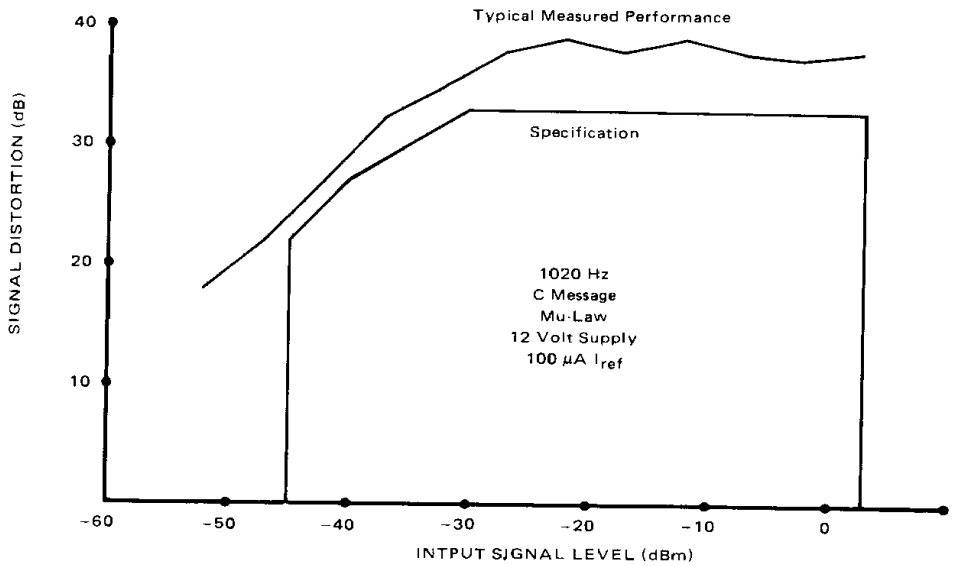
TEST CIRCUIT

MC14406 NOISE PERFORMANCE DATA



NOISE PERFORMANCE OF MC14406



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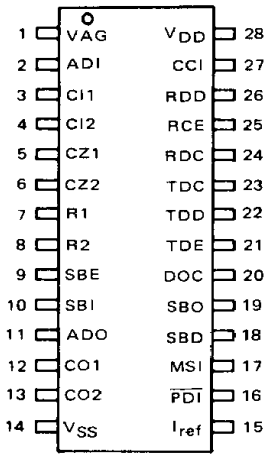
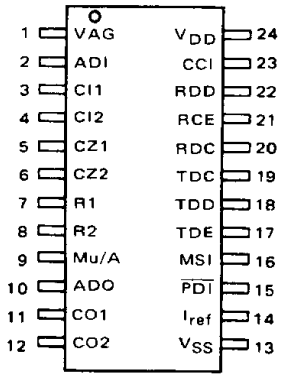
PIN DESCRIPTION





VAG – Analog Ground Output (V_{DD}–V_{SS})/2. VAG is the output of the internal (V_{DD}–V_{SS})/2 voltage reference. A pull-up load resistor and bypass capacitor may be required if this output is to be used elsewhere in the system. This pin serves as the analog ground.

ADI – Analog Data Input. The band-limiting input filter between the channel unit hybrid and the codec drive pin 2. Driver source impedance should be 600 Ω or less. This is the voice input to the codec and will be sampled at 8.0 kHz.

CI1, CI2 – Input Sample Capacitor. The input sample capacitor is connected to these pins. A 2000 pF silver mica capacitor is recommended.

CZ1, CZ2 – Auto Zero Capacitor. The auto zero circuit requires a 2000 pF capacitor between these pins.

R1, R2 – Gain Resistor. The V-to-I conversion resistor is connected between these pins. Gain is established by the ratio of this resistor and the resistor at pin I_{ref}.

Mu/A – Mu-Law/A-Law Select (Internal Pull-Up). Selection of Mu-law or A-law coding is provided for logic control. An internal pull-up provides Mu-law output. An external connection to V_{SS} provides A-law operation.

SBE – Signal Bit Enable (Internal Pull-Down). SBE controls the insertion of transmit signaling bits into the transmit data register. When taken high, the next transmit word will contain the SBI pin level in the LSB position rather than the last bit of the PCM word. If kept high, the SBI data will be inserted in succeeding conversions until one conversion after it is brought low. It can be used for on-hook signaling or A and B signaling in D3 banks.

SBI – Signal Bit Input (Internal Pull-Down). SBI is the data input for transmitting signaling bits. The level of SBI will be latched on the leading edge of SBE, or by the internal latch data pulse if SBE is held high. If SBE is pulsed, the leading edge of SBE will latch SBI, and load it into the next transmit word.

ADO – Analog Data Output. ADO outputs the received PAM sample for three convert clock cycles beginning with MSI. It then returns to the output neutral voltage which may be a few millivolts different from VAG1.

CO1, CO2 – Output Sample Capacitor. The output sample capacitor is connected between these pins. A silver mica capacitor of 2000 pF is recommended.

V_{SS} – Most Negative Supply. This is the most negative supply pin, and the digital ground. All digital inputs and outputs will swing the full supply voltage.

I_{ref} – Current Reference Input. A reference current of 50 to 200 μA sets the full scale DAC current. An 80 μA input current corresponds to 1.28 mA full scale DAC current at pin R2.

$\overline{PDI}$ – Power-Down Input. $\overline{PDI}$ deactivates the codec when pulsed to V_{SS}. In the power-down mode the analog circuitry bias is turned off and the digital clock inputs are disabled. Power-down dissipation is less than 1.0 mW.

MSI – Master Sync Input (Internal Pull-Down). The MSI leading edge resets the entire chip to the initial cycle (0000). The chip continues operation on the next leading edge of data and convert clock. MSI also resets the output data multiplexer to the transmit word sign bit.

SBO – Signal Bit Output. SBO outputs the LSB of the receive data register. The LSB may be sampled externally during the first three convert clocks after MSI or used as a trigger pulse in off-hook applications.

SBD – Signal Bit Decode (Internal Pull-Up). Signal bit decode allows the control of the 1/2 LSB or LSB centering required in sample decode cycles. It is loaded by the RCE edge in each cycle. If a zero is entered, the next decode cycle adds 1/2 LSB to the 8-bit received word to center the quantization error of the 8-bit received sample when the output sample capacitor is charged. If a 1 is loaded by RCE, the 1/2 LSB is not added, and the LSB is forced to

a 1 to form a centered error 7-bit output, and the LSB is ignored and assumed to be signaling information. (For codes 1111111X or 0111111X, the LSB is disabled for SBD high.)

DOC – Decode Only Control (Internal Pull-Down). DOC is normally tied low. When high, it configures the device to skip the eight convert clocks used for A-to-D conversion. The operating cycle is then two clocks for PAM output at ADO and six clocks for charging the next output sample. The device may be used to do as many as four decode cycles in a 125 μs/period with an external transmission gate selector.

Received Data is loaded into the transmit data register at MSI when in DOC mode, so DOC can be used as a digital loop back control.

TDE – Transmit Data Enable (Internal Pull-Up). The Transmit Data Enable is a three-state control for the transmit digital output. A number of codec outputs can be interleaved into a serial stream by connecting the outputs and controlling TDE with a 1-of-N decoder. It will provide switching characteristics capable of 3.088 MHz operation.

TDD – Transmit Digital Data. The Transmit Digital Data rate is controlled by the data clock input, and is frame aligned with the Master Sync Input. If data clock is at 1.544 MHz, and convert clock is at 128 kHz, the new sign bit will be output beginning with the leading edge of convert clock 8, and the 8-bit word repeated throughout the convert cycle at the data clock rate. The data word is inverted offset binary with zero code suppression. See Conversion and Data Timing.

TDC – Transmit Data Clock. TDC sets the digital data rate of the codec. The transmit data stream will provide a continuous repetition of the current transmit data word at the TDC bit rate, beginning with MSB first and synchronized with the last MSI. The new data word is loaded and serially output at mid-cycle or on the leading edge of convert clock 8.

RDC – Receive Data Clock. RDC controls the receive data register. It clocks the receive-data register on the trailing edge under the control RCE. It is often connected to TDC.

RCE – Receive Clock Enable. The rising edge of RCE triggers the receive data register to accept a new data input. After the rising edge of RCE, the data on RDD is loaded into the Receive Data Register on the next eight trailing edges of RDC. The ninth clock transfers the new 8-bit word to an internal intermediate register and frees the Receive Data Register for a new RCE.

RDD – Receive Digital Data. RDD is the input to the receive data shift register. It is controlled by RCE. The register is clocked on the trailing edge of RDC. The data format is sign bit first, inverted offset binary code.

CCI – Convert Clock Input. CCI controls the conversion sequence. A 128 kHz clock will produce 64K-bits/s full duplex operation and a 256K-bits/s clock will produce 64K-bit operation for two channels. Sixteen clocks represent one chip cycle from MSI to MSI.

V_{DD} – Most Positive Supply. V_{DD} is typically 12 V with an operation range of 10 V to 16 V. All logic outputs swing the full supply voltage.

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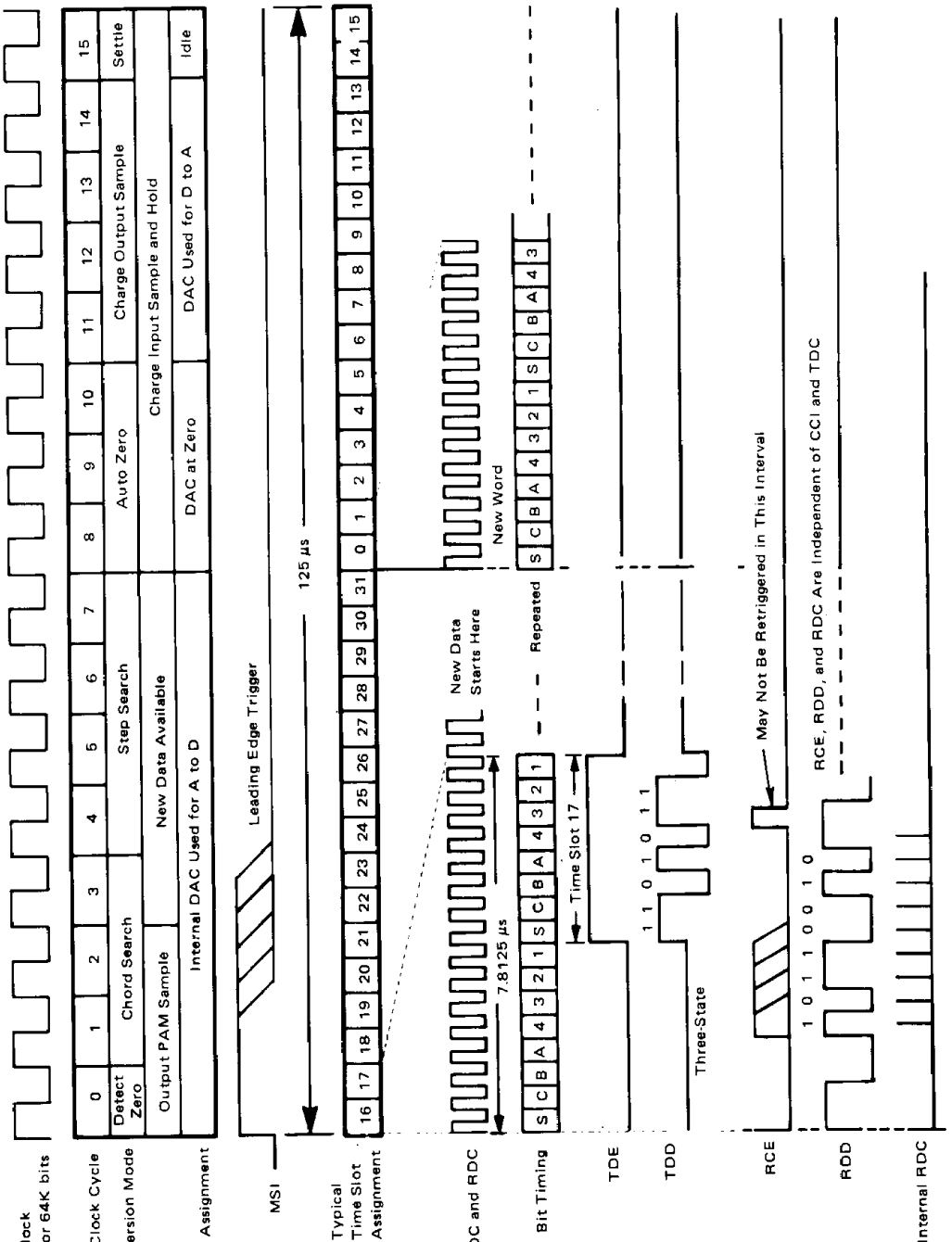
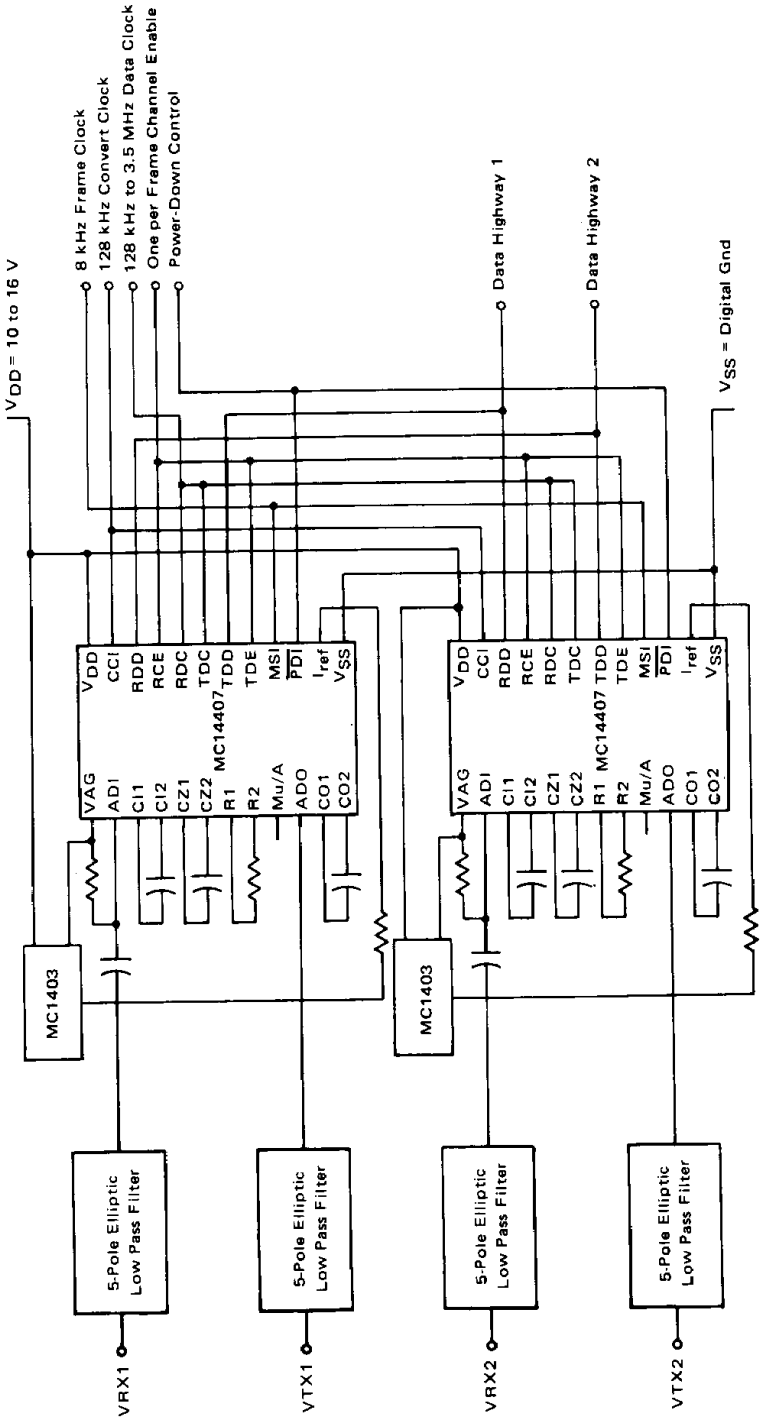
CONVERSION AND DATA TIMING FOR 64K BIT CHANNEL IN 2.048 MEGABIT FRAME



TYPICAL DIGITAL SWITCHING APPLICATION OF MC14407



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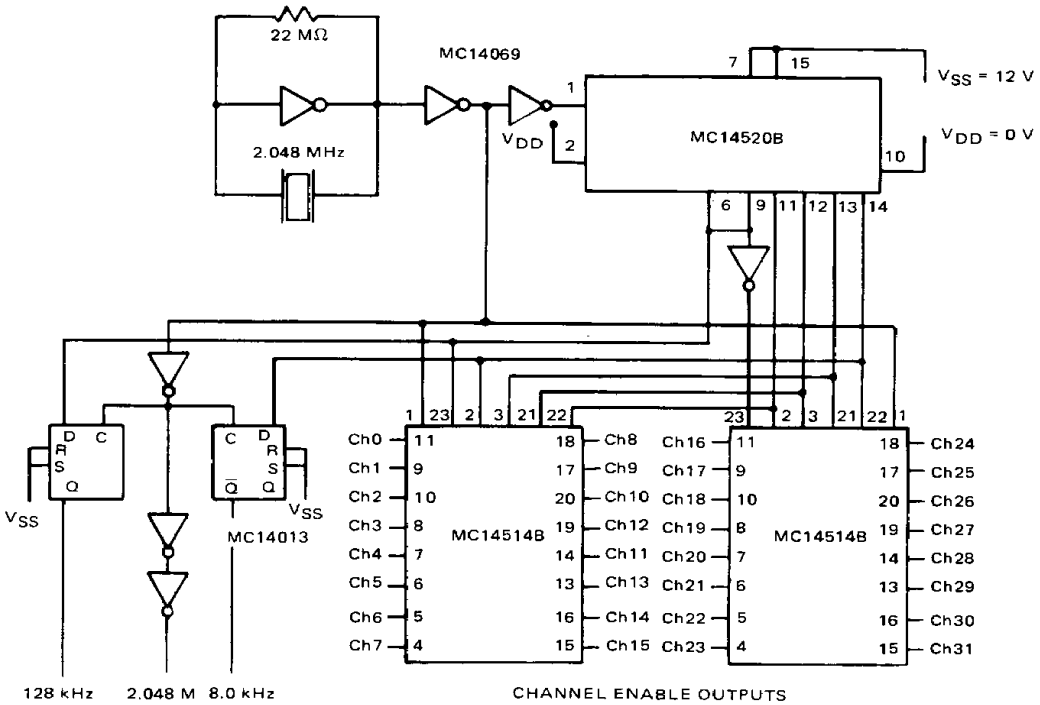
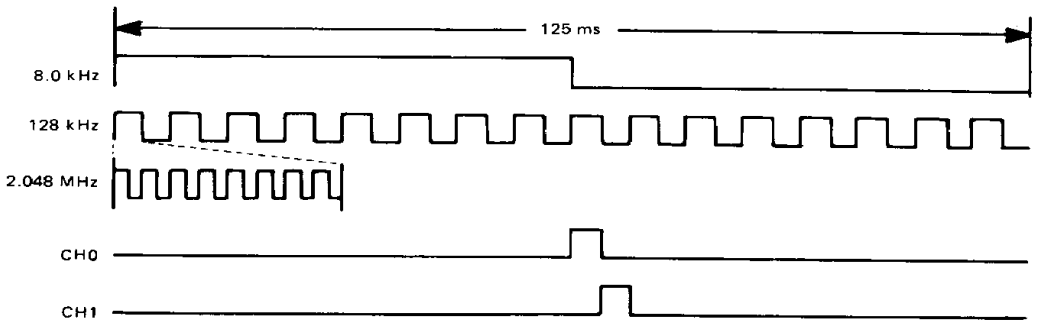
TYPICAL CMOS COMMON CLOCK GENERATOR





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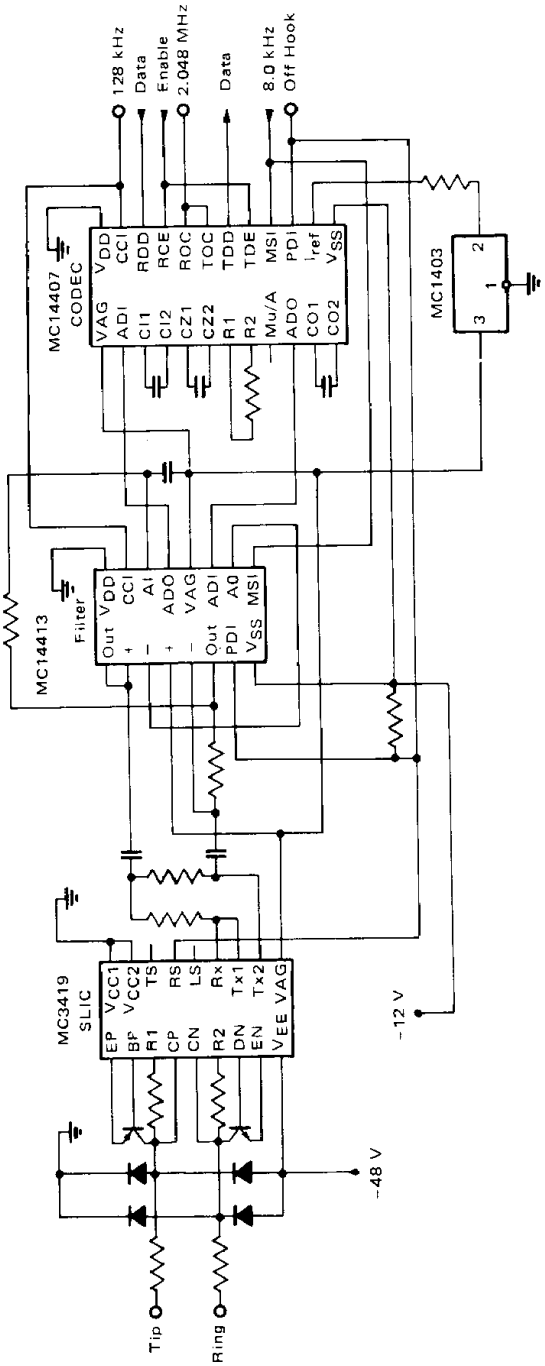
PROPOSED MOTOROLA 3-CHIP SUBSCRIBER CHANNEL UNIT



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