

**MJE13007****NPN SILICON TRANSISTOR**

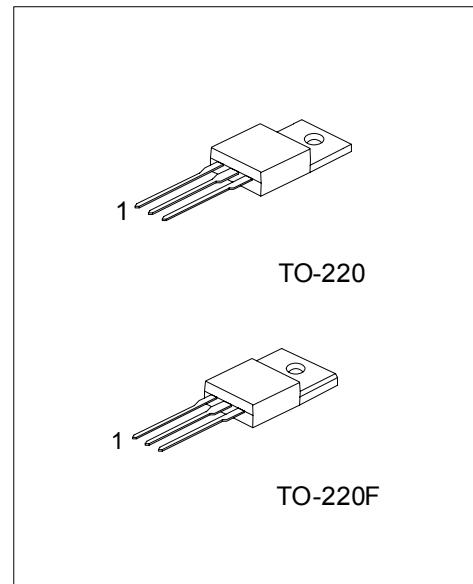
**NPN BIPOLAR POWER  
TRANSISTOR FOR SWITCHING  
POWER SUPPLY  
APPLICATIONS**

■ **DESCRIPTION**

The UTC **MJE13007** is designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V switch mode applications.

■ **FEATURES**

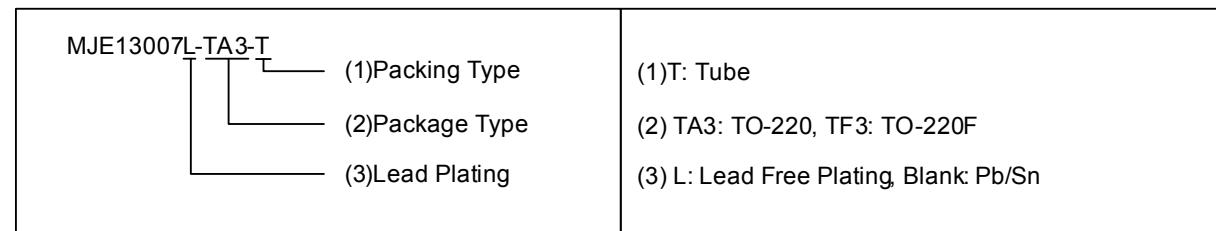
- \*  $V_{CEO(SUS)}$  400 V
- \* 700 V Blocking Capability



\*Pb-free plating product number: MJE13007L

■ **ORDERING INFORMATION**

Order Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
MJE13007-TA3-T	MJE13007L-TA3-T	TO-220	B	C	E	Tube
MJE13007-TF3-T	MJE13007L-TF3-T	TO-220F	B	C	E	Tube



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Collector-Emitter Sustaining Voltage	$V_{CEO}$	400	V
Collector-Emitter Breakdown Voltage	$V_{CBO}$	700	V
Emitter-Base Voltage	$V_{EBO}$	9.0	V
Collector Current	Continuous	$I_C$	8.0
	Peak (1)	$I_{CM}$	16
Base Current	Continuous	$I_B$	4.0
	Peak (1)	$I_{BM}$	8.0
Emitter Current	Continuous	$I_E$	12
	Peak (1)	$I_{EM}$	24
Total Device Dissipation	$T_C = 25$	$P_D$	80
Operating and Storage Junction Temperature Range	$T_J, T_{STG}$	-65 ~ +125	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction to Case	$\theta_{JC}$	1.56	/W
Thermal Resistance Junction to Ambient	$\theta_{JA}$	62.5	/W

Note 1: Pulse Test: Pulse Width = 5.0 ms, Duty Cycle≤10%.

Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8•lbs.

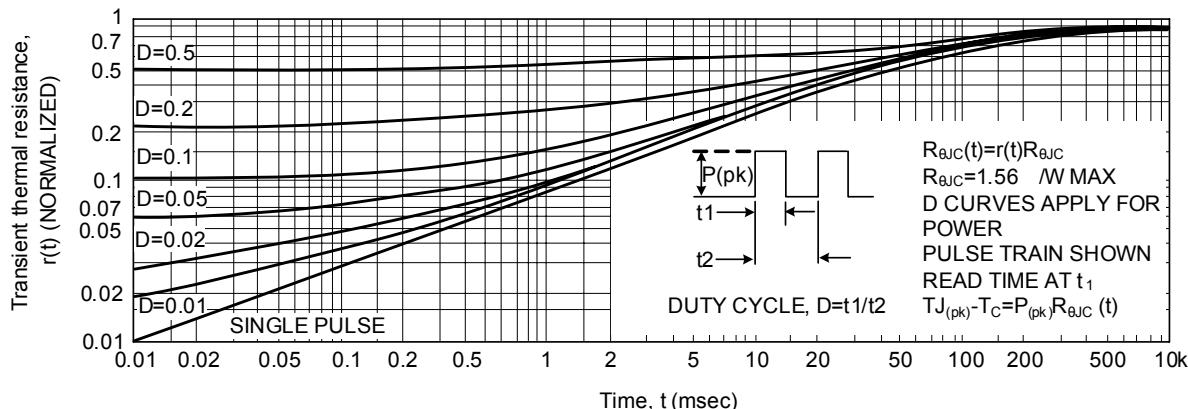
■ ELECTRICAL CHARACTERISTICS ( $T_C=25^\circ C$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Collector-Emitter Sustaining Voltage	$V_{CEO(SUS)}$	$I_C=10mA, I_B=0$	400			V
Collector Cutoff Current	$I_{CBO}$	$V_{CBO}=700V$			0.1	mA
		$V_{CBO}=700V, T_C=125^\circ C$			1.0	mA
Emitter Cutoff Current	$I_{EBO}$	$V_{EB}=9.0V, I_C=0$			100	μA
DC Current Gain	$h_{FE1}$	$I_C=2.0A, V_{CE}=5.0V$	8.0	40		
	$h_{FE2}$	$I_C=5.0A, V_{CE}=5.0V$	5.0		30	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C=2.0A, I_B=0.4A$			1.0	V
		$I_C=5.0A, I_B=1.0A$			2.0	V
		$I_C=8.0A, I_B=2.0A$			3.0	V
		$I_C=5.0A, I_B=1.0A, T_C=100^\circ C$			3.0	V
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	$I_C=2.0A, I_B=0.4A$			1.2	V
		$I_C=5.0A, I_B=1.0A$			1.6	V
		$I_C=5.0A, I_B=1.0A, T_C=100^\circ C$			1.5	V
Current-Gain-Bandwidth Product	$f_T$	$I_C=500mA, V_{CE}=10V, f=1.0 \text{ MHz}$	4.0	14		MHz
Output Capacitance	$C_{ob}$	$V_{CB}=10V, I_E=0, f=0.1\text{MHz}$		80		pF
Resistive Load (Table 1)						
Delay Time	$t_D$	$V_{CC}=125V, I_C=5.0A,$ $I_{B1}=I_{B2}=1.0A, t_p=25\mu s,$ Duty Cycle 1.0%		0.025	0.1	μs
Rise Time	$t_R$			0.5	1.5	
Storage Time	$t_S$			1.8	3.0	
Fall Time	$t_F$			0.23	0.7	

\* Pulse Test: Pulse Width 300 μs, Duty Cycle 2.0%

■ TYPICAL THERMAL RESPONSE

Figure1. Typical Thermal Response



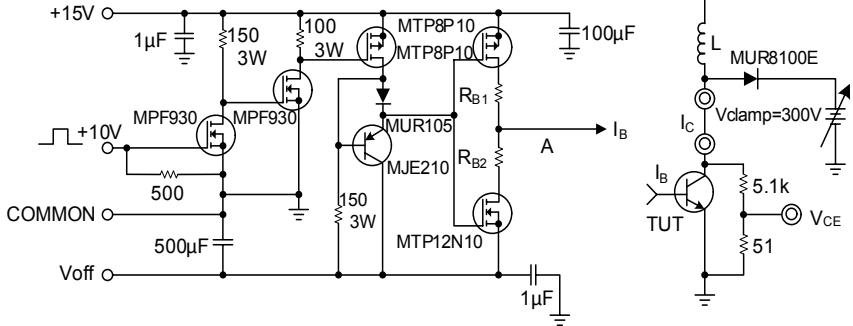
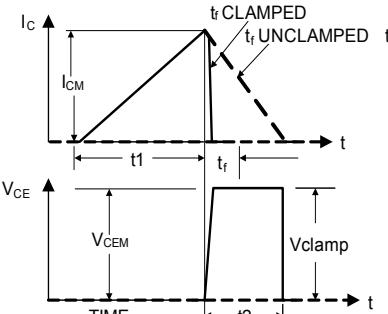
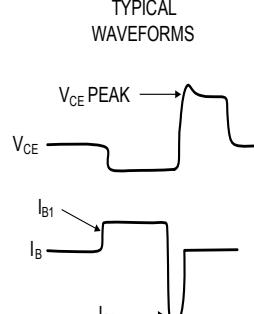
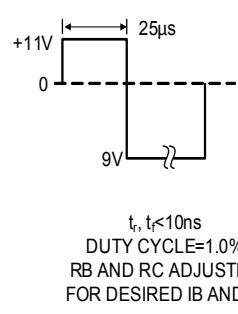
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C-V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on  $T_C = 25^\circ C$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be debated when  $T_C \geq 25^\circ C$ . Second breakdown limitations do not debate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

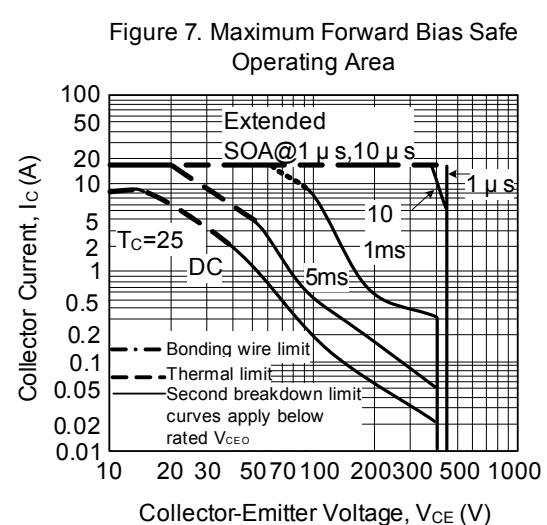
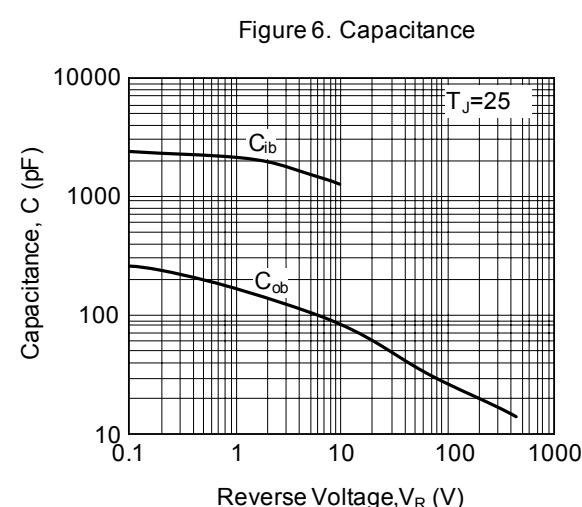
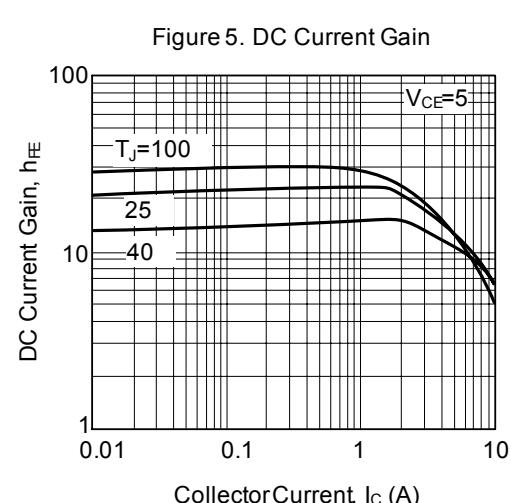
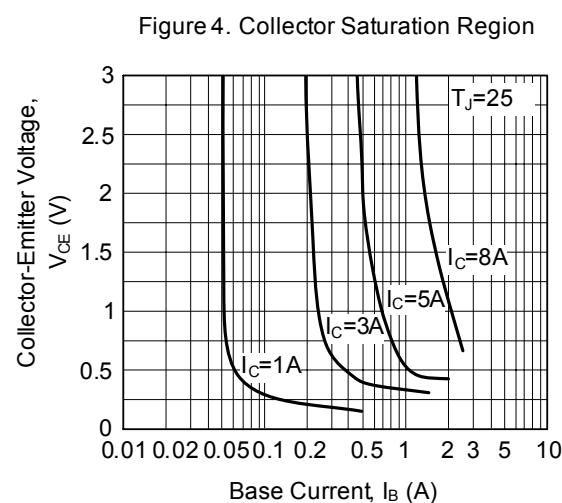
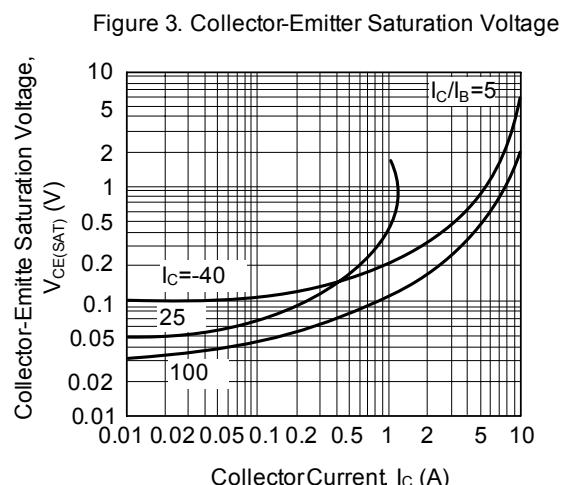
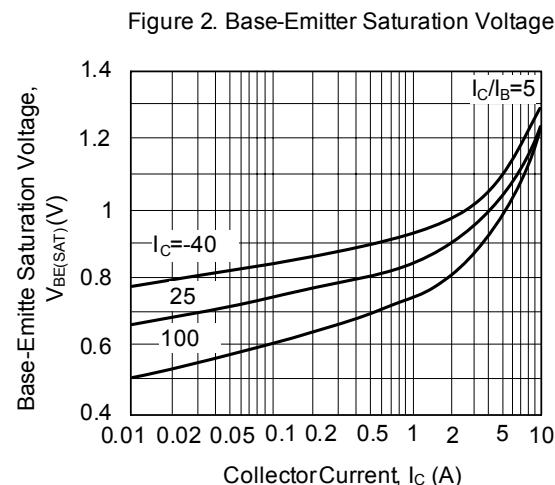
At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 8) is discussed in the applications information section.

Table 1. Test Conditions for Dynamic Performance

TEST CIRCUITS	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING	
				
CIRCUIT VALUES	BV <sub>CEO</sub> (SUS)	Inductive Switching	RBSOA	
	L=10mH R <sub>B2</sub> =8 V <sub>CC</sub> =20V I <sub>C(pk)</sub> =100mA	L=20mH R <sub>B2</sub> =0 V <sub>CC</sub> =15V R <sub>B1</sub> selected for desired I <sub>B1</sub>	L=500mH R <sub>B2</sub> =0 V <sub>CC</sub> =15Volts R <sub>B1</sub> selected for desired I <sub>B1</sub>	V <sub>CC</sub> =125V R <sub>C</sub> =25Ω D1=1N5820 OR EQUIV
		t <sub>1</sub> CLAMPED t <sub>1</sub> UNCLAMPED t <sub>2</sub> t <sub>1</sub> ADJUSTED TO OBTAIN I <sub>C</sub> t <sub>1</sub> $\frac{L_{coil}(I_{CM})}{V_{CC}}$ t <sub>2</sub> $\frac{L_{coil}(I_{CM})}{V_{clamp}}$ TEST EQUIPMENT SCOPE-TEKTRONIX 475 OR EQUIVALENT		 +11V    25μs 0 9V t, t_f<10ns DUTY CYCLE=1.0% RB AND RC ADJUSTED FOR DESIRED IB AND IC

### ■ TYPICAL CHARACTERISTICS



### ■ TYPICAL CHARACTERISTICS

Figure 8. Maximum Reverse Bias  
Switching Safe Operating Area

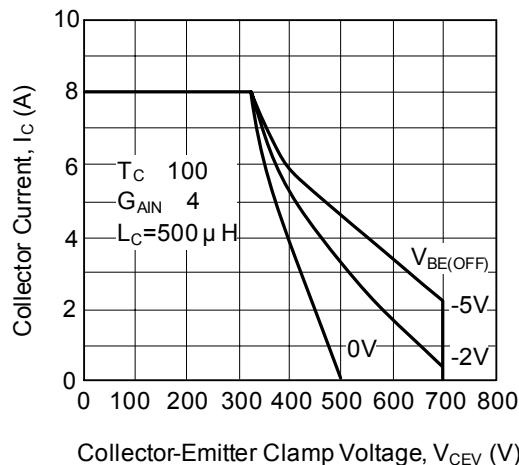


Figure 9. Forward Bias Power Derating

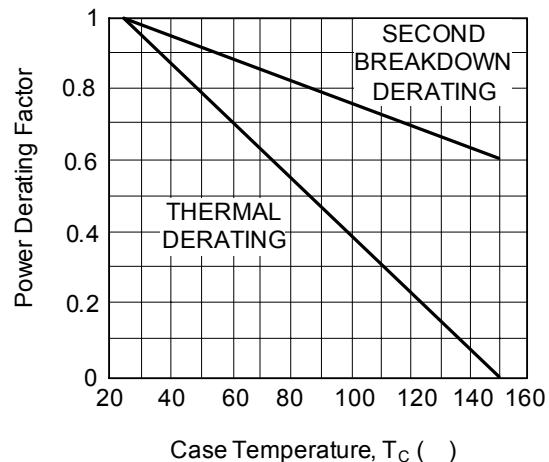


Figure 10. Turn-On Time(Resistive Load)

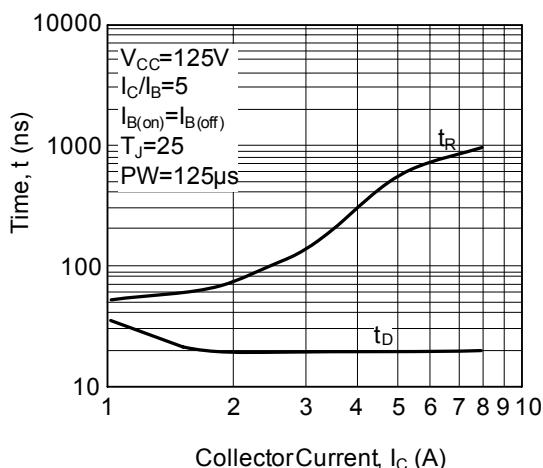
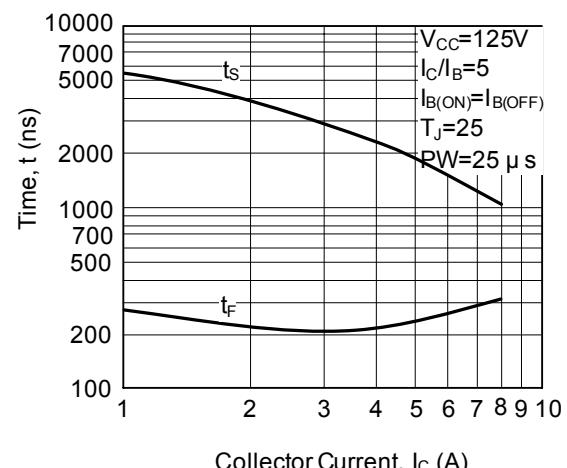


Figure 11. Turn-Off Time(Resistive Load)



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